# Suppression of the Boron Penetration Induced Dielectric Degradation by Using a Stacked-Amorphous-Silicon Film as the Gate Structure for pMOSFET

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*Abstract*— **This work proposes a stacked-amorphous-silicon (SAS) film as the gate structure of the $p^+$ poly-Si gate pMOSFET to suppress boron penetration into the thin gate oxide. Due to the stacked structure, a large amount of boron and fluorine piled up at the stacked-Si layer boundaries and at the poly-Si/$SiO_2$ interface during the annealing process, thus the penetration of boron and fluorine into the thin gate oxide is greatly reduced. Although the grain size of the SAS film is smaller than that of the as deposited polysilicon (ADP) film, the boron penetration can be suppressed even when the annealing temperature is higher than 950°C. In addition, the mobile ion contamination can be significantly reduced by using this SAS gate structure. This results in the SAS gate capacitor having a smaller flat-band voltage shift, a less charge trapping and interface state generation rate, and a larger charge-to-breakdown than the ADP gate capacitor. Also the Si/$SiO_2$ interface of the $p^+$ SAS gate capacitor is much smoother than that of the $p^+$ SAS gate capacitor.**

## I. Introduction

Recently, $p^+$ polycrystalline silicon (poly-Si) has been widely used as the gate material of pMOSFET to eliminate the short-channel effects [1]–[3]. In addition to the reliable process control for subthreshold characteristics and the threshold voltage adjustment, the $p^+$ poly-Si gate pMOSFET is also more resistant to the hot carrier induced instability than is the $n^+$ poly-Si gate pMOSFET [4].

The $BF_2$ implantation is typically used to form the $p^+$ poly-Si gate as well as the shallow $p^+$-$n$ junction [5]. Unfortunately, the $F$-incorporated $p^+$ poly-Si gate can not only enhance the boron penetration through the thin gate oxide into the Si substrate but also cause the generation of negative-charge interface states [5]–[8]. This results in a large threshold voltage shift, a large charge trapping rate and a poor reliability of device [5]–[8]. It has also indicated that the more fluorine atoms pile up at the poly-Si/$SiO_2$ and Si/$SiO_2$ interfaces, the more serious the boron penetration occurs [9]. Moreover, the $p^+$ poly-Si gate MOS devices are more susceptible to the mobile ion contamination than are the $n^+$ poly-Si gate MOS devices [10]. To avoid the boron penetration effect and simultaneously to form a shallow $p^+$-$n$ junction, the post-implantation annealing must be performed at a lower temperature, e.g. 850°C, for a short time [11]. However, under such a thermal cycle, it is difficult to sufficiently activate the dopant to degenerate the poly-Si film, especially as a silicide is formed on the poly-Si film [12], [13]. This will cause a depletion effect in the poly-Si film and result in a significant degradation in the device performance [11]–[13].

Recently, it has been reported that the boron penetration effects can be suppressed by using a stacked-amorphous-silicon (SAS) film as the gate structure for pMOSFET [14]. Due to the stacked structure, a large amount of dopants segregate at stacked-Si layer boundaries and at poly-Si/$SiO_2$ interface during the annealing process [14]–[16]. Although the grain size of the SAS film is smaller than that of the ADP film, the boron penetration size of the SAS film is smaller than that of the ADP film, the boron penetration effects can be exactly suppressed even when the annealing temperature is higher than 950°C [14]. In this paper, the characteristics of the $p^+$ SAS gate capacitor are systematically investigated in terms of the amount boron and fluorine penetration into the thin gate oxide, the flat-band voltage shift ($\Delta V_{\mathrm{fb}}$), the dielectric breakdown field ($E_{\mathrm{bd}}$), the charge trapping rate, the interface state generation rate, and the time dependent dielectric breakdown ($Q_{\mathrm{bd}}$). A physical model for suppression of the boron and fluorine penetration into the thin gate oxide with the SAS structure is also proposed.

## II. Experimental Procedures

In this study, $p^+$ poly-Si gate MOS capacitors were fabricated on $n$-type (100) Si wafers with the resistivity of 5–20 Ω-cm. After a standard RCA cleaning process, all wafers were dipped in a diluted HF solution (1:50) to remove the native oxide. Then, the thin oxides of 70 Å and 130 Å were grown at 900°C and 950°C in a dry $O_2$ ambient, respectively. The post-oxidation annealing of all samples were performed at the oxidation temperature for 15 min in an $N_2$ ambient. An LPCVD $\alpha$-Si film with total thickness of about 3 000 Å was subsequently deposited onto the wafers at 550°C in three steps [16]. The deposition pressure and deposition rate were controlled at 140–160 mtorr and 20 Å/min respectively.

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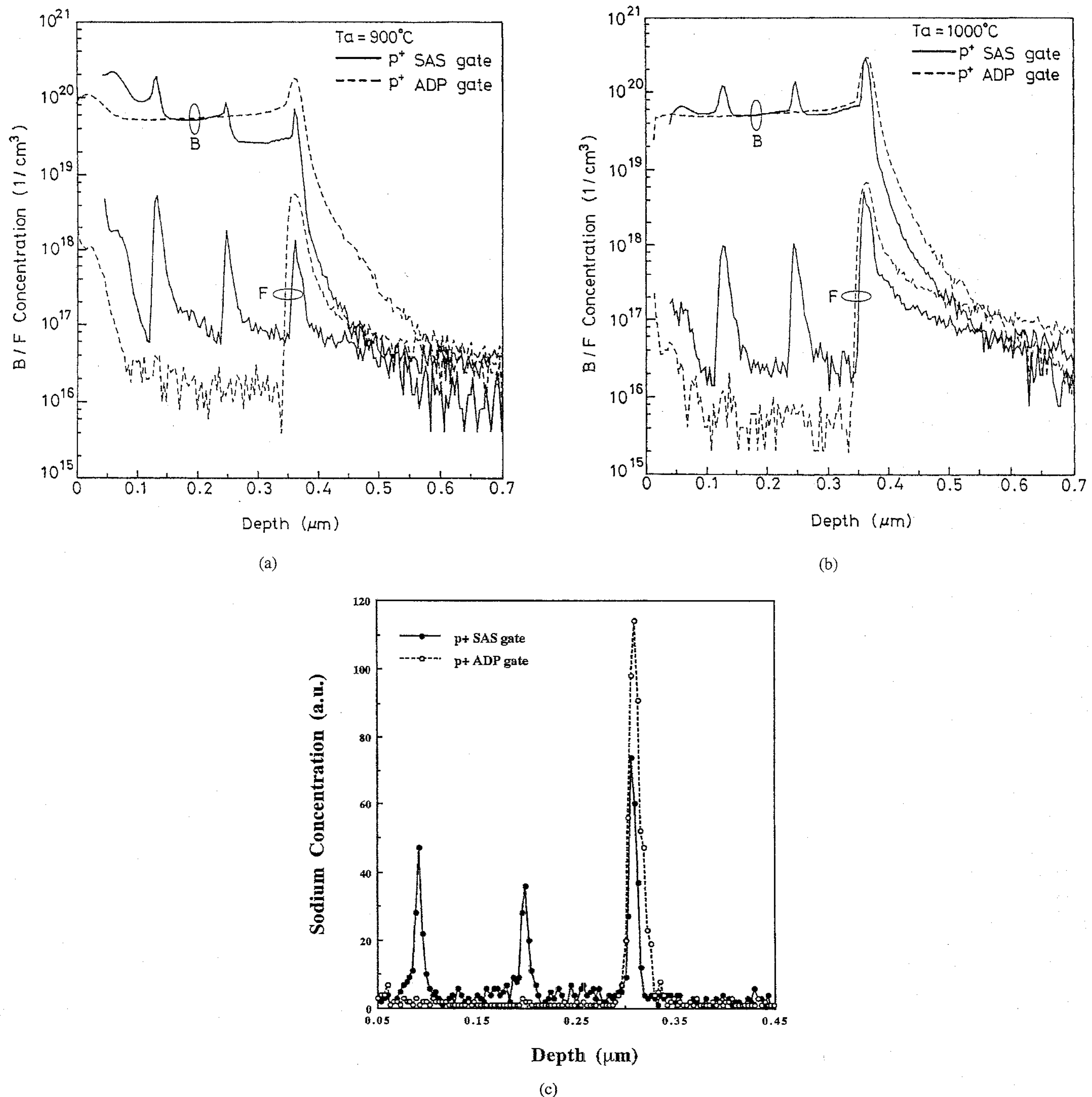
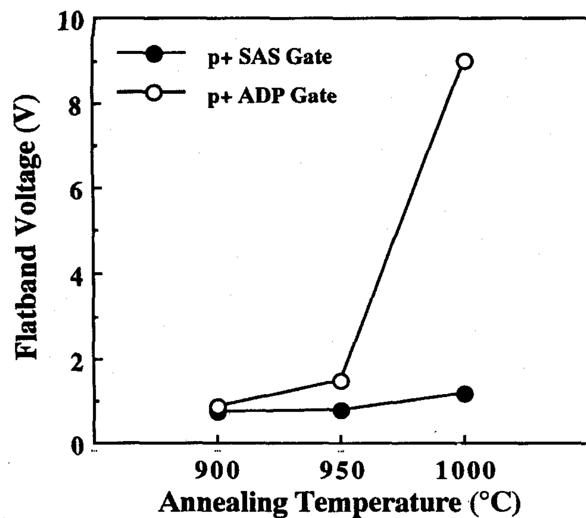


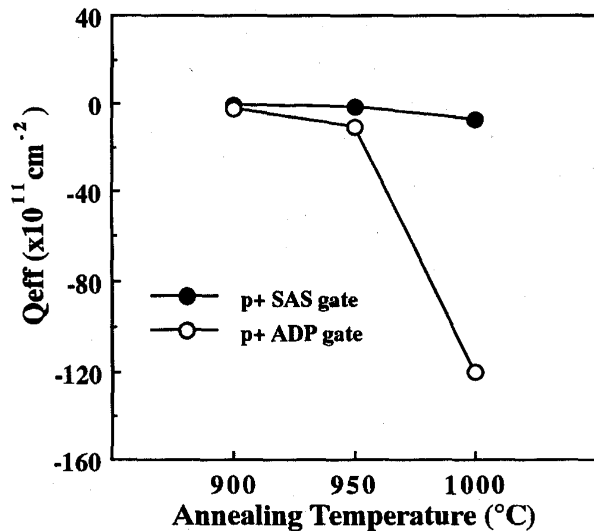

Fig. 1. The SIMS profiles of implanted boron and fluorine of the $p^+$ SAS and ADP gate capacitors annealed at (a) 900°C and (b) 1 000°C, respectively. The initial oxide thickness is 130 Å. (c) The SIMS profiles of sodium ion of the 900°C-annealing $p^+$ SAS (solid line) and ADP (dashed line) gate capacitors with the gate oxide thickness of 130 Å.

The thickness of each $\alpha$-Si layer was about 1 000 Å. During the stacked-Si layer deposition, the LPCVD system was not interrupted. After the first $\alpha$-Si layer deposition, the $SiH_4$ gas was removed and replaced by an $N_2$ gas to purge the LPCVD system for a period of 30 min. By using the same steps, the second and the third $\alpha$-Si layers were deposited on the wafers. During this deposition process, a layer boundary existed between two adjacent $\alpha$-Si layers [16]. To make a comparison, the ADP film of 3 000 Å was deposited at 625°C in one step. The deposition pressure and the deposition rate were 180–220 mtorr and 100 Å/min, respectively. Then, $BF_2$ ion implantation was performed at 50 keV with a dose of $6 \times 10^{15}$ cm$^{-2}$ and annealed at 800°C for 30 min in a dry $O_2$ ambient followed by driving-in at 850, 900, 950, and 1 000°C for 15 min in an $N_2$ ambient. After aluminum metallization, all samples were sintered at 400°C for 20 min in an $N_2$ ambient to form a good ohmic contact.

The I-V characteristics and the time-dependent-dielectric-breakdown (TDDB) characteristics of the $p^+$ poly-Si gate capacitors were measured by using an HP4145B semiconductor parameter analyzer. A constant Fowler-Nordheim (FN) tunneling current stressing was used to study reliability of

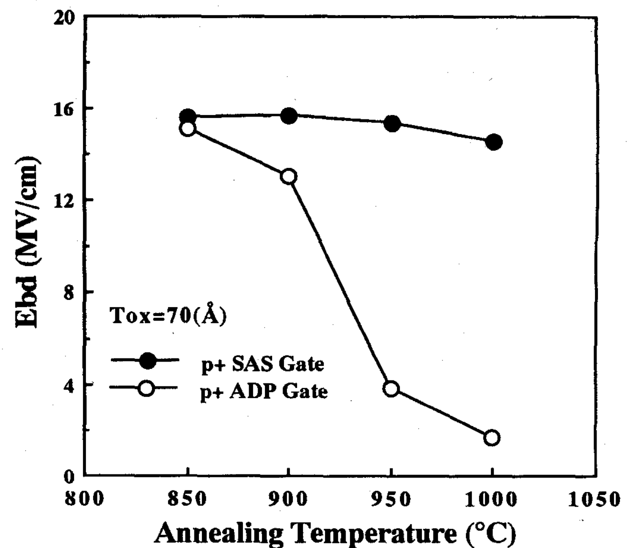



(a)

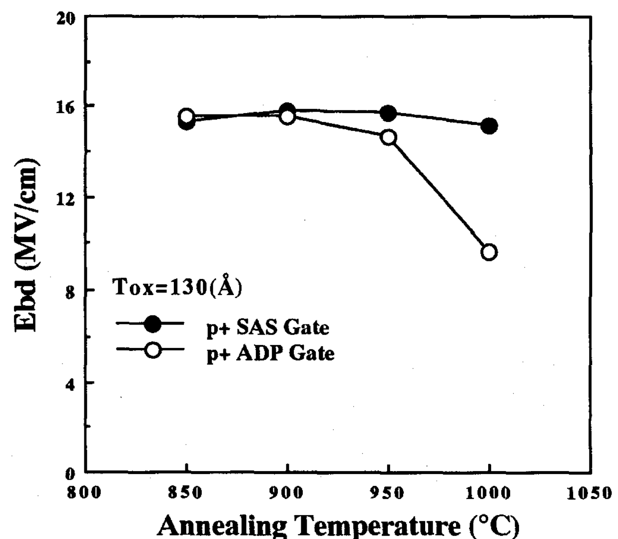



(b)

Fig. 2. The plots of (a) the flat-band voltage ($V_{fb}$), and (b) the effective oxide charge ($Q_{eff}$) versus the annealing temperature from 900°C to 1 000°C for both the $p^+$ SAS and ADP gate capacitors with the oxide thickness of 130 Å, respectively. $Q_{eff}$ is equal to $C_{ox}(\phi$ ms-$V_{fb})$, and $\phi$ ms is the work function difference between the poly-Si gate and Si substrate.




(a)




(b)

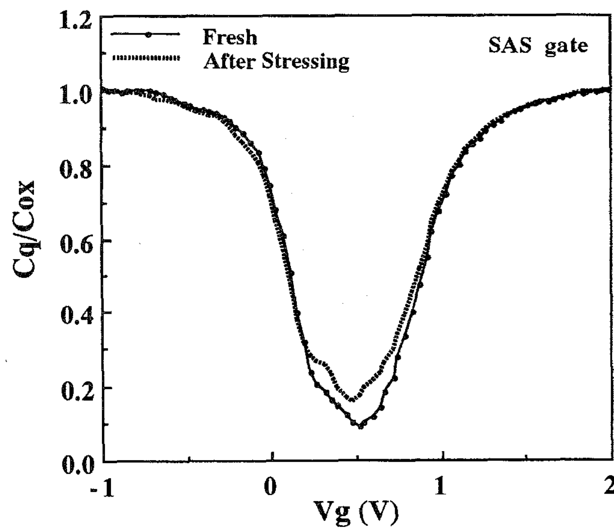
Fig. 3. The plots of the dielectric breakdown field ($E_{bd}$) versus the annealing temperature for $p^+$ SAS and ADP gate capacitors with the initial oxide thickness of (a) 70 Å, and (b) 130 Å, respectively.

the thin oxide capacitors. The oxide thickness and the flat-band voltage shift of the $p^+$ poly-Si capacitors before and after a constant current stressing were monitored by the high-frequency C-V (HFCV) measurements by using the Keithley 590/595 C-V analyzer. The impurity profiles were analyzed by using a VG Ionex SIMS tool with an $O_2^+$ beam for boron, fluorine and sodium analyses.

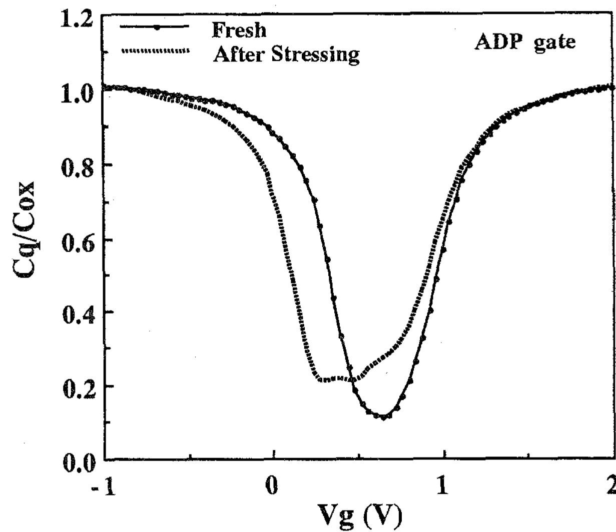
## III. Results and Discussion

### A. SIMS Profiles of the $p^+$ SAS and ADP Gate Capacitors

Fig. 1(a) and (b) compare the SIMS profiles of implanted boron and fluorine of the $p^+$ SAS and ADP gate capacitors annealed at 900°C and 1 000°C, respectively. Fig. 1(c) shows the sodium profiles of the 900°C annealing $p^+$ SAS (solid line) and ADP (dashed line) gate capacitors, respectively. For these capacitors, the initial thickness of the gate oxide was about 130 Å. It is seen that the $p^+$ SAS gate capacitors exhibit three boron and fluorine segregation peaks at the stacked-Si layer boundaries and at the poly-Si/$SiO_2$ interface, while for the $p^+$ ADP gate capacitors, there exists only one peak at the poly-Si/$SiO_2$ interface. The dopant segregation of the $p^+$ SAS gate capacitors are similar to that of the SAS and SPS (stacked-polycrystalline-silicon) emitter contacted $p^+$-$n$ shallow junction diodes [15]. For the $p^+$ SAS gate capacitors, due to the dopant segregation at the stacked-Si/$SiO_2$ interface

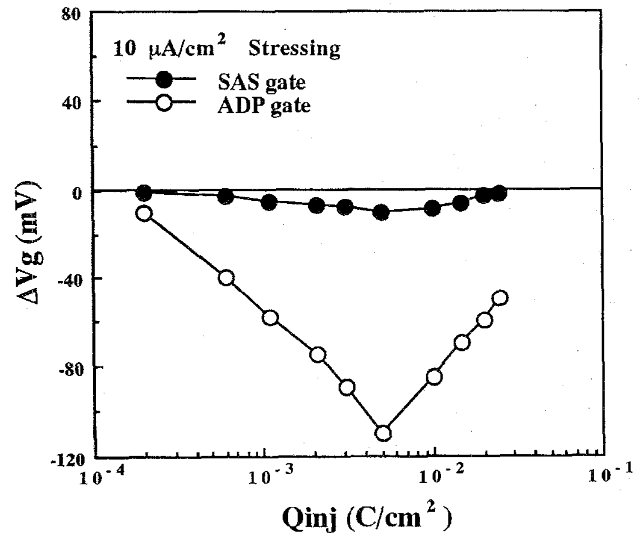



(a)

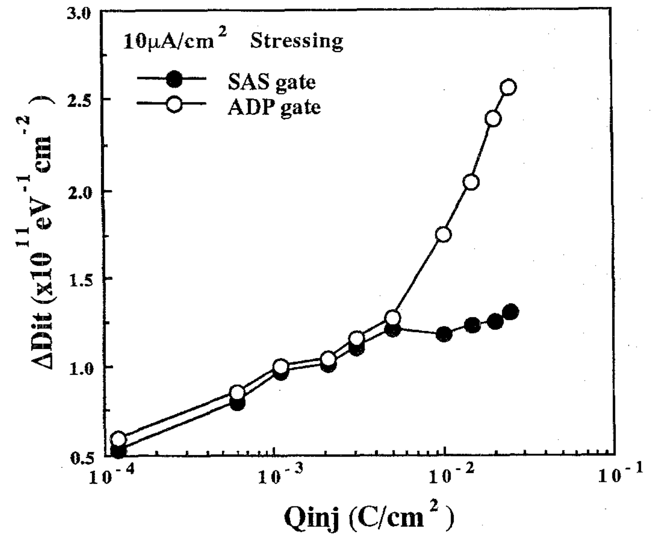



(b)

Fig. 4. The quasistatic C-V characteristics of (a) the $p^+$ SAS gate capacitor and (b) the $p^+$ ADP gate capacitor before and after a constant current of 10 $\mu$A/cm$^2$ stressing for 2 000 s, respectively. The initial gate oxide thickness is 130 Å and the dopant is driven-in at 900°C.




(c)




(d)

Fig. 4. The plots of (c) the gate voltage shift ($\Delta V_g$) and (d) the increase of interface state density ($\Delta D_{\text{it}}$) versus the injection charge ($Q_{\text{inj}}$) of the $p^+$ SAS gate capacitor and the $p^+$ ADP gate capacitor, respectively.

are less than that of the $p^+$ ADP gate capactiors. This in turn causes the boron and fuorine penetration through the thin gate oxide into the Si substrate for the $p^+$ SAS gate capacitors to be less than that of the $p^+$ ADP gate capacitor. In addition, the mobile ion contamination can be significantly reduced by using the SAS gate structure, as shown in Fig. 1(c).

### *B. Electrical Characteristics of the $p^+$ SAS and ADP Gate Capacitors*

As shown in Fig. 1(a) and (b), the amount of boron and fluorine penetration through the thin gate oxide into the Si substrate of the $p^+$ SAS gate capacitor is less than that of the $p^+$ ADP gate capacitor even when the annealing temperature of the $p^+$ SAS gate capacitor is higher. This results in a significant improvement of the flat-band voltage shift, the effective oxide charge, the dielectric breakdown field, the charge trapping rate, the interface state generation rate, and the charge-to-breakdown ($Q_{\text{bd}}$). This will be discussed in the following.

Fig. 2(a) and (b) show the plots of the flat-band voltage and the effective oxide charge versus the annealing temperature from 900°C to 1 000°C for both the $p^+$ SAS and ADP gate capacitors, respectively. $Q_{\text{eff}}$ is equal to $C_{\text{ox}}(\phi$ ms-$V_{\text{fb}})$, and $\phi$ ms is work function difference between the poly-Si gate and the Si substrate [17], [18]. Due to the suppression of the boron and fluorine penetration into the thin gate oxide, the

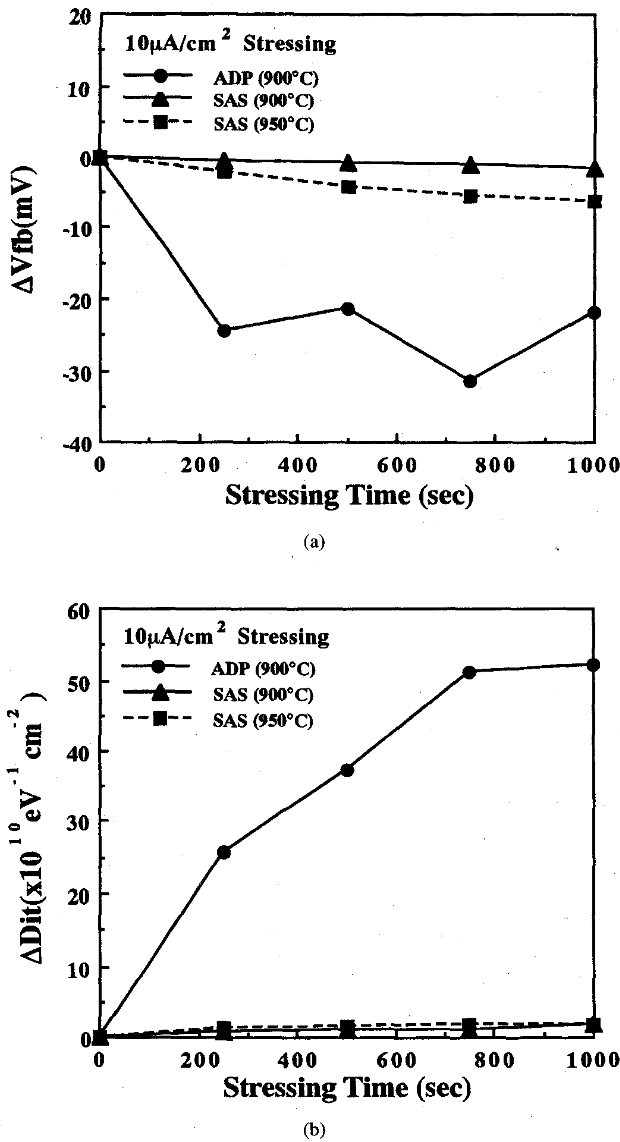



Fig. 5. The plots of (a) the flat-band voltage shift ($\Delta V_{fb}$), and (b) the increase of interface state density ($\Delta D_{it}$) versus the stressing time of the 950°C- and 900°C-annealing $p^+$ SAS gate capacitors and the 900°C-annealing $p^+$ ADP gate capacitor, respectively. The initial gate oxide thickness is 70 Å.

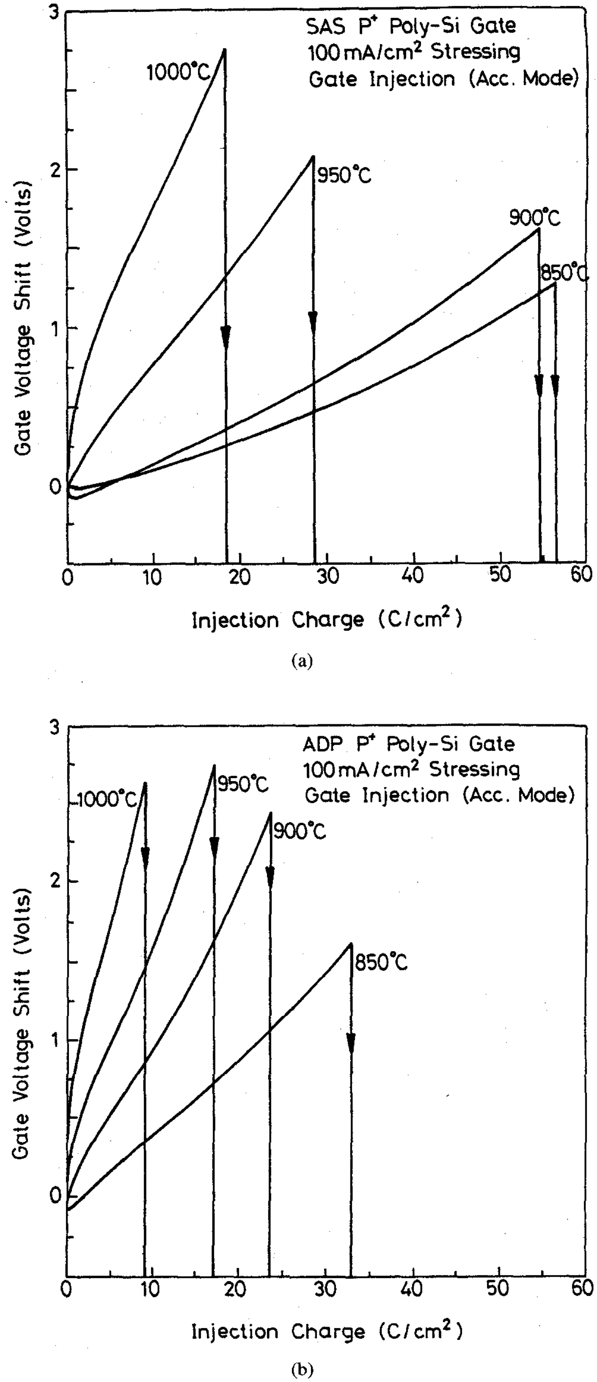



Fig. 6. The curves of gate voltage shift versus the injected charge of (a) the $p^+$ SAS gate capacitors and (b) the $p^+$ ADP gate capacitors, respectively. The initial gate oxide thickness is about 130 Å and the annealing temperature is from 850°C to 1 000°C and the injection current density is 100 mA/cm$^2$ in the positive gate bias.

increasse in flat-band voltage with the annealing temperature can be significantly reduced [5]–[9]. As shown in Fig. 2(a), the $V_{fb}$ values of the $p^+$ SAS gate capacitors annealed at 900°C, 950°C and 1 000°C are 0.73 V, 0.78 V and 1.18 V, respectively, while those of the $p^+$ ADP gate capacitors are 0.86 V, 1.46 V and 9.01 V, respectively. Also the boron penetration induced negative oxide charge generation can be reduced [7], [18], as shown in Fig. 2(b), the $Q_{eff}$ values of the $p^+$ SAS gate capacitors are $-5.3 \times 10^{10}$ C/cm$^2$, $-1.3 \times 10^{11}$ C/cm$^2$ and $-7.5 \times 10^{11}$ C/cm$^2$ for the annealing temperature of 900°C, 950°C and 1 000°C, respectively, while those of the $p^+$ ADP gate capacitors are $-2.2 \times 10^{11}$ C/cm$^2$, $-1.1 \times 10^{12}$ C/cm$^2$ and $-1.2 \times 10^{13}$ C/cm$^2$, respectively.

The dielectric breakdown field ($E_{bd}$) is determined by the flat-band voltage ($V_{fb}$) and the oxide thickness ($T_{ox}$), i.e., $E_{bd} = (V_g - V_{fb})/T_{ox}$, where $V_g$ is the applied gate voltage [19]. Thus, the boron and fluorine penetration induced the increase of the $V_{fb}$ and $T_{ox}$ values will cause a reduction in the

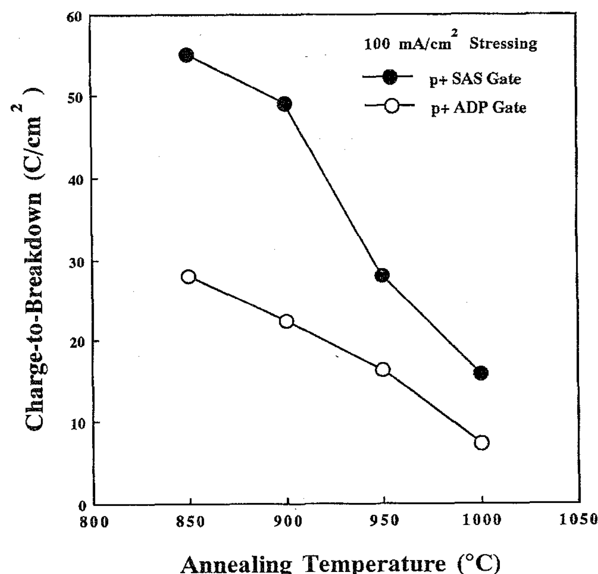



Fig. 7. The plots of the charge-to-breakdown ($Q_{\mathrm{bd}}$) versus the annealing temperature of the $p^+$ SAS and ADP gate capacitors with the initial oxide thickness of 130 Å. The stressing current density is 100 mA/cm$^2$ in the positive gate bias.

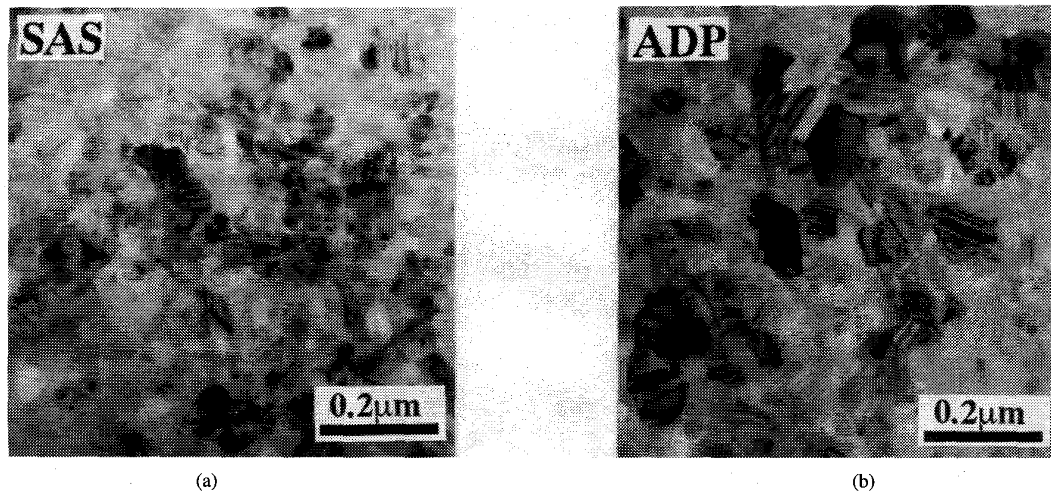
dielectric breakdown field [5], [15]. Fig. 3(a) and (b) show the plots of the $E_{\mathrm{bd}}$ value versus the annealing temperature for the $p^+$ SAS and ADP gate capacitors with the oxide thickness of 70 Å and 130 Å, respectively. It is seen that the dielectric breakdwon field of the $p^+$ SAS gate capacitors are nearly independent of the annealing temperature and the $E_{\mathrm{bd}}$ value of all capacitors are large than 15 MV/cm, which is very lose to the $E_{\mathrm{bd}}$ value of the $n^+$ poly-Si gate capacitor. However, the $p^+$ ADP gate capacitors, the $E_{\mathrm{bd}}$ value decreases drastically with the increase of the annealing temperature.

Fig. 4(a) and (b) show the quasistatic C-V (QSCV) characteristics of the 900°C annealing $p^+$ SAS and ADP gate capacitors with the oxide thickness of about 130 Å before and after a constant current stressing, respectively. Fig. 4(c) and (d) show the curves of the gate voltage shift ($\Delta V_g$) and the interface state generation ($\Delta D_{\mathrm{it}}$) versus the injection charge of the $p^+$ SAS and ADP gate capacitors, respectively. In this study, the injection current density was kept at a low level of 10 $\mu$A/cm$^2$ to reduce injection-induced electron-trap generation [20]. The area of the capacitor was $1.16 \times 10^{-3}$ cm$^2$ and electrons were injected from the Si substrate into the thin gate oxide (in the accumulation mode). It is seen that both capacitors exhibit a positive charge (hole) trapping behavior from the negative $V_{\mathrm{fb}}$ shift, as shown in Fig. 4(a) and (b), and the decrease in $\Delta V_g$, as shown in Fig. 4(c). However, the amount of trapped holes of the SAS gate capacitor is much less than that of the ADP gate capacitor. Also, the SAS gate capacitor shows a smaller interface state generation rate, as shown in Fig. 4(d). The reduction in the hole trapping rate and the interface state generation rate for the $p^+$ SAS gate capacitor is believed due to the suppression of the boron and fluorine penetration into the thin gate oxide [9], [13]. It had been reported that the boron-fluorine complex remaining within the oxide bulk would produce negative charge states at or near the Si/$SiO_2$ interface [5]–[9]. Although the $V_{\mathrm{fb}}$ values of the 900°C-annealing $p^+$ SAS and ADP gate capacitors derived form C-V curve are 0.73 and 0.86 V, respectively, which indicate that the boron penetration effect for both capacitors can be negligible [6], [11]. However, from the SIMS profiles, the amount of boron and fluorine penetration into the thin gate oxide of the ADP gate capacitor is much larger than that of the SAS gate capacitor. This is the reason that the SAS gate capacitor has a smaller hole trapping rate and interface generation rate than does the ADP gate capacitor [5]–[8]. For the capacitor with an ultra-thin oxide of 70 Å, the boron and fluorine penetration induced hole trapping and interface state generation rate become much more serious. As shown in Fig. 5(a) and (b), the hole trapping rate (negative increase in $V_{\mathrm{fb}}$ value) and the interface state generation rate of the 900°C-annealing $p^+$ ADP gate capacitor under a constant current of 10 $\mu$A/cm$^2$ stressing are much larger than those of the 900°C- and 950°C-annealing $p^+$ SAS gate capacitors. This is believed to be due to much larger amount of boron and fluorine penetration into the ultra-thin oxide of the 900°C-annealing $p^+$ ADP gate capacitor than into the ultra-thin oxide of the 900°C- or even 950°C-annealing $p^+$ SAS gate capacitors [13].

In addition to the suppression of the hole trapping and the interface state generation, the electron trapping rate and the charge-to-breakdown ($Q_{\mathrm{bd}}$) are also significantly improved for the $p^+$ SAS gate structure. Fig. 6(a) and (b) show the curves of the gate voltage shift versus the injection charge of the $p^+$ SAS and ADP gate capacitors with the oxide thickness of 130 Å annealed at the temperature from 850°C to 1 000°C, respectively. Fig. 7 shows the plots of the mean value of $Q_{\mathrm{bd}}$ (more than ten devices) versus the annealing temperature of the $p^+$ SAS and ADP gate capacitors with the oxide thinkness of 130 Å. The stressing current density was 100 mA/cm$^2$ and the injection polarity was in the accumulation mode. It is seen that the electron trapping rate increases with the annealing temperature for both type $p^+$ poly-Si gate capacitors, while the $Q_{\mathrm{bd}}$ values decrease with the increase of the annealing temperature. This is due to the higher temperature annealing resulting in a larger amount of boron and fluorine penetration through the thin gate oxide into the Si substrate [5], [6], [9]. Nevertheless, at the same annealing temperature, the gate voltage shift of the $p^+$ SAS gate capacitors are much less than that of the $p^+$ ADP gate capacitors. Also, the $Q_{\mathrm{bd}}$ value of the $p^+$ SAS gate capacitors are about a factor of two larger than that of the $p^+$ ADP gate capacitors. It is interesting to note that the 950°C-annealing $p^+$ SAS gate capacitor has a less electron trapping rate and a larger $Q_{\mathrm{bd}}$ value than the 900°C-annealing $p^+$ ADP gate capacitor. This is due to the fact that the amount of boron and fluorine penetration into the thin gate oxide of the 950°C-annealing $p^+$ SAS gate capacitor is still less than that of 900°C-annealing $p^+$ ADP gate capacitor (see [14]).

## IV. Physical Model

Since the stacked-Si layer boundaries limited the growth of the grain size [21], the final grain size of the SAS gate is smaller than that of the ADP gate, as shown in Fig. 8(a) and




(a) (b)

Fig. 8. The plan-view of the TEM micrographs of (a) the $p^+$ SAS gate structure, and (b) the $p^+$ ADP gate structure, respectively. The dopant driven-in was performed at 1 000°C. It is seen that the grain size of the SAS gate is smaller than that of the ADP gate.

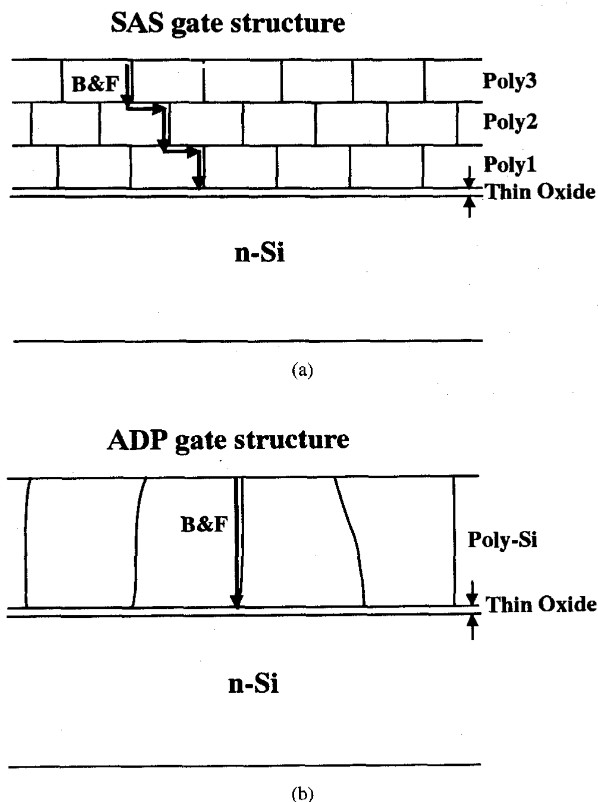



Fig. 9. The physical model of boron and fluorine diffusion in (a) the SAS gate, and (b) the ADP gate, respectively. Assume the grain structure is block-like.

(b). Hence, for the $p^+$ SAS gate structure, the suppression of the boron and fluorine penetration into the thin gate oxide was not caused by the grain size effect [9]. As mentioned above, for the $p^+$ SAS gate capacitors, due to the dopant segregation at the stacked-Si layer boundaries, the amount of boron and fluorine available for diffusion to the poly-Si/$SiO_2$ interface are less than that of the $p^+$ ADP gate capacitors. Moreover, due to the stacked-Si structure, the total path for boron and fluorine diffusion to the poly-Si/$SiO_2$ interface becomes longer than the ADP gate, as shown in Fig. 9 (assume the grain structure is block-like). Thus, for the SAS gate structure, the suppression of boron and fluorine penetration through the thin gate oxide into the Si substrate is believed to be due to the dopant segregation at the the stacked-Si layer boundaries and the longer path for dopant diffusion to the poly-Si/$SiO_2$ interface. It is worthy noting that due to the suppression of boron and fluorine penetration through the thin gate oxide into the Si substrate, the Si/$SiO_2$ interface of the $p^+$ SAS gate structure is atomically flat, while that of the $p^+$ ADP gate structure is relatively rough [14], [22].

## V. Conclusion

In this paper, we propose a stacked-amorphous-silicon (SAS) structure as the gate material for pMOSFET to suppress the boron penetration effect. Although the grain size of the SAS film is smaller than that of the ADP film, the boron and fluorine penetration-induced device degradation can be reduced even though the annealing temperature is higher than 950°C. The amount of the boron and fluorine penetration through the thin gate oxide into the Si substrate of the $p^+$ SAS gate capacitor is less than that of the $p^+$ ADP gate capacitor, even the annealing temperature of the $p^+$ SAS gate capacitor is higher. Besides, the mobile ion ($Na^+$) contamination can be reduced by using the SAS gate structure. Since the suppression of boron and fluorine penetration into the thin gate oxide, the $p^+$ SAS gate capacitor has a smaller flat-band voltage shift, a less charge trapping rate, a less interface state generation rate, and a larger $Q_{bd}$ value than does the $p^+$ ADP gate capacitor. Also the Si/$SiO_2$ interface of the $p^+$ SAS gate capacitor is much smoother than that of the $p^+$ SAS gate capacitor [14], [21]. The mechanism of the suppression of boron and fluorine penetration effect by using the SAS gate structure is believed to be due to the dopant segregation at the stacked-Si

layer boundaries and a longer path for dopant diffusion to the poly-Si/$SiO_2$ interface.

## Acknowledgment

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