New 4-Bit Transient-to-Digital Converter for System-Level ESD Protection in Display Panels

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***Abstract*—A new on-chip 4-bit transient-to-digital converter for system-level electrostatic discharge (ESD) protection design is proposed. The proposed converter is designed to detect ESD-induced transient disturbances and transfer different ESD voltages into digital codes under system-level ESD tests. The experimental results in a 0.13-μm CMOS integrated circuit with 1.8-V devices have confirmed the detection function and digital output codes. The proposed on-chip transient-to-digital converter can be codesigned with firmware operations to effectively enhance immunity of display systems against system-level ESD stresses.**

***Index Terms*—Converter, electromagnetic compatibility, electrostatic discharge (ESD), system-level ESD test, transient detection circuit.**

I. Introduction

RELIABILITY issues have been more important for industrial electronic products equipped with CMOS integrated circuits (ICs) [1]–[5]. For example, electrostatic discharge (ESD) stresses can cause serious latchup failure in the silicon chip inside a microelectronic system [6]. These reliability events result from not only the progress of more integrated functions into a single chip but also from the strict requirements of reliability standards, such as the system-level ESD test of IEC 61000-4-2 [7]. Furthermore, for industrial microelectronic products, such as uninterruptible power supply, Global Positioning System, motor drives, and robot system, CMOS ICs are widely used, and the operating environment could be with more electrical transient disturbance than before [8]–[12]. It has been investigated that CMOS ICs inside the industrial products are very susceptible to electrical transient disturbance, even though they have passed the component-level ESD specifications, such as human body model of ± 2 kV and machine model of ± 200 V [13]–[23].

Fig. 1 shows the measurement setup of the system-level ESD test with the indirect contact-discharge test mode [7]. When the ESD gun zaps to the horizontal coupling plane (HCP), all the CMOS ICs inside the equipment under test (EUT) would be disturbed due to ESD-coupled energy. Under normal operation, the display panel can continuously show the correct information composed of red, green, and blue colors, as shown in Fig. 2(a). With electrical transient disturbance coupling from the system-level ESD test, the display panel is locked in a frozen state, as shown in Fig. 2(b). Typical on-chip ESD protection circuits in CMOS ICs can protect the internal circuits against component-level ESD damage [24], but they cannot release the upset or locked states generated by the system-level ESD tests.

The traditional solution is to add some discrete board-level components into the printed circuit board (PCB) to decouple, bypass, or absorb the electrical transient energy [25]–[27]. However, the additional components substantially increase the total cost of industrial products. Therefore, the chip-level solutions to meet high immunity specification without the additional discrete components on PCB are highly desired by the IC industry [28]–[31].

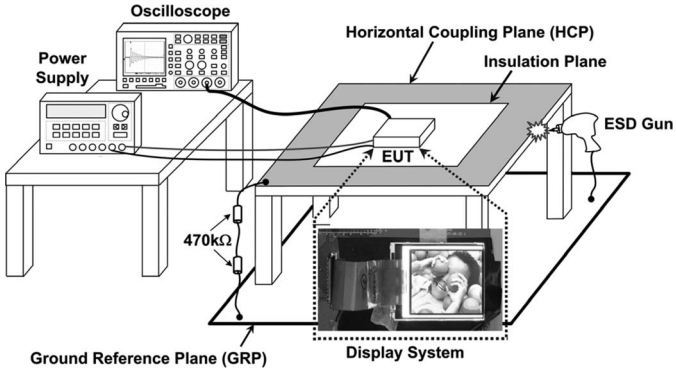

Fig. 1. System-level ESD test on a display system with indirect contact-discharge test mode.

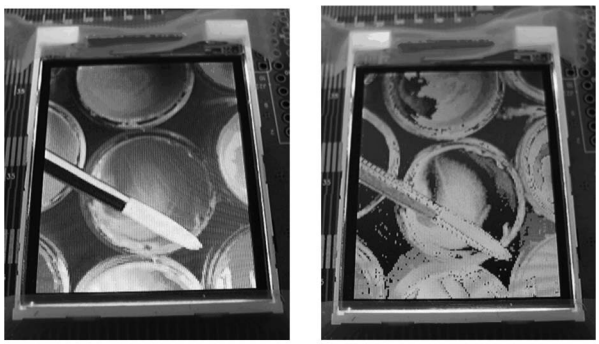

Fig. 2. Measurement results of a display system under (a) normal operation and (b) system-level ESD test.

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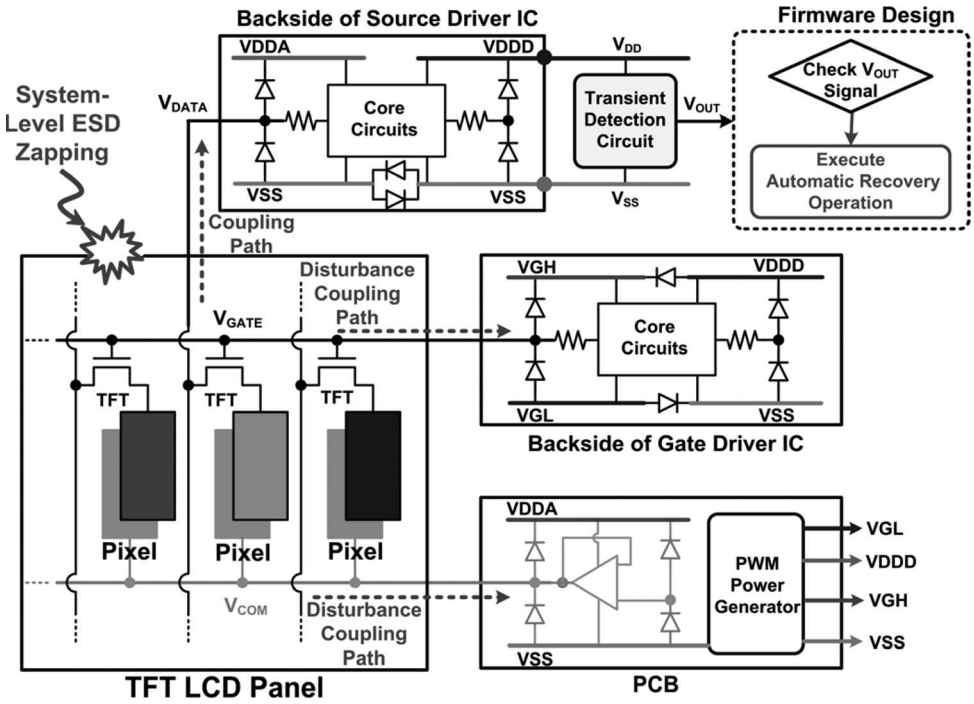


Fig. 3. Hardware/firmware system codesign with transient detection circuit in display panel product.

In this paper, a new on-chip 4-bit transient-to-digital converter composed of capacitor-resistor (CR)-based transient detection circuits is proposed to detect the fast electrical transients and provide output digital codes under system-level ESD stresses. The new proposed converter is designed to reduce the large decoupling capacitor used in a noise filter network. Experimental results in a 0.13-μm CMOS process with 1.8-V devices have verified that the output digital codes can correctly correspond with the magnitude of fast electrical transients under system-level ESD tests.

II. Display Panel Protection Design Against System-Level ESD Stress

It had been proven that the hardware/firmware codesign can effectively improve the robustness of the industrial products against electrical transient disturbance. For a display system protection design with a thin-film transistor liquid crystal display panel, multiple power systems are needed for electrical display functions, as shown in Fig. 3. For example, in the backside of a source driver IC, the analog power line (VDDA) is used for digital-to-analog converter circuit, and the digital power line (VDDD) is used for shifter register to store display signals. A transient detection circuit, designed for detecting and memorizing the occurrence of ESD-induced transient disturbance, can connect with a 1.8-V VDDD power line to implement the hardware/firmware protection design in a display system. The detection results from the detection circuit can be temporarily stored as a system recovery index for firmware check, as shown in Fig. 3. In the beginning, the output $(V_{\rm OUT})$ state of the detection circuit is initially reset to logic "1." When the electrical transients happen, the detection circuit can detect the occurrence of system-level ESD-induced

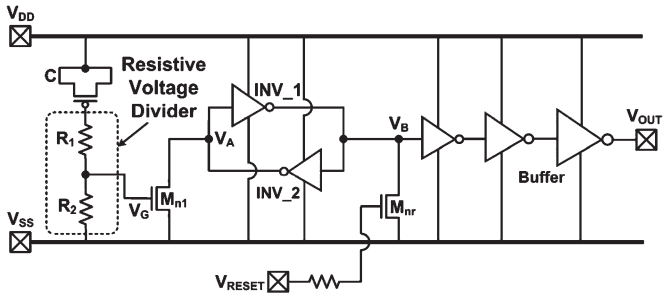


Fig. 4. New proposed on-chip CR-based transient detection circuit.

transient disturbance and transit the output state $(V_{\rm OUT})$ to logic "0." At this moment, the firmware index is also changed to logic "0" to initiate automatic recovery operation to restore the microelectronic display system to a desired stable state as soon as possible. After the automatic recovery operation, the output of the detection circuit and the system recovery index are reset to logic "1" again for detecting the next ESD-induced electrical transient disturbance events.

III. New On-Chip CR-Based Transient Detection Circuit

A. Circuit Implementation

Fig. 4 shows the new proposed on-chip CR-based ESD detection circuit. The CR-based circuit structure is designed to realize the transient detection function. The NMOS $(M_{\rm nr})$ is used to provide the initial reset function to set the initial voltages at node $V_{\rm OUT}$ and node V_A as 1.8 V with the $V_{\rm DD}$ of 1.8 V in a 0.13-μm CMOS process. In Fig. 4, node V_G is biased at $V_{\rm SS}$ during the normal operating condition. Under the system-level ESD stress with an overshooting ESD voltage, node V_G

will be coupled with a positive voltage. Then, the NMOS device $(M_{\rm n1})$ can be turned on by the overshooting ESD voltage to pull down the voltage level at node V_A. Therefore, the logic level stored at node V_A can be changed from logic "1" to logic "0" to memorize the ESD-induced transient disturbance. With the buffer inverters, the output voltage is finally changed from 1.8 to 0 V to detect the occurrence of system-level ESD events. Furthermore, by different combination design of R_1 and R_2, the ESD energy coupled to node V_G can be adjusted. Therefore, the minimum ESD voltage to cause transition at the output $(V_{\rm OUT})$ of the proposed detection circuit can be designed by this resistive voltage divider technique.

B. HSPICE Simulation

It has been investigated that the underdamped sinusoidal voltage waveform has been observed on the power line of CMOS IC during the system-level ESD stress. Therefore, a sinusoidal time-dependent voltage source given by

$$V(t) = V_0 + V_a \cdot \sin\left(2\pi f(t - t_d)\right) \cdot \exp\left(-(t - t_d)D_a\right) \quad (1)$$

is used to simulate the ESD-induced transient disturbance coupled on the power lines of the proposed detection circuit. With the proper parameters (including the applied voltage amplitude V_a, initial dc voltage V_0, damping factor $D_a = 2 \times 10^7$ s^{-1}, frequency $f = 50$ MHz, and time delay $t_d = 300$ ns), the underdamped sinusoidal voltage can be used to simulate the electrical transient waveforms under system-level ESD tests.

The simulated $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the proposed detection circuit with a positive-going (negative-going) underdamped sinusoidal voltage on $V_{\rm DD}$ line are shown in Fig. 5(a) and (b). The positive-going underdamped sinusoidal voltage with an amplitude of $+3$ V (-3 V) is used to simulate the coupling ESD transient noise under the system-level ESD test. From the simulated waveforms, $V_{\rm DD}$ begins to increase (decrease) rapidly from 1.8 V. $V_{\rm OUT}$ also acts with a positive-going (negative-going) underdamped sinusoidal voltage waveform during the simulated system-level ESD events on $V_{\rm DD}$ line. After this disturbance duration, $V_{\rm DD}$ returns to its normal voltage level of 1.8 V, and the output state $(V_{\rm OUT})$ of the detection circuit is changed from 1.8 to 0 V, as shown in Fig. 5(a) and (b). As a result, the detection circuit can detect the occurrence of simulated ESD-induced electrical transients. Furthermore, with increasing resistor ratio of R_1/R_2, the ESD energy coupled to node V_G will be decreased, and the minimum ESD amplitude $(\equiv V_{a(\min)})$ to cause transition of the proposed detection circuit will be increased, as shown in Fig. 6.

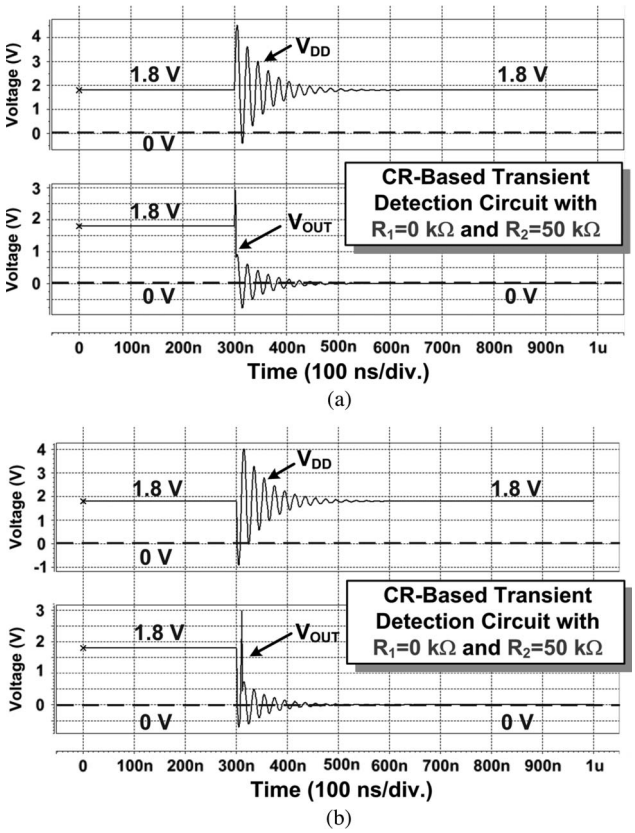


Fig. 5. Simulated $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the new proposed on-chip CR-based transient detection circuit under system-level ESD test with (a) positive-going and (b) negative-going underdamped sinusoidal voltages.

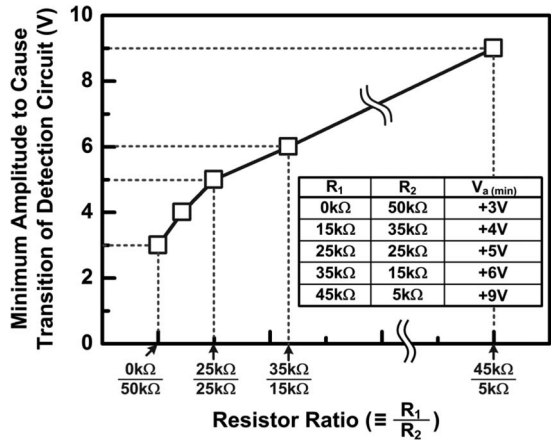


Fig. 6. Relation between resistor ratio and minimum simulated amplitude.

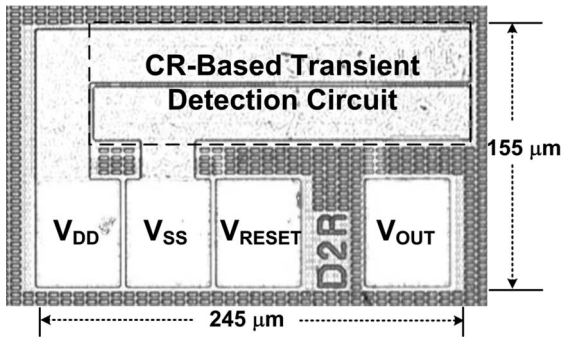


Fig. 7. Chip photo of the new proposed on-chip CR-based transient detection circuits fabricated in a 0.13-μm CMOS process.

IV. Experimental Results

The proposed detection circuit has been designed and fabricated in a 0.13-μm CMOS process. The fabricated chip for transient disturbance tests is shown in Fig. 7. The silicon area of the proposed on-chip detection circuit is $245\ \mu{\rm m} \times 155\ \mu{\rm m}$.

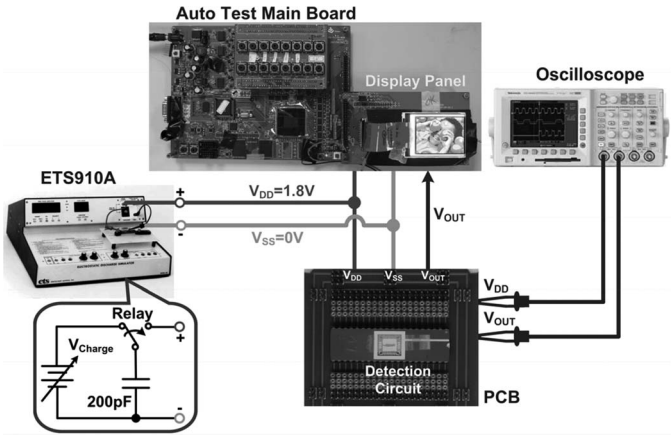


Fig. 8. Measurement setup for TLU test on display panel.

A. TLU Test

Fig. 8 shows such a component-level transient-induced latchup (TLU) measurement setup on a display system. An ESD simulator (ETS910A) is used to generate the TLU-triggering source, $V_{\rm Charge}$, to produce an underdamped sinusoidal voltage stimulus. Through applying a positive (negative) charged voltage $V_{\rm Charge}$, the intended positive-going (negative-going) underdamped sinusoidal voltage can be generated similar to transient disturbance generated from the ESD gun. In the equivalent circuit of a machine-mode module shown in the inset of Fig. 8, a charging capacitance of 200 pF is used to store charges for the TLU-triggering source, $V_{\rm Charge}$, and then, these stored charges are discharged to a 1.8-V power line of the display system through the relay. The intended underdamped sinusoidal voltage can be produced to simulate the transient voltage on the power pins of CMOS ICs under the system-level ESD test.

Fig. 9(a) and (b) shows the measured $V_{\rm DD}$ and $V_{\rm OUT}$ transient responses of the proposed detection circuit under the TLU test with $V_{\rm Charge}$ of $+200$ and -200 V, respectively. As shown in Fig. 9(a), under the TLU test with $V_{\rm Charge}$ of $+200$ V, $V_{\rm DD}$ begins to increase rapidly from 1.8 V with a positive-going underdamped sinusoidal voltage waveform. During the TLU test, $V_{\rm OUT}$ is influenced simultaneously with a positive-going underdamped sinusoidal voltage coupled to $V_{\rm DD}$ power line. After the TLU test with the $V_{\rm Charge}$ of $+200$ V, the output voltage $(V_{\rm OUT})$ of the proposed detection circuit can transit from 1.8 to 0 V. In Fig. 9(b), under the TLU test with $V_{\rm Charge}$ of -200 V, $V_{\rm DD}$ begins to decrease rapidly from 1.8 V with a negative-going underdamped sinusoidal voltage waveform. During the TLU test, $V_{\rm OUT}$ is influenced simultaneously with a negative-going underdamped sinusoidal voltage coupled to $V_{\rm DD}$ power line. After the TLU test with the $V_{\rm Charge}$ of -200 V, the output voltage $(V_{\rm OUT})$ of the proposed detection circuit can transit from 1.8 to 0 V.

From the TLU test results, the proposed detection circuit can successfully memorize the occurrence of electrical transients. With positive or negative underdamped sinusoidal voltages coupled to $V_{\rm DD}$ power line, the output voltages $(V_{\rm OUT})$ of the proposed detection circuit can both change from logic"1" to logic"0" after TLU tests.

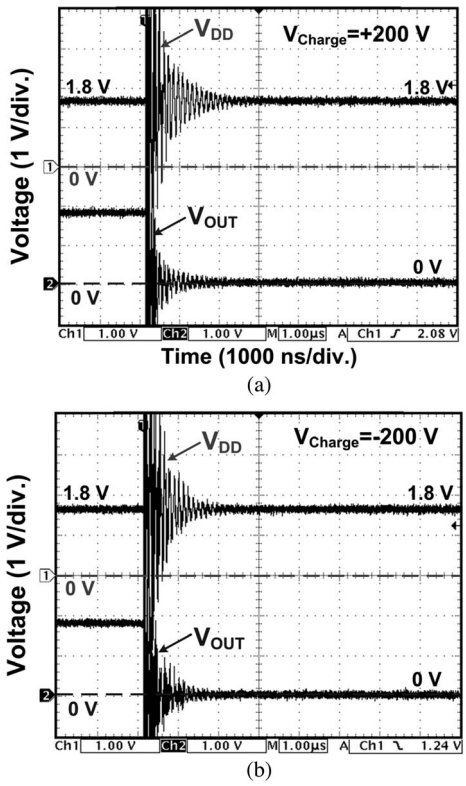


Fig. 9. Measured $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms on the new proposed CR-based transient detection circuit under TLU tests with $V_{\rm Charge}$ of (a) $+200$ and (b) -200 V.

B. System-Level ESD Test

In IEC 61000-4-2, two test modes have been specified, which are the air-discharge test mode and the contact-discharge test mode [7]. In the case of air-discharge test mode, the round discharge tip should be approached as fast as possible to touch the EUT. The air discharge is actuated by a spark to the EUT, and the ESD energy holding time is at least 5 s. In the case of contact-discharge test mode, the sharp discharge tip is used to simulate the mechanical ESD damage on the EUT. The contact discharge is applied to the conductive surfaces of the EUT (direct application) or to the horizontal or vertical coupling planes (indirect application). The measurement setup of the system-level ESD test consists of a wooden table on the grounded reference plane (GRP). In addition, an insulating plane of 0.5-mm thickness is used to separate the EUT/cables from the HCP. The HCP is connected to the GRP with two 470-kΩ resistors in series.

Fig. 10 shows the measurement setup of the system-level ESD test standard with an air-discharge test mode in a display system. When the ESD gun is approaching the EUT, the electromagnetic interference coming from the ESD gun will be coupled into all CMOS ICs inside EUT. The power lines of CMOS ICs inside EUT will be disturbed by the ESD-coupled energy.

With such a measurement setup shown in Fig. 10, the circuit function of the proposed detection circuit after system-level ESD tests can be evaluated. Before each system-level ESD test, the initial output voltage $(V_{\rm OUT})$ of the proposed

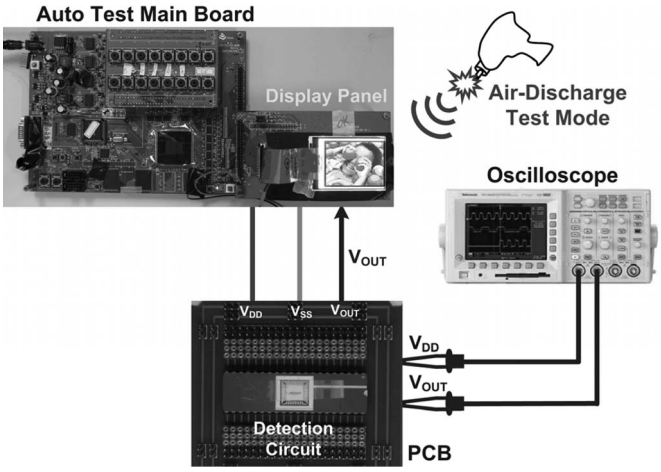


Fig. 10. Measurement setup for system-level ESD test with air-discharge test mode [7] to evaluate the detection function of the fabricated on-chip transient detection circuit on display system application.

detection circuit is reset to 1.8 V. After each system-level ESD test, the output voltage $(V_{\rm OUT})$ level is monitored to check the final voltage level and to verify the detection function.

The measured $V_{\rm DD}$ and $V_{\rm OUT}$ waveforms of the proposed detection circuit under a system-level ESD test with an ESD voltage of $+4$ kV are shown in Fig. 11(a). $V_{\rm DD}$ begins to increase rapidly from the normal voltage of $+1.8$ V. Meanwhile, $V_{\rm OUT}$ is disturbed under such a high-energy ESD stress. During the period with positive-going ESD-induced electrical transient disturbance, $V_{\rm DD}$ and $V_{\rm OUT}$ are influenced simultaneously. Finally, the output voltage $(V_{\rm OUT})$ of the proposed detection circuit transits from 1.8 to 0 V. Therefore, the proposed detection circuit can sense the positive-going electrical transient on the power line and memorize the occurrence of the system-level ESD event.

The measured $V_{\rm DD}$ and $V_{\rm OUT}$ transient voltage waveforms of the proposed detection circuit with the ESD voltage of -4 kV under a system-level ESD test are shown in Fig. 11(b). During the negative-going ESD-induced electrical transient disturbance on $V_{\rm DD}$ power line, $V_{\rm OUT}$ is disturbed simultaneously. After the system-level ESD test with the ESD voltage of -4 kV, $V_{\rm DD}$ returns to the operation voltage level of 1.8 V, and $V_{\rm OUT}$ transits from logic"1" to logic"0." The detection function of the proposed on-chip detection circuit after the system-level ESD tests has been verified by both the experimental results in silicon chip and HSPICE simulation.

For advanced system-level ESD verification on industrial display products, there are nine zapping locations defined on the display panels with air-discharge test mode, as shown in Fig. 12.

In the IEC 61000-4-2 standard, for microelectronic products after system-level ESD zapping, class A, class B, and class C denote normal performance, automatic recovery, and manual recovery, respectively. By using the output digital codes as the firmware index, the display panel can automatically recover all electrical functions to successfully release the locked or frozen states caused by system-level ESD transient disturbance. Table I shows the comparison among the measured results between the display panel without and with system hardware/firmware codesign via the proposed detection circuit. The display system criterion can be improved from "class C" to "class B" to meet the typical specifications of commercial microelectronic products.

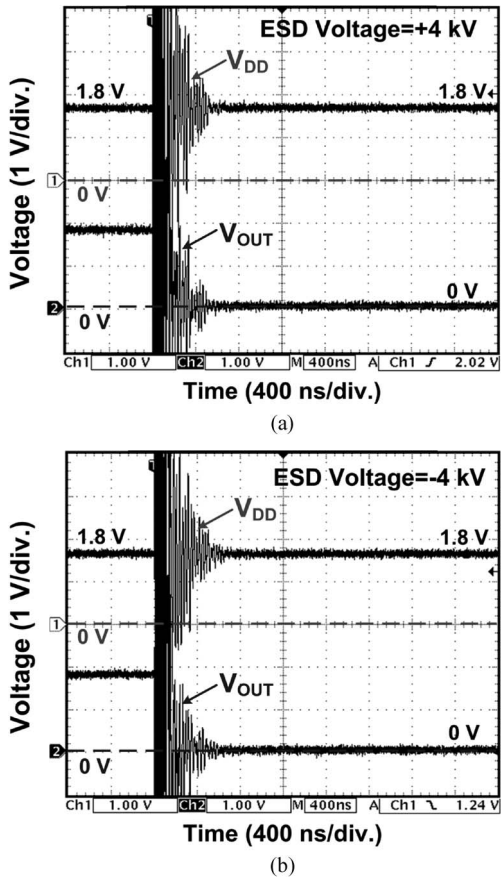


Fig. 11. Measured $V_{\rm DD}$ and $V_{\rm OUT}$ transient voltage waveforms of the new proposed detection circuit under system-level ESD tests with ESD voltages of (a) $+4$ and (b) -4 kV.

Fig. 12. Test point definition on display panel under system-level ESD tests with air-discharge test mode.

V. Transient-to-Digital Converter

A. Circuit Implementation

It has been investigated that noise filter networks can reduce the susceptibility of CMOS ICs against electrical transients by

TABLE I
MEASURED RESULTS OF DISPLAY PANEL WITHOUT AND WITH SYSTEM HARDWARE/FIRMWARE CODESIGN

Zapping Location Definition under Air-Discharge Test Mode	ESD Voltage = +4 kV		ESD Voltage = -4 kV	
	W/o System Hardware/Firmware Co-Design	With System Hardware/Firmware Co-Design	W/o System Hardware/Firmware Co-Design	With System Hardware/Firmware Co-Design
#1	Class C	Class B	Class C	Class B
#2	Class C	Class B	Class B	Class B
#3	Class C	Class B	Class C	Class B
#4	Class C	Class B	Class C	Class B
#5	Class A	Class A	Class B	Class B
#6	Class C	Class B	Class C	Class B
#7	Class C	Class B	Class C	Class B
#8	Class C	Class B	Class C	Class B
#9	Class C	Class B	Class C	Class B

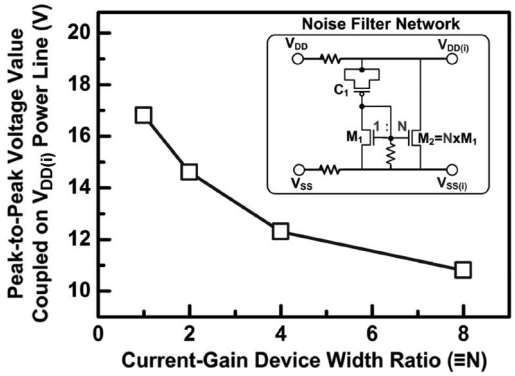


Fig. 13. Relation between current-gain device width ratio and the simulated peak-to-peak voltage value of degraded transient disturbance.

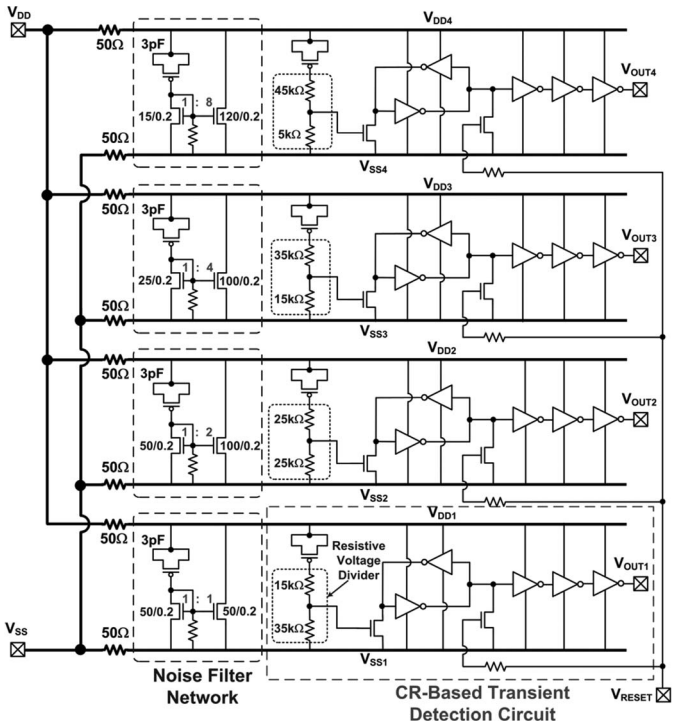


Fig. 14. Proposed 4-bit transient-to-digital converter realized with four CR-based transient detection circuits and four different noise filter networks.

decoupling or bypassing noise energy. In the previous design, a 10-pF on-chip decoupling capacitor is used in a noise filter network [30]. In this paper, a 3-pF on-chip capacitor (C_1) with a current mirror is adopted to replace the large decoupling capacitor between power lines, as shown in the inset of Fig. 13. If the current-gain device width ratio is N, the capacitor (C_1) can be scaled up by a factor of $N+1$. As shown in Fig. 13, when the underdamped sinusoidal voltage with an amplitude of $+10$ V is applied on $V_{\rm DD}$ power line, the transient disturbance coupled on internal power line $(V_{{\rm DD}(i)})$ will be decreased by increasing the current-gain device width ratio of the current mirror.

Fig. 14 shows the proposed on-chip 4-bit transient-to-digital converter consisted of four CR-based transient detection circuits and four different noise filter networks. With different device ratios in the current mirror, different ESD levels on $V_{\rm DD}$ and $V_{\rm SS}$ will reach to each transient detection circuit. For the CR-based circuit structure shown in Fig. 4, the ESD energy coupled to node V_G can be further adjusted by different resistive voltage dividers. Therefore, the minimum ESD voltage to cause transition at the output $(V_{\rm OUT})$ of the detection circuit can be designed for each stage in the transient-to-digital converter. Under the system-level ESD zapping conditions, the four transient detection circuits will have different output voltage responses.

Therefore, by combining different noise filter networks, the proposed on-chip transient-to-digital converter can be designed to detect different ESD voltage levels and transfer output voltages into digital codes under system-level ESD tests.

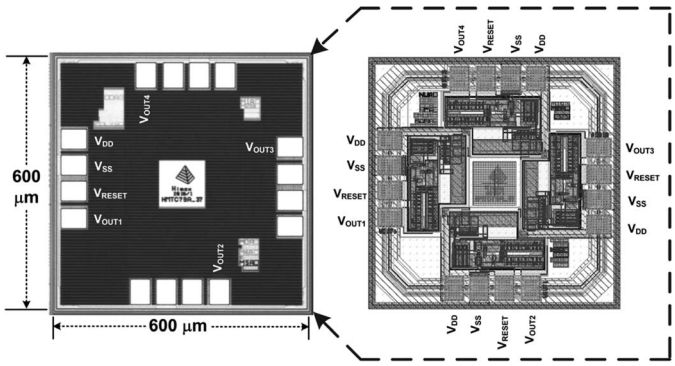


Fig. 15. Chip photo and layout of the proposed 4-bit transient-to-digital converter realized in a 0.13-μm CMOS process.

B. Experimental Results

The layout of the proposed on-chip 4-bit transient-to-digital converter is consisted of four unit cells of the CR-based detection circuit and different noise filter networks. The silicon area is 600 μm $\times$ 600 μm, as shown in Fig. 15. The system-level ESD test standard with indirect contact-discharge test mode is used to verify the output digital codes.

The measured $V_{\rm OUT1}$, $V_{\rm OUT2}$, $V_{\rm OUT3}$, and $V_{\rm OUT4}$ waveforms of the proposed 4-bit transient-to-digital converter under a system-level ESD test with an ESD voltage of $+0.7$ kV zapping on the HCP are shown in Fig. 16(a). During the fast transient of ESD stress, $V_{\rm OUT1}$, $V_{\rm OUT2}$, $V_{\rm OUT3}$, and $V_{\rm OUT4}$ are disturbed simultaneously during $V_{\rm DD}/V_{\rm SS}$ electrical disturbance. Finally, when $V_{\rm DD}$ returns to the normal operation voltage level of 1.8 V, $V_{\rm OUT1}$ will be changed from 1.8 to 0 V, and $V_{\rm OUT2}$, $V_{\rm OUT3}$, and $V_{\rm OUT4}$ are still kept at 1.8 V. Therefore, the detection output voltages can transfer the $+0.7$-kV ESD voltage level into a digital code of "1110."

Similarly, under a system-level ESD test with ESD voltages of $+0.8$, $+1.0$, and $+1.3$ kV, the transferred digital codes generated by the proposed 4-bit transient-to-digital converter are "1100," "1000," and "0000," as shown in Fig. 16(b)–(d), respectively. Therefore, the proposed on-chip converter can successfully transfer different positive ESD voltage levels into different digital codes. The digital code goes from "1110" to "0000" as the magnitude of positive ESD voltage increases from $+0.7$ to $+1.3$ kV.

The measured $V_{\rm OUT1}$, $V_{\rm OUT2}$, $V_{\rm OUT3}$, and $V_{\rm OUT4}$ voltage waveforms of the proposed transient-to-digital converter under a system-level ESD test with an ESD voltage of -0.2 kV are shown in Fig. 17(a). During the fast transient of ESD stress, all transient detection circuits are affected by ESD-induced transient disturbance coupled on $V_{\rm DD}$ line. Finally, $V_{\rm OUT1}$ transits from logic "1" to logic "0," while $V_{\rm OUT2}$, $V_{\rm OUT3}$, and $V_{\rm OUT4}$ are still kept at logic "1" states. Therefore, under the system-level ESD test with the ESD voltage of -0.2 kV, the output responses of the proposed 4-bit converter can be transferred into a digital code of "1110."

Similarly, under a system-level ESD test with ESD voltages of -0.3, -0.6, and -1.1 kV, the transferred digital codes generated by proposed 4-bit transient-to-digital converter are "1100," "1000," and "0000," as shown in Fig. 17(b)–(d), respectively.

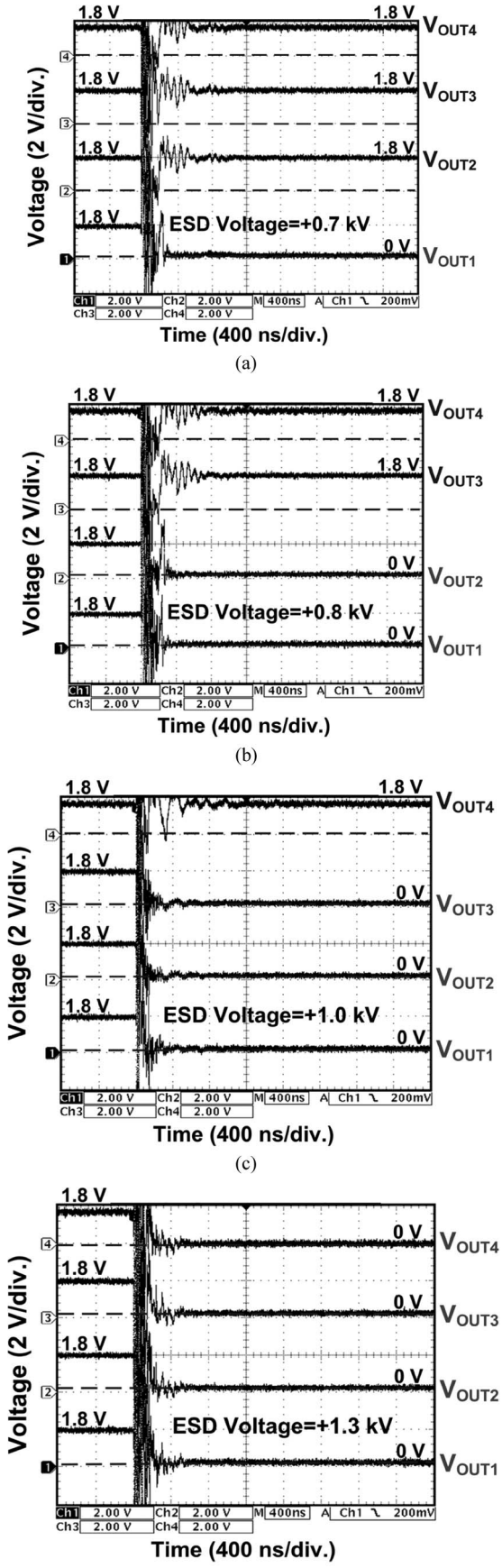
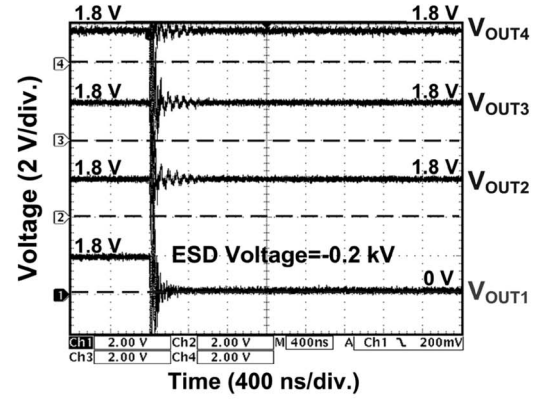
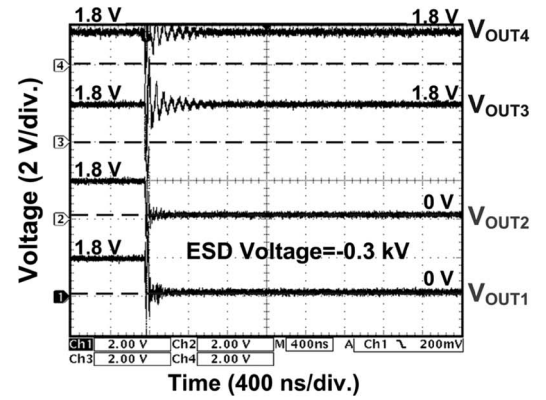


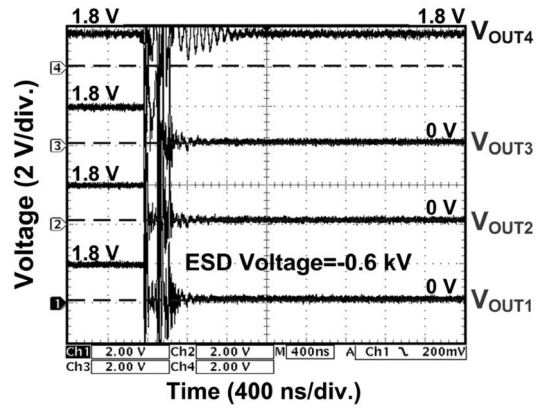
Fig. 16. Measured $V_{\rm OUT1}$, $V_{\rm OUT2}$, $V_{\rm OUT3}$, and $V_{\rm OUT4}$ transient voltage waveforms under system-level ESD test with ESD voltages of (a) $+0.7$, (a) $+0.8$, (a) $+1.0$, and (d) $+1.3$ kV zapping on the HCP.



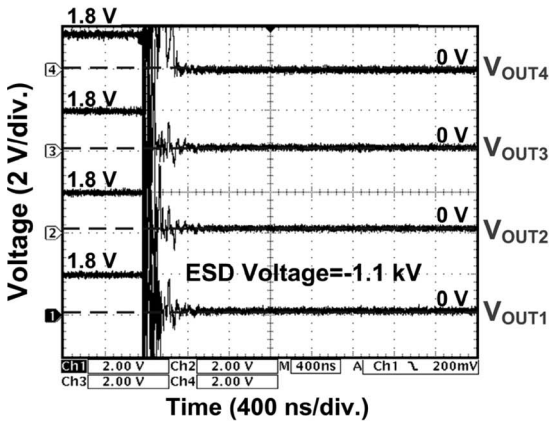
(a)



(b)



(c)



(d)

Fig. 17. Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms under system-level ESD test with ESD voltages of (a) -0.2, (a) -0.3, (a) -0.6, and (d) -1.1 kV zapping on the HCP.

TABLE II
ESD-VOLTAGE-TO-DIGITAL-CODE CHARACTERISTIC

Digital Codes	Positive ESD Voltage (kV)	Negative ESD Voltage (kV)
1111	< +0.7	> -0.2
1110	+0.7 ~ +0.8	-0.2 ~ -0.3
1100	+0.8 ~ +1.0	-0.3 ~ -0.6
1000	+1.0 ~ +1.3	-0.6 ~ -1.1
0000	> +1.3	< -1.1

From the measurement results, the detection and response time of the proposed converter is about 300 ns.

Table II shows the ESD-voltage-to-digital-code characteristic of the proposed 4-bit transient-to-digital converter. The digital code goes from "1110" to "0000" as the magnitude of ESD voltage increases from $+0.7$ to $+1.3$ kV and from -0.2 to -1.1 kV. Different ESD voltage levels can successfully respond to different digital codes.

C. Hardware/Firmware Codesign

To perform the hardware/firmware codesign, the digital codes from the transient-to-digital converter can be temporarily stored as a system recovery index for firmware check. The display system can be programmed to execute different recovery procedures according to different digital codes with the consideration of system recovery time and energy saving.

In the beginning, the output digital code is set as "1111." When the electrical transients happen, the transient-to-digital converter can detect the occurrence of system-level electrical transient disturbance and transfer the ESD voltage levels into digital codes. At this moment, the firmware index is also changed to initiate a system recovery procedure to restore the system to a known stable state as soon as possible. According to the different digital codes, the firmware can program the corresponding system recovery procedures. For example, under a system-level ESD test with low ESD voltage zapping, the transferred digital code is "1110," and the firmware can execute a partial system recovery procedure in a display panel, as shown in Fig. 18(a). With high ESD zapping, the transferred digital code is "0000," and the firmware can execute a total system recovery procedure, as shown in Fig. 18(b).

For system initial state setting, a power-on reset circuit can further be designed into a hardware/firmware codesign to set the initial digital code into "1111." However, there are some mistriggered conditions for the power-on reset circuit. For example, a sudden surge can result in a very short interval between the power-down and power-up transitions. Such short interval of power-off creates difficult situations for some power-on reset circuits to work properly. Therefore, the NAND logic gate circuit can be further added into the hardware/firmware codesign flow. The V_{OUT1} signal of the transient-to-digital converter and the output signal of the power-on reset circuit are connected as the input signals of the NAND logic gate. When electrical transient disturbance happens, the system recovery procedure can be still initiated to protect microelectronic display products against the electrical transitions caused by system-level ESD events.

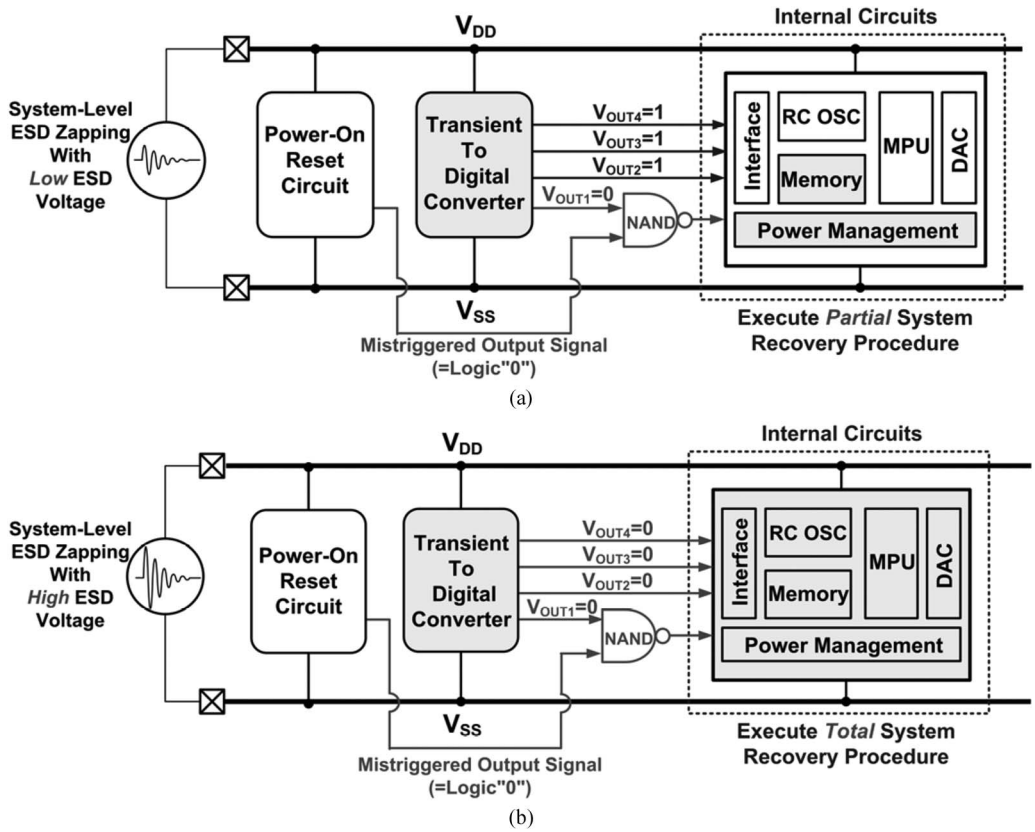


Fig. 18. Hardware/firmware operation in display panel system during (a) low and (b) high system-level ESD zapping conditions.

VI. Discussion

In this paper, the proposed transient-to-digital converter can successfully transfer different ESD voltage levels into different digital codes. The modified converter to distinguish positive and negative ESD voltages with symmetric digital codes will be further studied in our future works. Furthermore, with the on-chip ESD power clamp circuit and the CR-based transient detection circuit in a chip together, it can be further considered to share the same RC triggering circuit to provide on-chip ESD protection and transient disturbance detection.

VII. Conclusion

An on-chip transient-to-digital converter composed of four CR-based transient detection circuits and four different noise filter networks has been successfully verified in this paper. The measured results show that the output digital codes can correspond to the different magnitudes of the ESD voltages under system-level ESD tests. These output digital codes can be used as the firmware index to execute different autorecovery procedures of industrial products. The proposed circuit has been practically applied to the display panels of mobile phones to release the system locked or frozen states caused by ESD-induced transient disturbance under system-level ESD tests.

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