Pergamon

0038-1101(95)00126-3

Solid-State Electronics Vol. 39, No. 2, pp. 261–267, 1996

0038-1101/96 $15.00 + 0.00

HIGH GAIN *p–n–p* GATED LATERAL BIPOLAR ACTION IN A FULLY DEPLETED COUNTER-TYPE CHANNEL *p*-MOSFET STRUCTURE

JIH-SHIN HO, TZUEN-HSI HUANG and MING-JER CHEN

Department of Electronics Engineering & Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan 300, R.O.China

(Received 16 November 1994; in revised form 14 April 1995)

Abstract—A three-terminal *p–n–p* gated lateral bipolar transistor in a counter-type channel *p*-MOSFET structure has exhibited experimentally ideal *I–V* characteristics in low-level injection, with a peak current gain exceeding 1000. Two-dimensional device simulation and additional experiments have revealed that high current gains with ideal bipolar *I–V* characteristics can be obtained only if the counter-type channel is fully depleted. Under this condition, not only the surface emitter–base junction barrier beneath the gate is lowered, but also the holes injected from the emitter almost go through the potential valley in the channel. An analytical model and its validity range have both been established to provide understanding of such behavior, and have been supported experimentally by two-dimensional device simulation. The measured *I–V* characteristics, including high-level injection, have also been appropriately reproduced.

1. INTRODUCTION

A three-terminal gated lateral bipolar transistor in a MOSFET structure, fabricated by processes fully compatible with the existing CMOS and/or BiCMOS technologies, has recently exhibited experimentally high current gain, a high cut-off frequency, and improved low-temperature operation[1–4]. In view of these new features, utilization of a gated lateral bipolar transistor, rather than a conventional vertical bipolar transistor, is a considerably economical way to implement mixed-mode bipolar-MOS integrated circuits without increasing cost and process complexity[1–4]. An understanding of the mechanisms responsible, as well as design considerations, is very important in order to fully realize the potential of gated lateral bipolar transistors. Design guidelines for suppression of the base current reversal phenomenon in a high gain three-terminal gated lateral bipolar transistor have been established[5]. Gate assisted barrier lowering for enhanced carrier injection has been proposed to qualitatively interpret the measured high current gains[1–4]. Quantitative modeling of the *I–V* characteristics in a high gain gated lateral bipolar transistor has also been extensively studied[5–8]. The gated lateral bipolar transistors studied in [1–8] are all based on surface channel MOSFET structures. However, presently there indeed exists an n^+ polysilicon or polycide gate CMOS process for realizing a buried-channel or counter-type channel *p*-MOSFET structure, i.e., a thin *p*-type layer for the threshold voltage adjustment is introduced to the surface beneath the gate. Gated lateral bipolar action in such structures is essentially different from that in a surface channel structure, as will be demonstrated in the present work.

In this paper we report a study of a high gain *p–n–p* gated lateral bipolar transistor in a counter-type channel *p*-MOSFET structure. By means of experiment and two-dimensional device simulation, we will show that ideal bipolar *I–V* characteristics with high current gains can be obtained only if the counter-type channel is fully depleted. An analytical model and its validity range concerning the potential distribution and current conduction in the fully depleted channel is given and judged experimentally by two-dimensional device simulation. The modeling work extended to high-level injection will also be addressed.

2. EXPERIMENTAL

A gated lateral *p–n–p* bipolar transistor, based on a buried-channel or counter-type channel LDD *p*-MOSFET structure (as schematically illustrated in Fig. 1), was fabricated by an n^+ polycide gate twin-well CMOS process. In this process, the *n*-well was formed by implanting phosphorus (6.0×10^{12} cm^{-2}, 80 keV). Boron ($1.9 \times 10^{12}\,cm^{-2}$, 25 keV) was implanted to introduce the counter-type dopant (i.e., *p*-type dopant with respect to the underlying *n*-well) into the surface beneath the gate. The gate oxide was grown in dry O_2 at 920°C to a thickness of 185 Å, as determined by a *C–V* method. After gate poly-deposition and phosphorus doping, a layer of WSi_2 (2500 Å) was deposited and annealed at 920°C to form the n^+ polycide gate. BF_2 ($10^{13}\,cm^{-2}$, 50 keV) and BF_2 ($3 \times 10^{15}\,cm^{-2}$, 70 keV) were implanted to

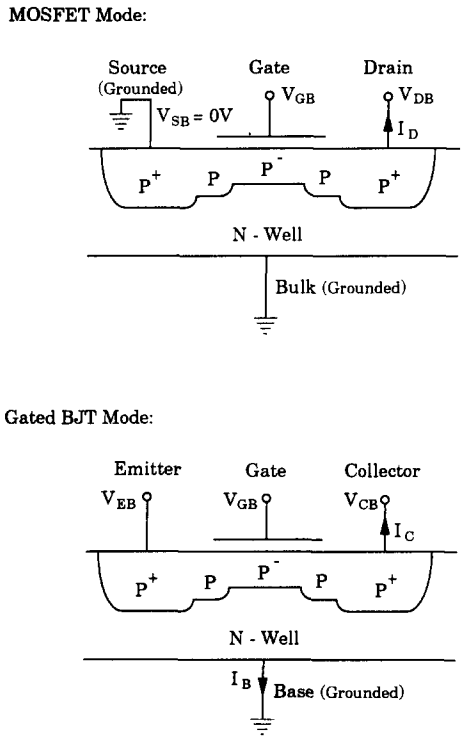


Fig. 1. Schematic cross section view of the test device operated (a) in the normal MOSFET mode, and (b) in the gated BJT mode.

form the low-doped and highly doped drain regions, respectively. The gate length and width were 1.0 and 20 μm, respectively. The flat-band voltage was about -0.1 V. The two-dimensional doping profile was obtained by performing the process simulator SUPREM-IV. The depth of the counter-type channel was 0.16 μm, with a peak concentration of 3.1×10^{16} cm^{-3} at the surface.

As demonstrated in Fig. 1, the p-channel MOSFET structure can be employed as a gated lateral p–n–p bipolar transistor by transferring the roles of the source as emitter, drain as collector, and well as

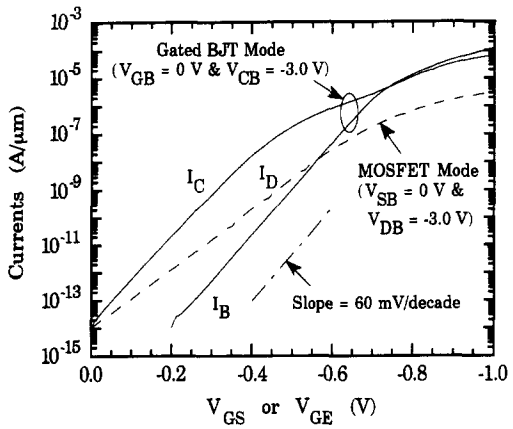


Fig. 2. Comparison of the measured I–V characteristics between the normal MOSFET and gated BJT modes.

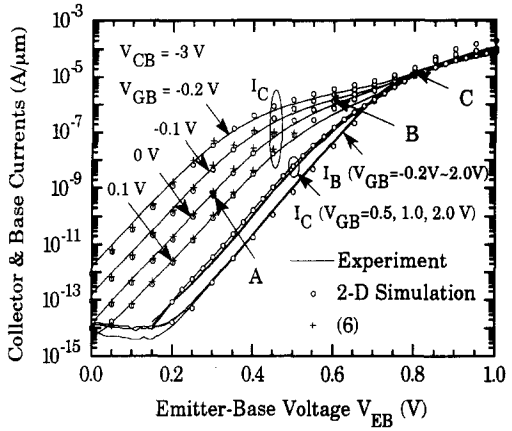


Fig. 3. Measured and simulated Gummel I–V characteristics of the p–n–p gated lateral bipolar transistor with gate-to-base voltage as parameter. Also plotted are the calculated results using eqn (6).

base. The gate and base are tied together and grounded, i.e., $V_{GB} = 0$ V, in order to implement a three-terminal gated lateral p–n–p bipolar transistor. The corresponding Gummel I–V characteristics measured in the common-base configuration for $V_{CB} = -3$ V are depicted in Fig. 2. From this figure, it can be observed that for emitter–base bias voltage V_{EB} ($= -V_{GE} = -V_{GB} + V_{EB}$ for $V_{GB} = 0$ V) less than about 0.45 V, our three-terminal gated lateral bipolar transistor exhibits ideal exponential I–V characteristics (i.e., approx. 62 mV per decade) in a wide current range of about six decades with a peak current gain exceeding 1000. This high current gain value is comparable to those reported in gated lateral bipolar transistors based on deeply depleted surface-type channel MOSFET structures[1–8]. As we further increase V_{EB} from 0.45 V, the increase in the collector current is becoming slow with respect to the base current, indicating a fast roll-off in current gain simultaneous with the ideal I–V characteristics lost. Also plotted in Fig. 2 is the drain current vs gate-to-source voltage curve measured in the normal MOSFET mode under the identical drain (collector) voltage conditions. This curve has a slope of about 89 mV per decade in low-level injection. Figure 2 clearly reveals that for $0.2\text{ V} < -V_{GS}$ (or $-V_{GE}$) < 1.0 V, the current drive capability of the gated lateral bipolar transistor is as least ten times higher than that of the MOSFET.

3. DETAILED INVESTIGATION

3.1. Additional experiments

We attribute the forward-mentioned high current gain with ideal bipolar I–V characteristics to gate-assisted barrier lowering in the fully depleted counter-type channel. This can be supported by further measuring the I–V characteristics for different gate biases, as plotted in Fig. 3. From Fig. 3, it can be observed that the base current is essentially

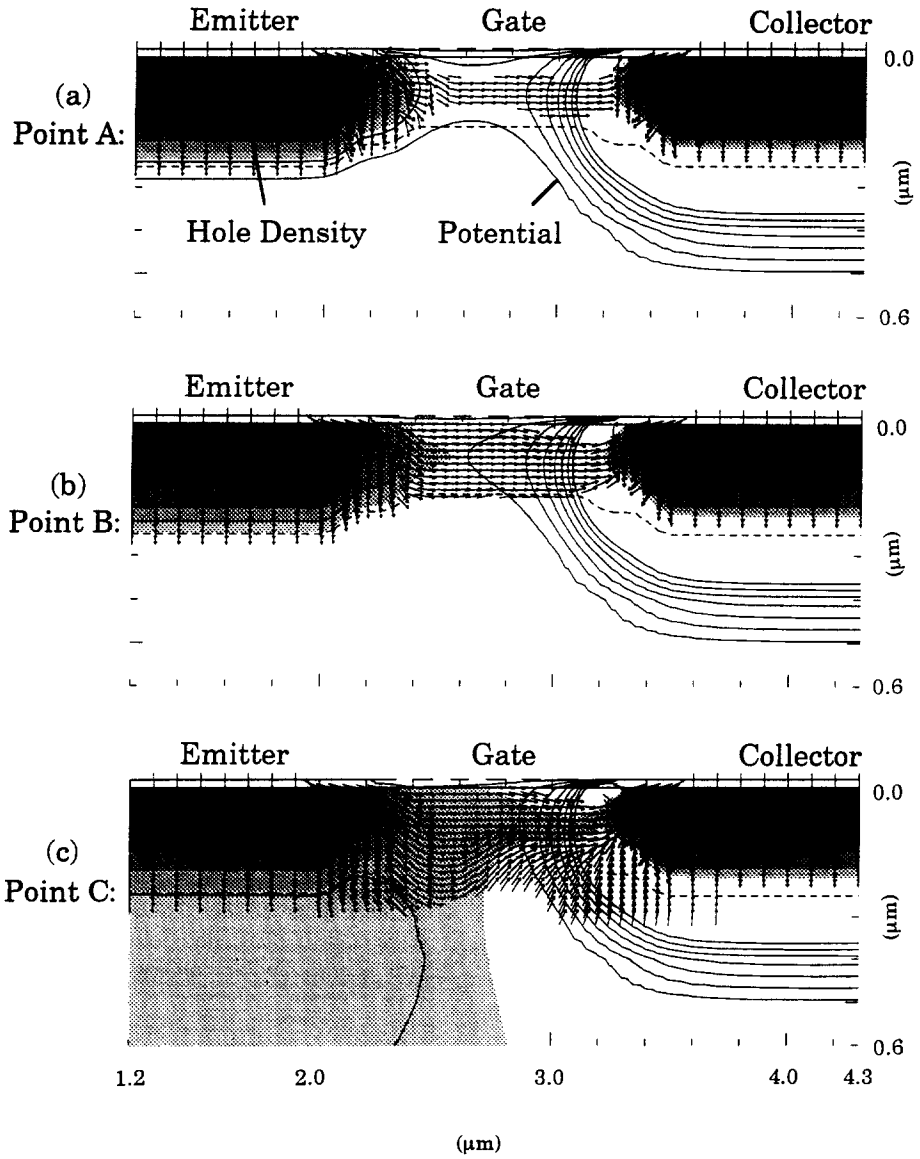


Fig. 4. Simulated hole density distribution, current flowline, and potential contour for three different operating points, as labeled on the I–V curve of $V_{GB} = 0$ V in Fig. 3.

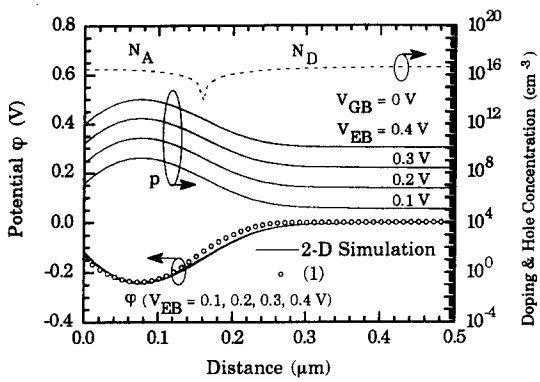
independent of gate bias, while for low level injection the collector current is a strong function of gate bias for $V_{GB} < 0.1$ V. Also it can be seen from Fig. 3 that for low current levels (i.e., below 10^{-7} A μm^{-1}) the same slope of about 62 mV per decade appears not only in the base current vs emitter–base bias characteristics but also in the collector current vs emitter–base bias characteristics. Such observations suggest that the counter-type channel should be fully depleted, so as to modulate the emitter–base junction barrier height by the gate bias applied, which locally enhances the hole injection from the emitter but does not affect the electrons injected into and recombined within the emitter. If the gate voltage increases from 0.1 V, the collector current tends to saturate and become independent of V_{GB} for $V_{GB} > 1.0$ V, as shown in Fig. 3, indicating that parasitic bipolar action dominates the collector current. It is also noted from Fig. 3 that the peak current gain is raised to a very high value of 113 600 for $V_{GB} = -0.2$ V.

3.2. *Two-dimensional simulation*

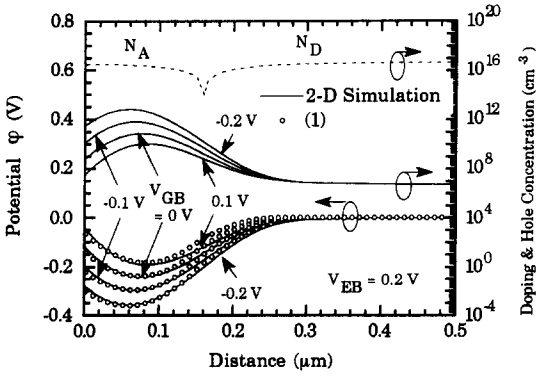
Prior to the determination of the mechanisms responsible for the measured high current gains, two-dimensional simulation work employing the program MEDICI[9] has been calibrated, i.e., the parameter values in the physical models such as concentration- and field-dependent mobilities, Shockley–Read–Hall recombination, Auger recombination, and band-gap narrowing, have been carefully adjusted to appropriately reproduce the measured I–V characteristics simultaneously in the MOSFET and gated BJT modes. As clearly demonstrated in Fig. 3, the simulation results agree reasonably with

the measurement data in the gated BJT mode. The parameter values have also been found to agree with those cited in the literature. These agreements validate the simulation process. Consequently, the mechanisms responsible can be adequately drawn from the simulated distributions of the potential and hole densities, as well as the hole current vector.

Figure 4 demonstrates the hole current flowline, potential contour, and hole density distribution for three different operating points, A, B, and C, as labeled on the simulated I–V curve of $V_{GB} = 0$ V in Fig. 3. From Fig. 4(a) we can observe that: (i) the counter-type channel is fully depleted, and (ii) the holes injected flow through the potential valley in the channel rather than along the surface. We have also found that such observations are reproducible in the whole low-level injection regime, i.e., the emitter–base voltage $V_{EB} < 0.45$ V for $V_{GB} = 0$ V. In this regime, the hole conduction is predominantly by means of diffusion. As we increase V_{EB} to point B, more of the holes appear at the surface near the emitter, constituting the drift component to the collector current, as depicted in Fig. 4(b). From Fig. 4(c), it can be seen that a further increase in V_{EB} to the high-level injection point C causes action of the pure lateral bipolar transistor far away from the surface, which contributes comparably to the collector current. The simulated potential and hole density distributions along the vertical direction in the mid-channel are also plotted in Fig. 5. From Fig. 5(a) we can observe that: (i) the potential distribution is not changed by varying V_{EB}, while the hole density increases exponentially with increasing V_{EB}; (ii) there exists a potential minimum at which a peak hole density is located; (iii) not only the whole counter-type channel but also the portion of the underlying n-well are depleted, and (iv) the hole density is several orders of magnitude smaller than the ionized dopant. Figure 5(b) reveals that a positive increase in V_{GB} moves the potential valley away from the surface (rather than toward the surface) and reduces the magnitude of the potential minimum, which in turn causes an exponential decrease in the hole density. Until $V_{GB} > 0.5$ V, the dominant component of the collector current arises from the parasitic lateral bipolar transistor itself, as revealed by the above measurement and simulation results.



(a)



(b)

Fig. 5. Simulated potential and hole density vs position from the surface in the mid-channel for (a) $V_{EB} = 0.1$ to 0.4 V at $V_{GB} = 0$ V, and (b) $V_{GB} = -0.2$ V to 0.1 V at $V_{EB} = 0.2$ V. The doping profile from process simulator and the potential profiles calculated from eqn (1) are plotted together.

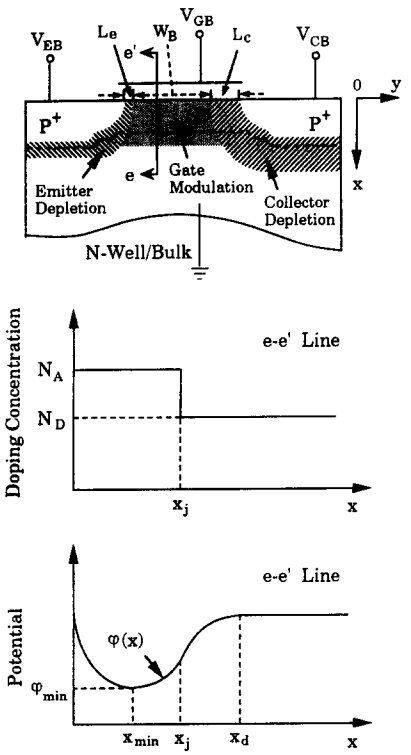


Fig. 6. The structure schematically separated into three distinct depletion regions. Along the e–e′ line, the uniform doping profile and potential distribution are schematically illustrated.

4. MODELING

According to the simulation, the depletion region beneath the gate in low level injection can be separ-

ated into three distinct sub-regions: the emitter depletion, the gate modulation, and the collector depletion, as schematically illustrated in Fig. 6. In the gate modulation region, the potential is the same along the channel and is independent of y. To derive an analytical model, we assume that the counter-type channel and underlying n-well are each uniformly doped, as demonstrated in Fig. 6. The corresponding downward potential distribution is also schematically plotted. In the gate modulation region, the potential, φ, with respect to the grounded n-well (i.e., here the electron quasi-Fermi level $\phi_{fn} = (kT/q)\ln(n_i/N_D)$, where N_D is the n-well doping concentration and n_i is the intrinsic carrier concentration) can be expressed as[10]:

$$\varphi(x) = \begin{cases} \varphi_{min} + \dfrac{qN_A}{2\epsilon_{si}}(x - x_{min})^2, & 0 \leqslant x \leqslant x_j, \\ -\dfrac{qN_D}{2\epsilon_{si}}(x_d - x)^2, & x_j \leqslant x \leqslant x_d, \\ 0, & x_d \leqslant x, \end{cases} \quad (1)$$

with

$$x_{min} = x_j - \sqrt{-\frac{2\epsilon_{si}}{qN_A}\frac{N_D}{N_D + N_A}\varphi_{min}},$$

$$x_d = x_j + \sqrt{-\frac{2\epsilon_{si}}{qN_D}\varphi(x_j)},$$

$$\varphi_{min} = -\left(1 + \frac{N_D}{N_A}\right) \times \left(\sqrt{\frac{V_2}{4} - (V_{GB} - V_{FB} - V_1)} - \frac{\sqrt{V_2}}{2}\right)^2,$$

$$V_1 = \frac{qN_A}{2\epsilon_{si}}x_j^2\left(1 + \frac{2\epsilon_{si}}{x_j C_{ox}}\right),$$

$$V_2 = \frac{2qN_D}{\epsilon_{si}}x_j^2\left(1 + \frac{\epsilon_{si}}{x_j C_{ox}}\right)^2,$$

where x_{min} is the position of the minimum bulk potential φ_{min}, x_d is the depletion width of the gate modulation region, x_j is the junction depth of the buried channel, q is the electronic charge, ϵ_{si} is the silicon permittivity, C_{ox} $(=\epsilon_{ox}/t_{ox})$ is the gate capacitance per unit area, ϵ_{ox} is the oxide permittivity, t_{ox} is the gate oxide thickness, N_A is the doping concentration of the buried channel, and V_{FB} is the flat-band voltage. We set an upper limit, $V_{GB,max}$, for the gate bias in order to ensure the validity of eqn (1). This is achieved by making $\varphi(x = 0) = 0$ in eqn (1), such that the density of the electrons induced at the surface is equal to N_D, thus yielding:

$$V_{GB,max} = V_{FB} + V_1 - \frac{\sqrt{F}\cdot x_j}{\sqrt{D}\cdot(\sqrt{E} + 1)} \times \sqrt{V_2} - \left[\frac{\sqrt{F}\cdot x_j}{\sqrt{D}\cdot(\sqrt{E} + 1)}\right]^2 \quad (2)$$

where $D = 2\epsilon_{si}/(qN_A)$, $E = N_D/(N_A + N_D)$, and $F = 1 - E$. Equation (1) clearly reveals that the position of the minimum potential is away from the surface, indicating that the injected holes almost go through the potential valley, rather than along the surface, as in deeply depleted surface channel MOSFET structures[1–8]. The validity of eqns (1) and (2) is described later.

From the simulation results, we have found that for $V_{GB} < 0.1$ V, the current component through the gate modulation depletion region is exponentially greater than that through the underlying neutral bulk region. Hole diffusion in the gate modulation region constitutes the collector current component $I_{C,diff}$:

$$I_{C,diff} = kT\mu_p W \int_0^{x_d} \frac{p_e(x) - p_c(x)}{W_B}\,dx, \quad (3)$$

where μ_p is the hole mobility, W is the channel width, and W_B is the base width. If the abrupt depletion approximation is applied to the emitter and collector depletion regions, the base width W_B can be effectively evaluated by:

$$W_B = L - L_e - L_c, \quad (4)$$

where L is the channel length,

$$L_e = \sqrt{\frac{2\epsilon_{si}}{qN_A}(\phi_{bi} - V_{EB} + \varphi_{min})},$$

and

$$L_c = \sqrt{\frac{2\epsilon_{si}}{qN_A}(\phi_{bi} - V_{CB} + \varphi_{min})},$$

where L_e and L_c are the depletion extensions at the emitter and collector ends, respectively, and ϕ_{bi} is the built-in potential. Since the hole quasi-Fermi levels at the emitter and collector ends are $\phi_{fn} + V_{EB}$ and $\phi_{fn} + V_{CB}$, respectively, the hole concentration $p_e(x)$ at the emitter end and $p_c(x)$ at the collector end can be expressed as:

$$p_e(x) = n_i \exp\left[\frac{q(\phi_{fn} - \varphi(x) + V_{EB})}{kT}\right],$$

$$p_c(x) = n_i \exp\left[\frac{q(\phi_{fn} - \varphi(x) + V_{CB})}{kT}\right]. \quad (5)$$

By substituting the potential distribution (1) into eqns (3) and (5), we obtain:

$$I_{C,diff} = \eta\frac{W}{W_B}n_i kT\mu_p \exp\left(-\frac{q}{kT}\varphi_{min}\right) \times \left[\exp\left(\frac{qV_{EB}}{kT}\right) - \exp\left(\frac{qV_{CB}}{kT}\right)\right], \quad (6)$$

$$\eta = \exp\left(\frac{q\phi_{fn}}{kT}\right)\left\{\int_0^{x_j} \exp\left[\frac{-q^2N_A}{2\epsilon_{si}kT}(x - x_{min})^2\right]dx + \int_{x_j}^{x_d} \exp\left[\frac{-q^2}{2\epsilon_{si}kT}[N_A(x_j - x_{min})^2 + N_D(x_j^2 + 2x_d(x - x_j) - x^2)]\right]dx\right\}.$$

Therefore, we have achieved a new model for the low-level collector current, analytically expressed as a function of the structure and process parameters such as N_A, N_D, t_{ox}, V_{FB} and x_j, and the bias parameters such as V_{GB}, V_{EB}, and V_{CB}.

The calculated results of the low-level collector I–V characteristics using eqn (6) and the potential distribution in the mid-channel using eqn (1) are together plotted in Figs 3 and 5, respectively. In these figures, the experimental data and/or the calibrated two-dimensional simulation results are utilized to check the validity of the model. The doping concentration parameter, N_A, in the model has been appropriately determined by making $N_A = \int_0^{x_j} N(x)\,dx/x_j$, where $N(x)$ is the doping distribution of the buried channel. Agreements between Figs 3 and 5 show that the measured and simulated results can be appropriately reproduced by the model. Using the same structure and process parameters, the upper limit $V_{GB,max}$, based on eqn (2) for ensuring the validity of the model, has been calculated to be about 0.1 V, which is reasonably in agreement with that demonstrated experimentally in Fig. 3, i.e., for $V_{GB} > 0.1$ V other components such as the parasitic bipolar collector current, must be taken into account. Note that eqn (4) explicitly expresses the Early effect, which has been reported in detail in [11].

We have further found that the first term in the η expression of eqn (6) is about 2–3 orders of magnitude larger than the second term. Therefore, a compact formulation for η can further be derived in terms of the error function, leading to:

$$I_{C,diff} = I_{CO}\exp\left[\frac{q(V_{EB}-\varphi_{min})}{kT}\right] \tag{7}$$

$$I_{CO} = \frac{\sqrt{\pi}}{\sqrt{q^2N_A/2\epsilon_{si}kT}}\frac{W}{W_B}n_i kT\mu_p \times\left[erf\left(\sqrt{\frac{N_D}{N_D+N_A}}\frac{q(-\varphi_{min})}{kT}\right)\right.$$

$$\left.+erf\left(\sqrt{\frac{q^2N_A}{2\epsilon_{si}kT}}x_j-\sqrt{\frac{N_D}{N_D+N_A}}\frac{q(-\varphi_{min})}{kT}\right)\right].$$

Equation (7) transparently demonstrates that the low-level collector current can be exponentially increased by lowering the barrier height, thus explicitly explaining the measured high current gains. Figure 7 depicts the relationship of the collector current vs the effective forward bias ($V_{EB} - \varphi_{min}$), with V_{GB} as parameter. Close agreement in a wide current range validates the analytical model of eqn (7).

According to the above description, the measured collector I–V characteristics in Fig. 3 can be separated into three distinct components: the gate-controlled diffusion current in low-level injection as modeled by eqns (6) or (7), the drift current due to the holes appearing at the surface, and the parasitic bipolar collector current. The parasitic bipolar collector current dominates for $V_{GB} > 0.5$ V and thus can easily be extracted experimentally. A complete expression concerning both the drift current and the parasitic bipolar collector current can be found in our recent work[8] with the signs appropriately exchanged. The fitting process has also been described in detail in [11] and can be employed here accordingly. The corresponding calculated results are plotted in Fig. 8, along with the measured I–V characteristics for comparison. In Fig. 8, the error between the measurement and calculation is about 20–30% for a wide range of V_{EB} between 0.1 and 1.0 V.

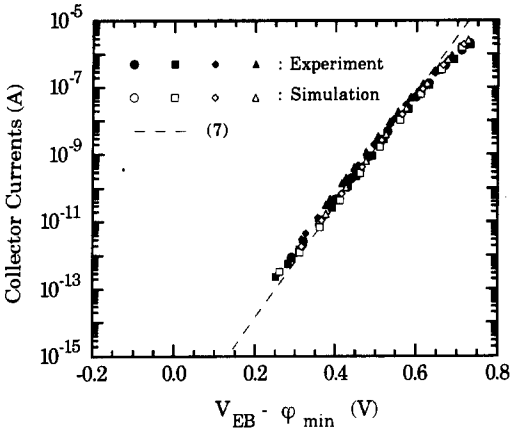


Fig. 7. Measured, simulated, and calculated collector currents as functions of the effective surface emitter–base junction bias voltage ($V_{EB} - \varphi_{min}$) for $-0.2\,V \leq V_{GB} \leq 0.1$ V.

5. CONCLUSION

A high gain p–n–p gated lateral bipolar transistor in a counter-type channel p-MOSFET structure has been investigated in detail. Both the experimental and two-dimensional simulation results have exhibited that ideal bipolar I–V characteristics, with high current gains, can only be obtained if the counter-type

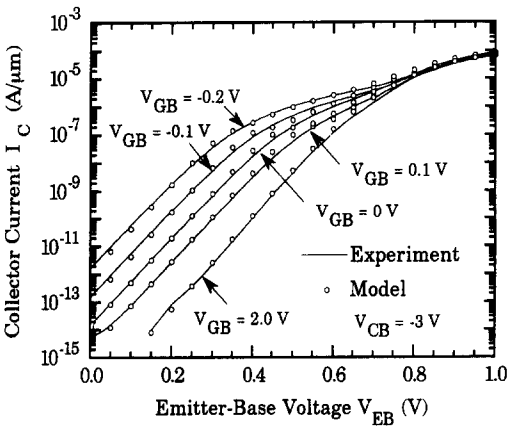


Fig. 8. Comparison between the calculated and measured I_C–V_{EB} characteristics with V_{GB} as parameter.

channel is fully depleted. An analytical model has also been established for providing transparent understanding of the behavior of the holes injected into the fully depleted channel. Experimental data and two-dimensional simulation results have both confirmed the validity of the model. The measured I–V characteristics in a wide operation range have been appropriately reproduced.

Acknowledgements—The authors would like to thank the reviewers for their helpful suggestions and comments. This work was supported by the National Science Council under Contract NSC 83-0404-E-009-087.

REFERENCES

1. S. Verdonckt-Vandebroek, S. S. Wong and P. K. Ko, *IEEE IEDM Tech. Dig.* 406 (1988).
2. J. C. S. Woo, S. Wong, S. Verdonckt-Vandebroek, P. Ko and P. K. Vasudev, *IEEE Proc. Bipolar Circuits and Technology Meeting* 152 (1989).
3. S. Verdonckt-Vandebroek, S. S. Wong, J. C. S. Woo and P. K. Ko, *IEEE Trans. Electron Devices* **38,** 2487 (1991).
4. S. Verdonckt-Vandebroek, J. You, J. C. S. Woo and S. S. Wong, *IEEE Electron Device Lett.* **13,** 312 (1992).
5. T. H. Huang and M. J. Chen, *IEEE Trans. Electron Devices* **42,** 321 (1995).
6. K. K. Au, P. G. Y. Tsui, Y. S. Kim, K. K. Diogu, M. L. Kosty and C. M. Palmer, *IEEE Proc. Custom Integrated Circuits Conference* 18.5.1 (1991).
7. K. Joardar, *IEEE Trans. Electron Devices* **41,** 373 (1994).
8. T. H. Huang and M. J. Chen, *Solid-St. Electron.* **38,** 115 (1995).
9. TMA MEDICI, *Two-Dimensional Device Simulation Program*, Version 1.1. Technology Modeling Association, Inc. (1993).
10. C. K. Kim, in *Charge-Coupled Devices and Systems* (Edited by M. J. Howes and D. V. Morgan), p. 47. Wiley, New York (1979).
11. T. H. Huang, *CMOS-Compatible High-Gain Gated Lateral Bipolar Transistors: Characterization, Modeling and Applications* Ph.D. dissertation, National Chiao-Tung University (March 1995).