Assessment of ESD Robustness in High Power Light-Emitting Diodes

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ABSTRACT

The capability of high-power nitride-based light-emitting diodes (HPLED) to withstand electrostatic discharge (ESD) is very important key index due to the horizontal structure of the insulating property of the sapphire substrate. However, it is difficult to real-time monitor the damage caused by the ESD stress because it occurred in a very short period. Current-voltage (I-V) curves and electroluminescence (EL) spectrum were applied to study the change during the series ESD stress. Time-resolved optical beam induced current (TR-OBIC) was used to analyze the characteristics of the delay time between normal region and the defect point caused by ESD stress. Transmission electron microscopy (TEM) was used to compare to the difference in the distribution of damage region and investigate the failure modes. During the series ESD stresses, V-shaped pits suffered from the high electrical field and the distance from multi-quantum well (MQW). The bottom of V-shaped defect would be one of index to assess the ESD endurance of LED chips.

Keywords: light emitting diode (LED), electrostatic discharge (ESD), Time-resolved optical beam induced current (TR-OBIC), V-defect.

1. INTRODUCTION

In recent years, high power white light emitting diodes (LEDs) have attracted much interest due to the extensive demands such as liquid crystal display (LCD) backlights, automobile lighting and general illumination. Many applications of LEDs become more and more popular so the papers have investigated the failure issues of the LEDs [1]-[3]. The rapid developments of the solid state light (SSL) of LEDs are due to several advantages comparing to conventional lights, such as longer lifetime, higher efficiency, higher ESD endurance, and so on. Due to the insulating feature of sapphire substrates, it is very important to improve ESD reliability of GaN-based devices. In the investigation of ESD endurance, there are many methods to combine a GaN-based LED with a device such as a MOS capacitor [4], an inverse-parallel protection diode [5], CMOS protection circuits [6], a GaN Schottky diode [7], a Si-based Zener diode [8].

Before the shipment of LED chips, they have to pass a sampling inspection of ESD stress today. The ESD test is a part of reliability in LED chips in order to check the early failure of LED chips. It is important to understand the role of ESD stress and the physical mechanisms to evaluate the robustness of an ESD stress. Three fundamental testing modes to simulate ESD stress, which are human body model (HBM), machine model (MM), and charged device model (CDM).

In this study, the damages were demonstrated in detail by the high resolution examination instruments to investigate the failure of LED chips due to ESD simulation.

2. EXPERIMENT

As shown in Fig. 1(a), commercial products of 1W blue LED with rate current 350mA are applied for ESD test without the protection of silicone and plastic lens. The available chips (dominant wavelength at 458 nm) in this investigation were growth on the substrate of (0001) sapphire with the size of 1×1 mm^2. LED cross-section structure consisted of a low-temperature thick GaN buffer layer, a highly conductive n-type GaN layer, an InGaN/GaN MQW active layer, and a p-type GaN layer as displayed in Fig.1(b). A mesa was deposited to preserve the sidewall of the LED device to perform for the current isolation and silicon dioxide film. A thin layer of indium tin oxide (ITO) was deposited around 300 nm thicknesses on the p-GaN layer to improve the current spreading. This study will focus on the effect of test conditions and procedures of ESD test for the LEDs, and try to investigate to ESD failure mechanisms. In this study, we applied the different ESD stresses, which are "discharge frequency", "discharge times "and " discharge voltage in each step" to the treated chips from the same wafer to explore the accumulation effect of ESD stress. Both of reverse leakage current and optical output power are the key indexes to assess the ESD endurance of LEDs. At first, the characteristics of electroluminescence (EL) spectrum by integrating sphere with spectroradiometer IS-CAS140B and the current-voltage (I-V) using Keithley 2430 sourcemeter were measured before the ESD stresses. The ESD stresses were simulated by an ESD/CDM simulator of Tokyo Electronics Trading Co. Ltd., which meets all of the testing requirements specified in MIL-STD-883 Method 3015, MIL-STD-750 Method 1020, ESD STM5.1, and EIA/JEDEC JESD22-A114-B for HBM model. After the ESD stresses, both of EL spectrum and I-V characteristics were examined and then specific damaged chips were selected to the further investigate ESD failure mechanisms of LED chips.

The following analyses were applied to investigate ESD failure mechanisms and ESD endurance of LED chips. The electroluminescent (EL) mapping images are measured by ProMetric Color Model 14011 of Radiant Imaging INC. Time-resolved optical beam induced current (TR-OBIC) is examined by Olympus Fluoview-IX70 with lock-in amplifier. In destructive failure analysis, the abnormal locations are taken by FEI Nova-600 of focus ion beam (FIB) after defining the defective point by infra-red optical beam induced resistance change (IR-OBIRCH) images. The local cross- section is captured by Hitachi S-4800 scanning electron microscope (SEM). The detail images of transmission electron microscope (TEM) are taken by FET Tecnai G2F-20.
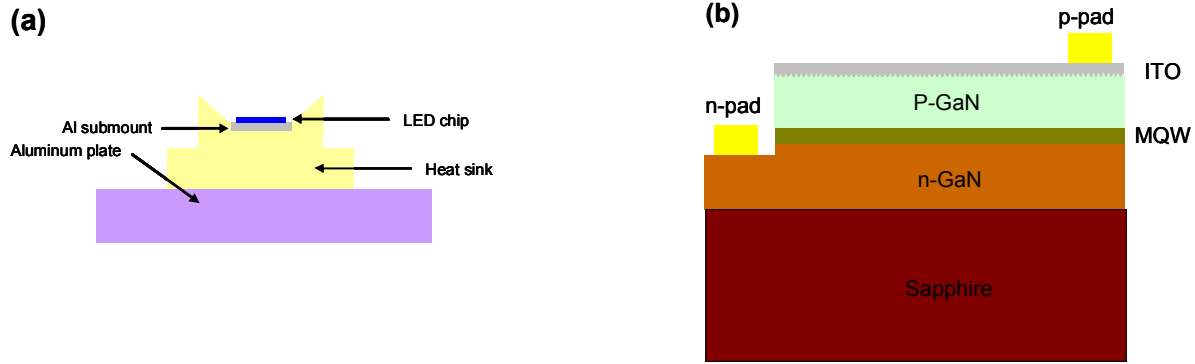
Fig. 1: (a) Configuration of GaN-based LED package. (b) Schematic diagram of GaN-based LED chip structure.

3. RESULTS AND DISCUSSION

In the study, more than two thousands chips in one wafer were measured their basic properties. As presented in Fig.2, the representative LED chips were selected to apply the ESD stresses. After the series forward ESD stresses of 100V, 250V, 500V, 1kV, 2kV and 4k, the reverse leakage current of majority LED chips kept the baseline around 10^{-8} A under -5V. However, after the series reverse ESD stresses, the leakage current in most treated chips obviously increased to 1.1×10^{-4} A. As shown in Fig. 3, relative intensity of dominant wavelength rapidly decreased under 350mA/25℃ without dominant wavelength shift after reverse ESD series stress. On the other hand, the damage caused by forward ESD stress was not significant, especially in leakage current. Therefore, the experiment in the next phase would only investigate the failure mechanisms of reverse ESD stress of 4kV.

Two different intervals in ESD pulse, which were 3 minutes and 0.8 seconds, were used to research the influence of discharge frequency and discharge times. As shown in Fig. 4, the shorter interval time (0.8 seconds) in ESD pulse would cause the larger leakage current around six to seven times than the longer delay time (3 minutes). In the same way, the relative intensity of the shorter interval time (0.8 seconds) in ESD pulse reduced to two-third and the relative intensity of dominant wavelength was lower about one-half than the longer delay time (3 minutes) as displayed in Fig. 5. Therefore, the interval of ESD pulse closely correlates to the endurance of LED chips. In the other words, the accumulation phenomena in the LED chips would influence the ESD robustness.
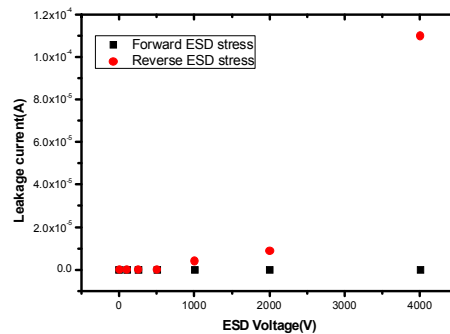

Fig. 2: Reverse leakage current after forward and reverse ESD stresses.
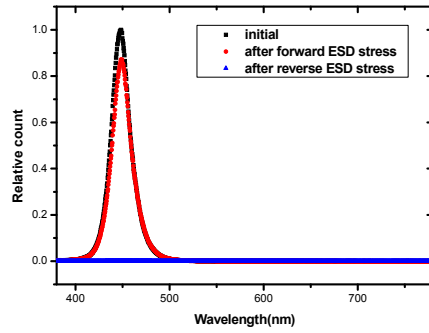
Fig. 3: The spectrum distribution before and after the series forward or reverse ESD stresses.

After the series of reverse ESD stresses, OBIC was used to define the failure point as shown in the right inset of Fig. 6 and time-resolved OBIC (TR-OBIC) would change the frequency of pulse laser to investigate the difference between normal region and damage point caused by ESD stresses. In this analysis, we applied the characteristic that the signal of OBIC was the same with Ti: Sapphire pulse laser to measure the phase of OBIC by the lock-in amplifier. In the analysis of normal region, the phase delay (red line) was proportional to the frequency and the intensity of amplitude (blue line) was inversely proportional to the frequency. However, compared with Fig. 6(a) and Fig. 6(b), the intensity of amplitude has the different trend as the frequency increasing in the hot spot (defect point). According to the following formula, the phase was converted to the delay time as a function of frequency.

$$T_d = \frac{\theta_p / 360°}{F_m}$$

where Td is delay time, θp is phase θ, and Fm is modulation frequency. As shown in Fig. 7, the defect point caused by ESD stress has the different delay time from the normal region.

Figure 8(a) presented EL mapping of treated chip after the series ESD stress. The intensity distribution of light was obvious decreased near the left bottom corner of the chip and the surface exhibited the melting damage around the diameter of 4 um by SEM review as displayed in Fig. 8(b).
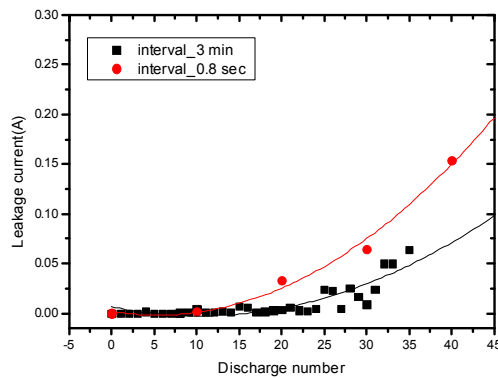

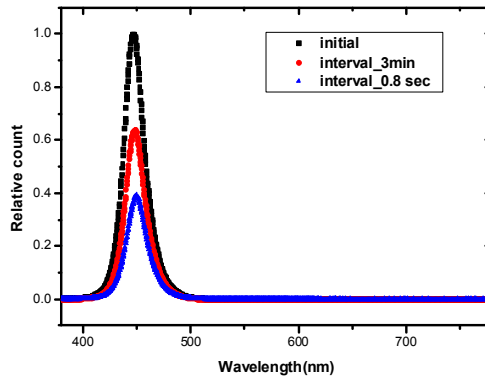Fig. 4: Reverse leakage current after two different intervals in ESD pulse.

Fig. 5: The spectrum distribution after two different intervals in ESD pulse.

For further investigating the failure mechanisms, the cross section of LED chip was drilled by FIB and explored the failure interfaces between different layers and dislocations through TEM inspection as shown in Fig. 9. The melting region displayed between ITO layer and p-GaN layer around the deeper V-shaped defect that had the smaller distance from ITO layer to MQW around five times than other V-defect. Therefore, the current might go through the shorter circuits, and the LED chip produced heat instead of light. The increase of junction temperature and the extra electrical fields induced by ESD stress become the driving force to patch the chip defect, and thus ESD stress reduced the conductivity of the dislocations for leakage currents. The dislocation density would be not only the index to evaluate the ESD endurance but also the depth of V-defect. Therefore, the performances of surface profile and leakage current of LED chip are also the main assessment factors.
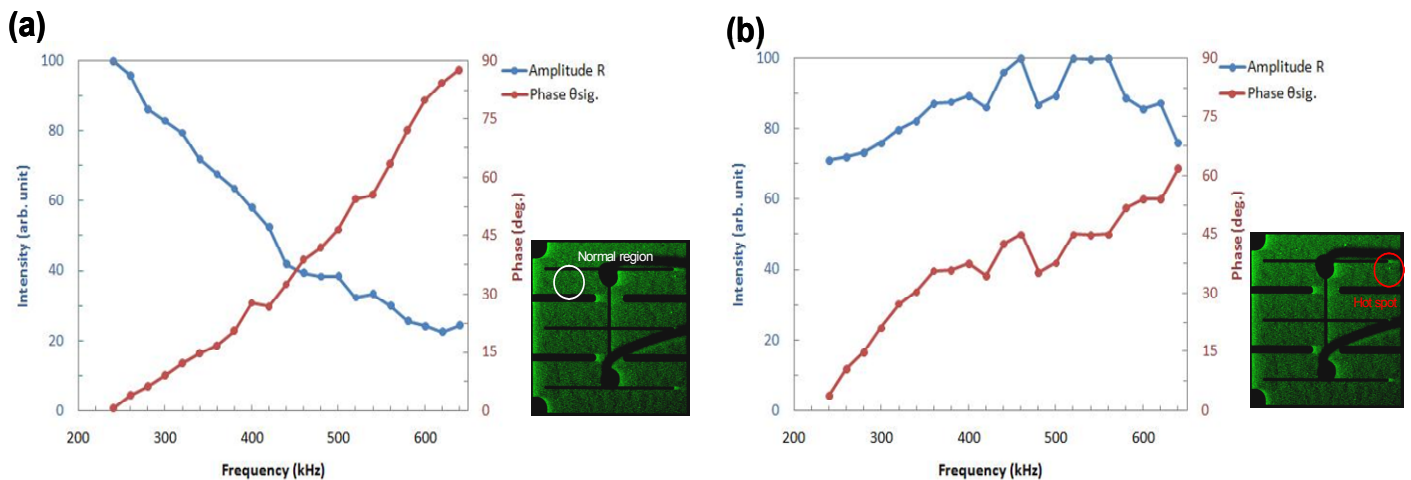

Fig. 6: Relative intensity and amplitude as a function of frequency (a) normal region (b) hot spot (defect point).
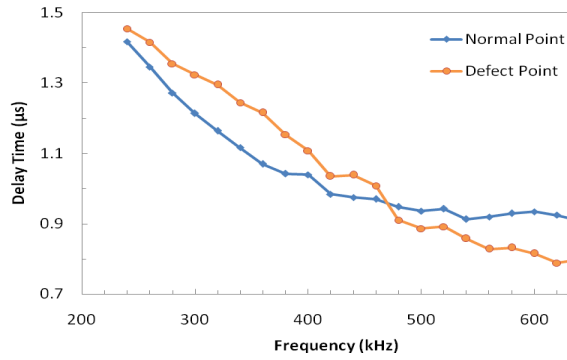
Fig. 7: Delay time as a function of frequency between normal point and defect point.
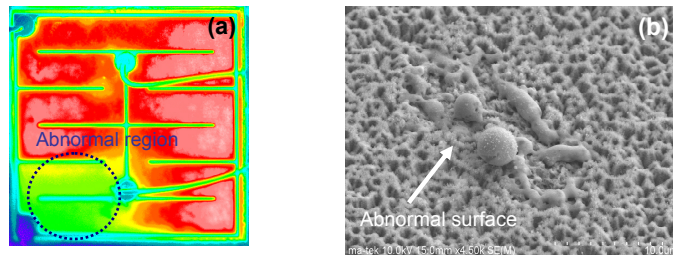

Fig. 8: (a) EL mapping image after reverse ESD stress (b) Top view of SEM image in the failure region before FIB process.
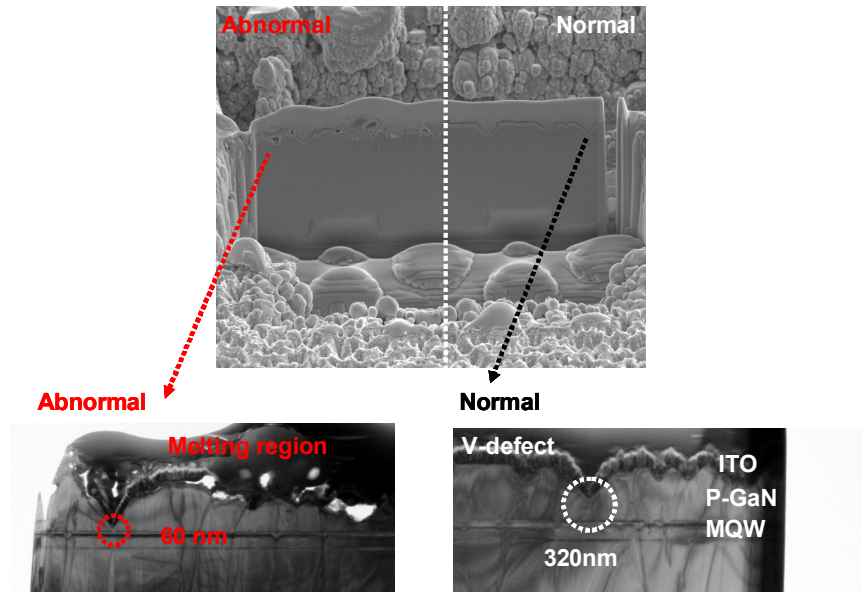

Fig. 9: TEM cross-section images showing that the different dimensions of V-shaped pits from the pit to multi-quantum well between normal region and abnormal region.

4. CONCLUSION

In the investigation, the specific damage characteristics caused by ESD stress are found in the definite power LED chips. When the applied ESD voltage is over the critical point of ESD endurance, the forward ESD stress would induce series damages, especially in the leakage current and light intensity without the dominant wavelength shift. Moreover, the interval of ESD testing stress plays an important role in the endurance of LED chips so the accumulation effect would influence the ESD endurance. According to the analysis of TR-OBIC, the defect caused by ESD stress would shows the different delay time comparing to the normal region. If no consideration about in-line process issue, V-shaped defects with high electrical field are the major factor to enhance ESD damages during the ESD stress due to the shorter distance between ITO layer and MQW. Our results suggest that the modification of the V-shaped defect and surface morphology are significant to improve the ESD endurance.

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