Novel Two-Bit-per-Cell Resistive-Switching Memory for Low-Cost Embedded Applications

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***Abstract*—A novel two-bit-per-cell embedded nonvolatile memory (NVM) device requiring no additional mask and process modification in a logic technology has been proposed using a low-temperature poly-Si thin-film transistor with a HfO_2/Ni gate stack. The feature of two-bit-per-cell is realized by independent localized resistive switching (RS) at the drain and source bits, respectively, and enables increased bit density over the present single-poly NVM for low-cost embedded applications. Furthermore, minimal degradation of the transistor characteristics after RS allows interchangeable logic/memory operations in an identical device.**

***Index Terms*—Embedded nonvolatile memory (NVM), resistive switching (RS), resistive-switching random access memory (RRAM), two-bit-per-cell.**

I. Introduction

RESISTIVE-SWITCHING random access memory (RRAM) has garnered significant interest for next-generation nonvolatile memory (NVM) applications because of its numerous advantages, including simple cell structure, low operational voltage, fast switching speed, and high integration density [1]. The most popular RRAM cell structure comprises a layer of transition metal oxides such as NiO, TiO_2, CuO, and HfO_2 placed between two metal electrodes in a metal–insulator–metal (MIM) configuration. Although the MIM structure can be implemented via back-end metallization processes for embedded memory applications where both logic core and memory array are present, it increases the manufacturing cost because the materials required in RRAM cells do not typically exist in the back-end process of standard logic integrated circuits, and additional masks are also unavoidable to implement back-end MIM capacitors. Recently, resistive-switching (RS) characteristics have been discovered in various metal–insulator–Si capacitors and transistors with HfO_2-based gate dielectrics and Ni-based metal gates [2]–[5]. The results inspired us to investigate the integration of RRAM cells into the front-end transistors as an ultralow-cost embedded NVM technology because it does not require modifying process steps or adding extra masks in the standard logic process.

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In this letter, we demonstrate a low-temperature poly-Si thin-film transistor (TFT) with a HfO_2 gate dielectric and a Ni metal gate using a logic-compatible process. An identical TFT can be used as a logic switch, an RS memory, or an interchangeable logic/memory multifunctional device. Maximum process temperature below 600 °C further enables new applications on 3-D integrated circuits and system-on-panel displays. Additionally, we show that the location where RS occurs can be locally confined in the one-transistor (1T) structure, either to the drain or to the source terminal. This enables reliable two-bit-per-cell operations with increased bit density, i.e., 0.5T per bit for a passive array and 1.5T per bit for an active array, whereas the present low-cost charge-based single-poly embedded NVM technology requires at least 2T per bit [6].

II. Experimental Procedures

A gate-last p-channel poly-Si TFT was fabricated using a four-mask process flow similar to that previously reported [7]. First, a 50-nm amorphous silicon (α-Si) layer was deposited on 550-nm SiO_2 by low-pressure chemical vapor deposition at 550 °C. Solid-phase crystallization at 600 °C for 24 h in N_2 ambient was performed to convert α-Si to poly-Si. Active regions were defined by conventional lithography and dry etching. Source/drain regions were doped by boron ion implantation using a photoresist as an implant mask over channels, followed by a dopant activation process at 600 °C for 12 h. After rapid thermal oxidation at 500 °C for 10 s in O_2 ambient, 20-nm HfO_2 was deposited by metal–organic chemical vapor deposition at 500 °C using $Hf(OtBu)_2(mmp)_2$ as a precursor. Ni gate electrodes with a thickness of 100 nm were defined by a liftoff process. Finally, the source/drain regions were opened by dry etching, and 350-nm Al was deposited and patterned as contact pads.

III. Results and Discussion

Fig. 1(a) shows well-behaved I_D–V_G characteristics of the p-channel poly-Si TFT device with a current on/off ratio of over six orders of magnitude. To enable RS in HfO_2 at the drain bit, a forming voltage of about -10 V was applied to the drain while the gate was grounded. RS was nonpolar [2], but only bipolar RS was utilized in this study. Typical bipolar RS characteristics are illustrated in Fig. 1(b) with negative set voltages V_{SET} and positive reset voltages V_{RESET} by dc I_D–V_D sweeps. The difference of drain current I_D at low-resistance state (LRS) and high-resistance state (HRS) can be as high as five orders of magnitude. RS was attributed to the formation

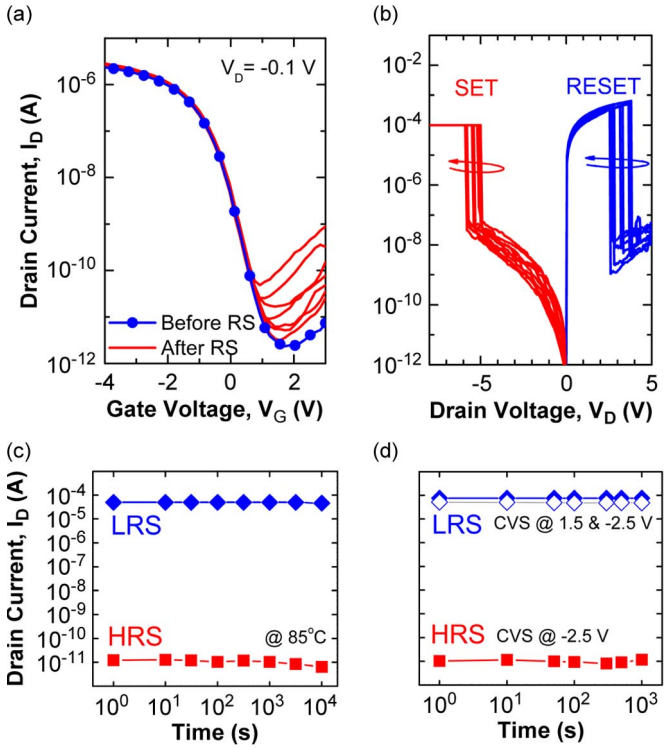


Fig. 1. (a) I_D–V_G characteristics of the p-channel poly-Si TFT device at its virgin state and after RS cycles. The channel length and width were 5 and 10 μm, respectively. (b) Typical bipolar RS characteristics by dc I_D–V_D sweeps while V_G was grounded. (c) Retention of LRS and HRS at 85 °C. (d) Disturb of HRS at −2.5 V and disturb of LRS at 1.5 and −2.5 V.

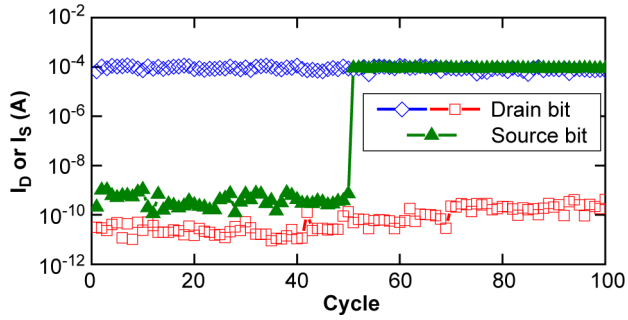


Fig. 2. Readout of I_D and I_S at −0.5 V showing no interference between the drain/source bits during 100 successive bipolar RS cycles at the drain bit. The source bit was intentionally set to LRS after the first 50 cycles.

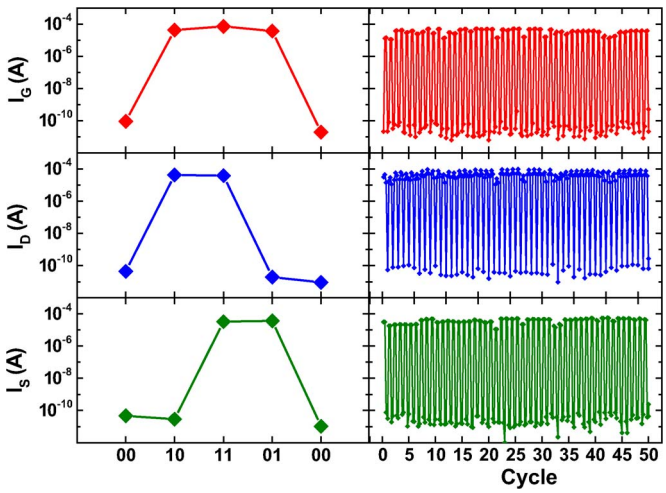
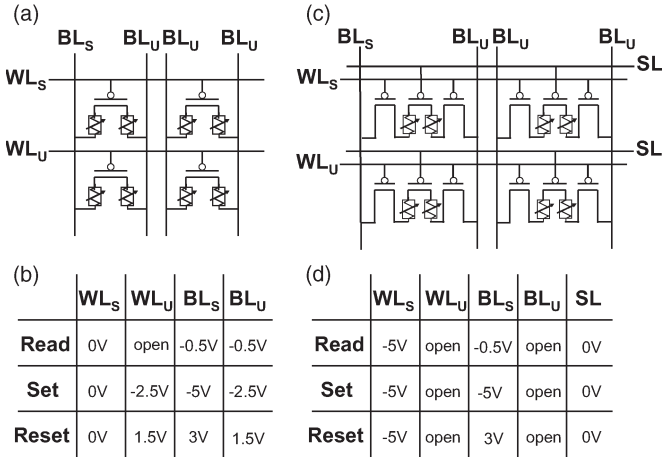


Fig. 3. Simultaneous I_G, I_D, and I_S readout of a two-bit-per-cell programming sequence 00 (D:HRS; S:HRS)→10 (D:LRS; S:HRS)→11 (D:LRS; S:LRS)→01 (D:HRS; S:LRS)→00 (D:HRS; S:HRS) for (left) one cycle and (right) successive 50 cycles.

of Ni filaments near the drain. Details on the mechanism have been extensively discussed elsewhere [2]. After being reset to its HRS, the I_D–V_G characteristics of the poly-Si TFT device can be fully recovered to its virgin state except for the increased off current due to the leakage current between the gate and the drain at HRS. A negligible shift of threshold voltage $V_{\rm TH}$ and yet sufficient current on/off ratio suggest that the identical TFT can be used as a logic switch and a memory cell interchangeably. Fig. 1(c) and (d) demonstrates the excellent immunity to thermal and set/reset disturbs. Both HRS and LRS were highly stable at 85 °C and under constant voltage stress (CVS) at one half of the set/reset voltages. LRS was also immune to unipolar reset at one half of the set voltage.

Similar RS characteristics can be obtained at the source bit by simply exchanging the source with the drain. In the previous studies of RS in high-k transistors [3], [4], $|V_G| > |V_{\rm TH}|$ was applied to trigger RS. However, the location of filament formation was rather random across the entire device region because of the existence of an inversion channel during RS. To confine the filament formation only at the selected bit for a reliable two-bit-per-cell operation, the TFT device was turned off by grounding the gate at set/reset. Fig. 2 depicts I_D and I_S at the read condition when the drain bit was subjected to repeated cycling. During the first 50 cycles, the source bit was reset to HRS. I_S remained low even when the drain bit was set to LRS, indicating that the localized filament was formed close to the drain. The drain bit operation was completely independent of the resistance state of the source bit, as evidenced when the source bit was intentionally set to LRS after 50 cycles. Fig. 3 further shows the simultaneous I_G, I_D, and I_S readout in a two-bit-per-cell programming sequence 00 (D:HRS; S:HRS)→10 (D:LRS; S:HRS)→11 (D:LRS; S:LRS)→01 (D:HRS; S:LRS)→00 (D:HRS; S:HRS). The robust cycling endurance highlighted the immunity of set/reset interference between two neighboring bits.

Fig. 4(a) illustrates an array architecture comprising a 1T unit cell. Because the drain and source bits can be independently operated, the two-bit-per-cell NVM was equivalent to a RRAM passive array with high integration density of 0.5T per bit. The operation conditions of the proposed array are listed in Fig. 4(b). Set/reset disturbs can be minimized by a 1/2 $V_{\rm DD}$ voltage scheme [8], where full set/reset voltages were applied to the selected bit, but only 1/2 set/reset voltages were applied to the unselected bits along the selected bit/word lines. As proved in Fig. 1(d), the voltage scheme can effectively suppress disturbs, even for the worst case scenario when the 1/2 set voltage could potentially trigger unipolar reset at unselected LRS bits. A similar 1/3 $V_{\rm DD}$ voltage scheme can offer an increased disturb margin with reduced 1/3 set/reset voltages applied to any unselected bits [8]. However, read interference



(b)

	WL_S	WL_U	BL_S	BL_U
Read	0V	open	-0.5V	-0.5V
Set	0V	-2.5V	-5V	-2.5V
Reset	0V	1.5V	3V	1.5V

(d)

	WL_S	WL_U	BL_S	BL_U	SL
Read	-5V	open	-0.5V	open	0V
Set	-5V	open	-5V	open	0V
Reset	-5V	open	3V	open	0V

Fig. 4. (a) Schematic of a passive RS TFT memory array. (b) Typical operation conditions of the passive RS TFT memory array. (c) Schematic of an active RS TFT memory array. (d) Typical operation conditions of the active RS TFT memory array.

through sneak paths remained the major obstacle, similar to any other passive resistor-based arrays [9]. An all-bit-line pull-up scheme was applied to alleviate this problem in small-size arrays less than 64 bits [9] and made this compact NVM very attractive for low-bit-count embedded applications such as radio-frequency identification tags, fuse replacement, etc. As for an array size larger than 64 bits, adding additional selection transistors was necessary to prevent read interference. Fig. 4(c) and (d) shows an array architecture and operation conditions comprising a 3T unit cell that is equivalent to 1.5T per bit. Because no source/drain contacts were required between the selection and RS transistors, the cell size can be very competitive compared with at least 2T per bit in the single-poly embedded NVM.

IV. Conclusion

A new two-bit-per-cell RS memory device utilizing a logic-compatible TFT with the HfO_2 gate dielectric and the Ni metal gate has been fabricated. RS in HfO_2 can be precisely controlled at the drain and source bits independently without interference, and both LRS and HRS exhibit excellent retention and immunity to disturbs. The proposed new RS memory is highly desirable for low-cost embedded memory applications. In comparison with the mainstream embedded NVM technologies such as split-gate Flash and silicon–oxide–nitride–oxide–silicon memory, it requires no additional mask and process modification in a logic process technology. Meanwhile, its cell structure, namely, 0.5T per bit for a passive array and 1.5T per bit for an active array, is more compact than the present low-cost single-poly NVM.

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References

[1] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories—Nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, no. 25/26, pp. 2632–2663, Jul. 2009.

[2] K. L. Lin, T. H. Hou, J. Shieh, J. H. Lin, C. T. Chou, and Y. J. Lee, "Electrode dependence of filament formation in HfO_2 resistive-switching memory," *J. Appl. Phys.*, vol. 109, no. 8, p. 084 104, Apr. 2011.

[3] A. Crespo-Yepes, J. Martin-Martinez, A. Rothschild, R. Rodriguez, M. Nafria, and X. Aymerich, "Recovery of the MOSFET and circuit functionality after the dielectric breakdown of ultrathin high-k gate stacks," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 543–545, Jun. 2010.

[4] N. Raghavan, W. Liu, X. Li, X. Wu, M. Bosman, and K. L. Pey, "Filamentation mechanism of resistive switching in fully silicided high-κ gate stacks," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 454–457, Apr. 2011.

[5] X. A. Tran, H. Y. Yu, Y. C. Yeo, L. Wu, W. J. Liu, Z. R. Wang, Z. Fang, K. L. Pey, X. W. Sun, A. Y. Du, B. Y. Nguyen, and M. F. Li, "A high-yield HfOx-based unipolar resistive RAM employing Ni electrode compatible with Si-diode selector for crossbar integration," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 396–398, Mar. 2011.

[6] Y. Ma, T. Gilliland, B. Wang, R. Paulsen, A. Pesavento, C. H. Wang, H. Nguyen, T. Humes, and C. Diorio, "Reliability of pFET EEPROM with 70-Â tunnel oxide manufactured in generic logic CMOS processes," *IEEE Trans. Device Mater. Rel.*, vol. 4, no. 3, pp. 353–358, Sep. 2004.

[7] S. C. Wu, T. H. Hou, S. H. Chuang, H. C. Chou, P. Y. Kuo, T. S. Chao, and T. F. Lei, "High-performance polycrystalline silicon thin-film transistor with nickel-titanium oxide by sol–gel spin-coating and fluorine implantation," in *Proc. Int. Conf. SSDM*, 2010, pp. 479–480.

[8] Y. C. Chen, C. F. Chen, C. T. Chen, J. Y. Yu, S. Wu, S. L. Lung, R. Liu, and C. Y. Lu, "An access-transistor-free (0T/1R) non-volatile resistance random access memory (RRAM) using a novel threshold switching, self-rectifying chalcogenide device," in *IEDM Tech. Dig.*, 2003, pp. 905–908.

[9] A. Flocke and T. G. Noll, "Fundamental analysis of resistive nanocrossbars for the use in hybrid nano/CMOS-memory," in *Proc. 33rd ESSCIRC*, 2007, pp. 328–331.