Design and fabrication of a CMOS MEMS logic gate

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ABSTRACT

This study aims to develop a novel CMOS-MEMS logic gate via commercially available CMOS process (TSMC, 2P4M®). Compared to existing CMOS MEMS designs, which uses foundry processes, the proposed design imposes several new challenges including: carrying two voltage levels on a non-warping suspended plate, metal-to-metal contact, and etc. Different combinations of oxide-metal films and post-CMOS process are investigated to achieve a non-warping suspended structure layer. And different wet etchants are investigated to remove sacrificial layers without attacking structure layers and features. In a prototype design, the selected structure layer is metal-3 and oxide film; the device is released using AD-10 and titanium etchant; the device is 250 μm long, 100 μm wide, and 1.5 μm gap. The experimental results show that the suspended plate slightly curls down 0.485 μm. This device can be actuated by 10/0 V with a moving distance 50nm. The resonant frequency is measured at 36 kHz. Due to the damage of the tungsten plugs, the logic function can only be verified by its mechanical movements instead of electrical readouts for now.

Keywords: CMOS-MEMS, logic gate, tungsten plugs, metal to metal contact, non-warping suspended plate

1. INTRODUCTION

MEMS (micro-electro-mechanical system) switches have the advantages of no leakage current and low insertion loss. Thus, they have been considered one of the possible solutions for IC power management and RF transmission lines. In order to boost the applications of MEMS switches, a number of researchers studied a new device: MEMS logic gate, which is a MEMS switch that can perform Boolean algebra. With this computation capability, MEMS logic gates are expected to have more applications than the existing MEMS switches.

The research of MEMS logic gate is at an initial stage, and not many designs has been proposed. According to the designs shown in[1],[2] they should take four or more MOS-like MEMS devices to demonstrate logic functions and thus consume more layout areas. Previously, our research group proposed a novel MEMS logic gate design that does not stem from conventional MOS devices. It not only consume less silicon area but also performs NAND or NOR gate functions with the same mechanical structure. Therefore, it is promising if this device can be fabricated in situ with other IC components and work with IC components. In our previous study, the functionality of the proposed logic gate design were verified using bulk micromachining processes[3] and in-house developed CMOS-compatible, surface micromachining process[4].[5] The integration with IC components has not been verified yet.

In this paper, we aim to fabricate the proposed logic gate design using foundry-provided CMOS process and in-house developed post-CMOS process. Therefore, the integration with IC components can be approached easily and the fabrication cost can be lowered. The employed CMOS foundry process is 0.35 μm-2P4M® from the Taiwan Semiconductor Manufacturing Company (TSMC). The post-CMOS process includes: two standard post-CMOS lithography steps provided by national chip implementation center (CIC) in Taiwan, in-house developed wet etching process to release MEMS devices, and a STS RIE blanket etch to tune the structure bending.

Comparing to existing CMOS MEMS designs, which intend to be fabricated by CMOS foundry process, the proposed design imposes several new challenges including: carrying two voltage levels on a non-warping

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suspended plate, see-saw motions with dimple structures, and metal-to-metal contact between shuttle electrodes and fixed electrodes. Other than the considerations of designing in the proposed logic gate using a standard fabrication process, this paper focuses on exploring different combinations of deposited films to achieve a non-warping suspended structure, and different combinations of wet etchants in the post-CMOS process to release the MEMS structure. The design considerations and experimental results are discussed in detail in this paper.

2. OPERATION PRINCIPLES OF THE PROPOSED LOGIC GATE DESIGN

Figure 1 illustrates a caricature version of the proposed logic gate design. The proposed design consists of shuttle electrodes on the top and fixed electrodes at the bottom. When the shuttle electrodes are biased at the voltages of V_{cc+} and V_{cc-}, and the fixed electrodes (input terminals A and B) are deployed by either V_{cc+} or V_{cc-}, the devised dimensions of actuation pads (A_l and A_r in Fig. 1) produce differential electrostatic force on both sides of the shuttle electrodes. Thus, the shuttle electrodes would carry out a see-saw motion and connect the output terminal at each end to export the corresponding output voltage. If the voltage level of V_{cc+} and V_{cc-} represents "1" and "0" in digital circuitry respectively, the input-output relations of this device can be the same as a logic gate consisting of solid-state transistors. For example, the design shown in Fig. 1 can function the same as a NOR gate. Besides, reversing the bias voltages on the shuttle electrodes can switch the logic function of this device from a NOR gate function to a NAND gate function.

Based on the intended operation of this device, the design task is to ensure that the tilting plate can rotate toward the designed direction and connect with the output terminal to export signals. This is accomplished mainly by the design of the actuation pad configurations, stiffness of the torsional flexures, dimple height, gap height, and actuation voltages. The equations and design considerations were addressed in detail in our previous paper.[4] However, it should be emphasized here that the maximum tilting angle of the suspended plate is the key factor to the functionality of the device, which makes the warping of the suspended plate a critical issue in this design.

3. DEVICE FABRICATION

The proposed logic gate designs are fabricated using the TSMC 2P4M® process, which consists of two polysilicon layers, four metal layers, oxide layers in between each metal layer, and tungsten plugs for VIA. The metal layer is an aluminum layer encapsulated by titanium and titanium nitride layers.[6] The cross-sectional view of this process is shown in Fig. 2. For this logic gate design, the sacrificial layer is designed to be metal-2 layer; the suspended structure is a composite structure consisting of oxide and metal films; the dimple structures are tungsten plugs. Three different combinations of oxide-metal films were investigated to achieve a non-warping suspended plate. Type 1 uses metal-3 and oxide as the suspended structure layer; type 2 uses a composite structure of metal-3-oxide-metal-4; type 3 uses metal-4 and oxide.

Figure 3 shows the fabrication process of the type 1 design. It starts with a cross-sectional view of the design after the accomplishment of TSMC 2P4M process (Fig. 3(a)). The "Pad" mask provided by CIC were used to remove the nitride and oxide passivation layer on top of the metal-4 layer. It then goes through an anisotropic oxide etch using CIC-provided "RLS" mask and a hard mask from exposed metal-4 layer. As shown in Fig. 3(b), this etch step defines the MEMS device geometry and etch holes, and then stop on the designated sacrificial metal-2 layer. Figure 3(c) shows that the metal-2 and metal-4 layer were entirely removed to release the structure by isotropic wet etch. This is the most critical step in this fabrication process and will be discussed in detail in the later section. Figure 3(d) shows that the dielectric layer of the structure should be trimmed back to expose tungsten plugs for metal-to-metal contact. According to the design rules,[7] the thickness of the metal layer and oxide layer are both approximately 1 μm. Therefore, it is preferred that at leat 0.25 μm of oxide is removed to ensure good contact performance. This is done by using BOE (six parts of 40% NH_4F and one part of 49% HF) with a time etch of 15-second.[8] After this etching step, the gap between top and bottom electrodes are expected to be 1.5 μm. Note that, the oxide layer also provides an isolation feature for carrying two voltage levels on a suspended plate. The last step is to use STS RIE process to do a blanket etch on the exposed oxide film. This step determines the oxide thickness of the suspended structure and thus affect the deflection profile of the suspended plate. This etch step is performed using a SF_6 plasma and its recipe is presented in Table. 1. Totally, five steps are used to complete the post-CMOS process for the type 1 design.

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Figure 4 shows the fabrication process for the type 2 design. The major difference between this design and the previous one is that the metal-4 layer is protected by the passivation layer and used as one of the suspended structure layers. Type 3 design is shown in Fig. 5 and its post-CMOS process flow is omitted because it is the same as that of the type 2.

4. EXPERIMENTAL RESULTS AND DISCUSSION

Figure 6 shows a photo of the fabricated MEMS logic device after completing all the post-CMOS process of the type 1 design. Since the oxide film is transparent, the isolation features on the suspended plate, the metal film under oxide, and the dimple structures are all clearly visible. The V_{cc+} and V_{cc-}. are applied to the anchor and then transferred through micro flexures to the suspended plate. Two input signals are given to the input terminals A and B. The dimple structures are underneath the suspended plate at two ends. Two output terminals are shown at the two ends of the device, and they will be linked together through electrical interconnects later on.

4.1 Exploration of wet etchant for removing sacrificial metal layers

In the proposed logic gate design, two voltage levels (V_{cc+} and V_{cc-}) will be applied to the suspended plate on the left and right. Therefore, any metal residue from sacrificial metal-2 layer would electrically short the device. Besides, the tungsten plugs are designed to be the dimple structures for metal-to-metal contact. Therefore, the selected wet etchant need to completely remove metal layers without attacking the oxide films and tungsten plugs. The metal layer consists of titanium nitride, titanium, and aluminum. Four wet etchants for removing those materials were investigated, and their composition and experimental results were summarized in Table. 2. Those four wet etchants are aluminum etchant, AD-10 etchant, Carro's acid, and titanium etchant.

The aluminum etchant is a H_3PO_4 acid-based etchant. The high viscosity of H_3PO_4 prevents the etchant from passing through small etch holes, and thus cannot clearly remove the sacrificial aluminum layer underneath the structure layer. Carro's acid is a recommended etchant for striping the metal layers in the TSMC CMOS process[9].[10] However, the observations often find contaminations of gray particles on the structure layer after this etching step. These particles are silicon nodules and could result in plate release failure.[11] This study employs the AD-10 solution to remove aluminum for two reasons. One is that some active surfactants in AD-10 etchant can assist the etchant to infiltrate small etch holes and thus make etch reaction speed up. The other is that the etchant has high etching selectivity between the aluminum and the silicon dioxide film. Since the AD-10 does not attack Ti/TiN films, a titanium etchant must be used subsequently to remove the Ti/TiN films. After several experiments, as shown in Fig. 7, the tungsten plugs were completely removed from the VIA trenches. This denotes that the titanium etchant quickly attack tungsten plugs, which could impair the metal-to-metal contact feature of the logic gate design. So far, we have not found out a suitable etchant that can remove titanium nitride without attacking tungsten.

4.2 Passivation layer damage

Figure 8 shows a photo of type 2 and type 3 design after the lithography of the "Pad" mask and "RLS" mask. As shown in the plot, the passivation layer on top of the metal-4 were damaged for unknown reasons. This phenomenon has been observed in many process runs. The damaged passivation layer cannot provide a complete coverage for the metal-4 layer, which is a designated structure layer in type 2 and type 3 design. This greatly lower the yield of the type 2 and type 3 design.

4.3 Deflection profile of the suspended plate

Figure 9 illustrates the deflection profiles of the suspended plate of the type-2 and type-3 designs. Although the type-2 design only bends down 0.25 μm (see, Fig. 9(a)), the electrical interconnects made of metal-4 layer has been damaged due to passivation defect. Thus, the device is malfunctioning. Type-3 design bends down 1.95 μm (see, Fig. 9(b)). This bending distance is roughly the same as the gap between the top and bottom electrodes. Thus, the device is malfunctioned by touching the output terminals without applying any actuation voltage. Figure 10(a) shows the deflection profile of type-1 design. The suspended plate bends down 0.485 μm, which creates a 1 μm gap. For comparison, Fig. 10(b) shows the plate deflection of type 1 design without applying

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RIE blanket etch. The plate bending distance is approximately 0.785 μm, which creates a 0.7 μm gap. These results indicate that the RIE etching step can be applied to achieve a non-warping suspended plate in a CMOS MEMS design. Furthermore, the type 1 design is preferred because it avoids the passivation damage problem while achieving a non-warping suspended structure.

4.4 Dynamical responses

To investigate the dynamics of the proposed logic gate design, we measured the frequency response of a fabricated device using a laser doppler vibrometer (LDV) and a network analyzer. Figure 11 shows that the resonant frequency of the fabricated device was measured at approximately 36 kHz. The time response of the tilting plate is performed by applying a voltage 10 $sin(2\pi * 10^3 t)$V to one of the input terminals, while the voltage to the other input terminal is kept at zero volts. As shown in Fig. 12, the plate is moving at a frequency twice as fast as the actuation frequency; meanwhile, the plate moving distance is close to 50 nm. Unfortunately, due to the damage of the tungsten plug, the electrical readout is difficult. The logic function of the device can only be verified through its mechanical movements for now.

5. CONCLUSION

This paper presents the design and post-CMOS process for a novel MEMS logic gate fabricated by a foundry service TSMC 2P4M CMOS process. The proposed design impose serval challenges on its fabrication process including: carrying two voltage levels on a non-warping suspended plate, see-saw motions with dimple structures, and metal-to-metal contact between shuttle electrodes and fixed electrodes. For exploring the non-warping suspended structure, three different combinations of oxide-metal composite films, accompanied with the STS RIE blanket etch, were investigated. The better one is the combination of metal-3 film and oxide film. In that case, the 125 μm long suspended structure bends down 0.485 μm. For the dimple structure and metal-to-metal contact, four wet etchants (aluminum etchant, AD-10, Carro's acid, and titanium etchant) were investigated to remove the sacrificial Ti/TiN/Al layer without attacking the oxide films and tungsten plugs. Unfortunately, we found that none of above four etchants can remove titanium nitride without damaging the tungsten plugs.

In a prototype design, the device is 250 μm long, 100 μm wide. The experimental results show that this device can be actuated by 10/0 volts with a moving distance 50nm; the resonant frequency of the device is measured roughly at 36 KHz. These numbers are consistent with the equation prediction in our previous study.[4] Thus, we expect the logic functions of this device. However, due to no metal-to-metal contact in the current design, its logic function can not yet be verified by the electrical readouts.

ACKNOWLEDGMENTS

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REFERENCES

[1] Hirata, A., MacHida, K., Kyuragi, H., and Maeda, M., "A electrostatic micromechanical switch for logic operation in multichip modules on si," *Sens Actuators A Phys* **vol 80**, p 119–125 (2000).

[2] L, S.-W., J, R. W., and P, A.-M., "Mems mechancial logic units: Design and fabrication with micragem and polymumps," in [*Canadian Conference on Electrical and Computer Engineering*], 1513–1516 (2005).

[3] Chen, T.-L., *Design and Fabrication of PZT-actuated Silicon Suspensions for Hard Disk Drives*, PhD thesis, UC Berkeley (2001).

[4] Tsai, C.-Y., Kuo, W.-T., Lin, C.-B., and Chen, T.-L., "Design and fabrication of mems logic gates," *J. Micromech. Microengineering* **18**, 045001 (2008).

[5] Tsai, C.-Y. and Chen, T.-L., "Design, fabrication and calibration of a novel mems logic gate," *J Micromech Microengineering* **20**, 095021 (2010).

[6] [*Metal contact reliability of RF MEMS switches*], **6463**(646305) (2007).

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[7] Chen, Y.-L., [*CIC User Handbook-0.35 um CMOS MEMS Process v.2.0*], Taiwan Chip Implementation Center (CIC) (2006).

[8] Ying-Chou, C., Ching-Liang, D., Chi-Yuan, L., Ping-Hei, C., and Pei-Zen, C., "A mems micromirror fabricated using cmos post-process," *Sens Actuators A Phys* **120**, 573–581 (2005).

[9] Ko, C.-T., Wu, J.-P., Wang, W.-C., Huang, C.-H., Tseng, S.-H., Chen, Y.-L., and Lu, M.-C., "A highly sensitive cmos-mems capacitive tactile sensor," in [*Micro Electro Mechanical Systems*], (2006).

[10] Ming-Han, T., Chih-Ming, S., Yu-Chia, L., Chuanwei, W., and Weileun, F., "Design and application of a metal wet-etching post-process for the improvement of cmos-mems capacitive sensors," *J Micromech Microengineering* **19**, 105017 (2009).

[11] Hua, Y., Redkar, S., An, L., and Ang, G., "A study on silicon nodules due to the si precipitation in wafer fabrication," in [*Semiconductor Electronics*], *Journal of Materials Science* (2000).

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Table 1. Experiment parameters of the STS reactive ion etching (RIE)

Gas flow (sccm)	40,SF_6
Pressure (mTorr)	100
RF Power (W)	100 @ 13.56 MHz
Temperature ($\circ C$)	25
Etch rate ($\dot{A}/min$)	1000

Table 2. Wet etch rates for metal micromachining ($\dot{A}/min$)

		MATERIAL		
ETCHANT EQUIPMENT CONDITIONS	TARGET MATERIAL	Aluminum	Ti/TiN	Tungsten (W)
Aluminum Etchant ($32H_3PO_4$: $1NHO_3$: 5HAc: $6H_2O$) Heated Bench $80°C$	Aluminum	Initial etch rate : 34000 Undercut 50 (μm) Etch time : 0.2 hour Undercut 150 (μm) Etch time : 1.6 hour	×	×
AD-10 (TMAH, 2.83%) Wet Sink Room Temp.	Aluminum	3000 ∼ 4000	× ×	× ×
Carro's acid ($3H_2SO_4$: $1H_2O_2$)	Aluminum Ti/TiN	1800	Ti:2400/TiN:×	×
Titanium Etchant ($2NH_4OH$: $1H_2O_2$: 1DI water)	Ti/TiN	$>$ 100	8800	$>$ 1000

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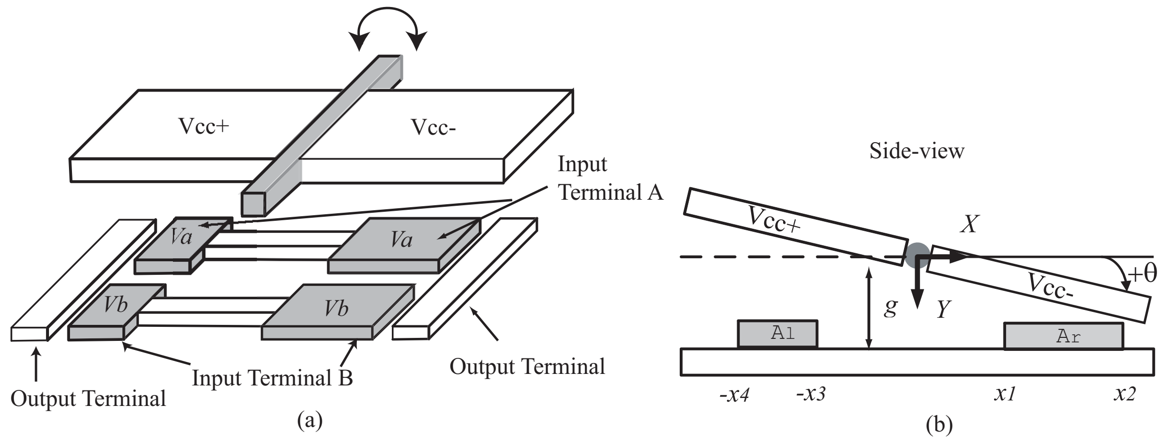

Figure 1. A torsional, two-layer MEMS logic gate design. (a) 3D view (b) Side view.

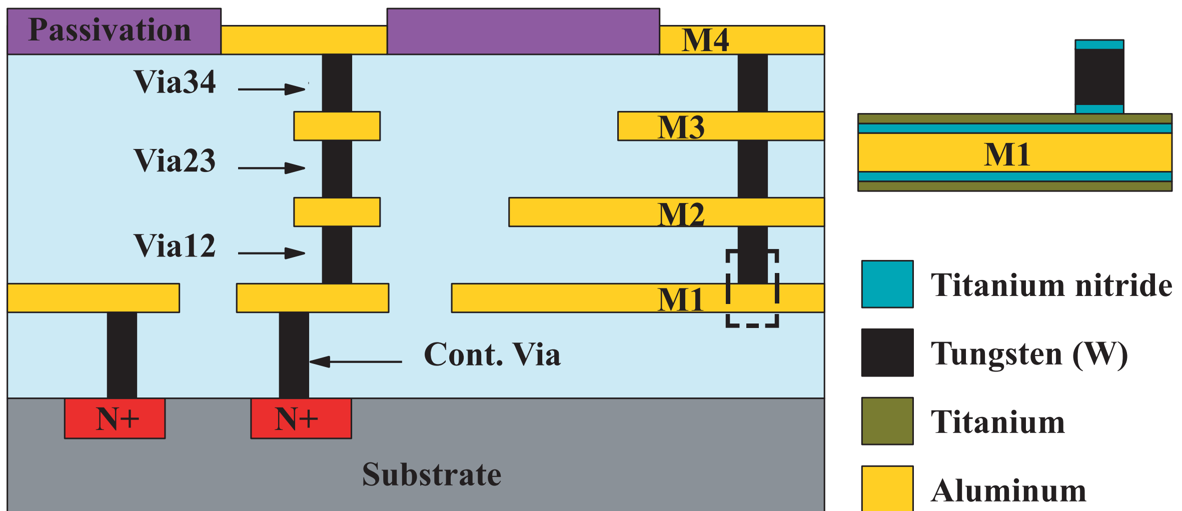

Figure 2. A schematic plot of TSMC 2P4M ® process. The close-up view shows the composite structure in each metal film.

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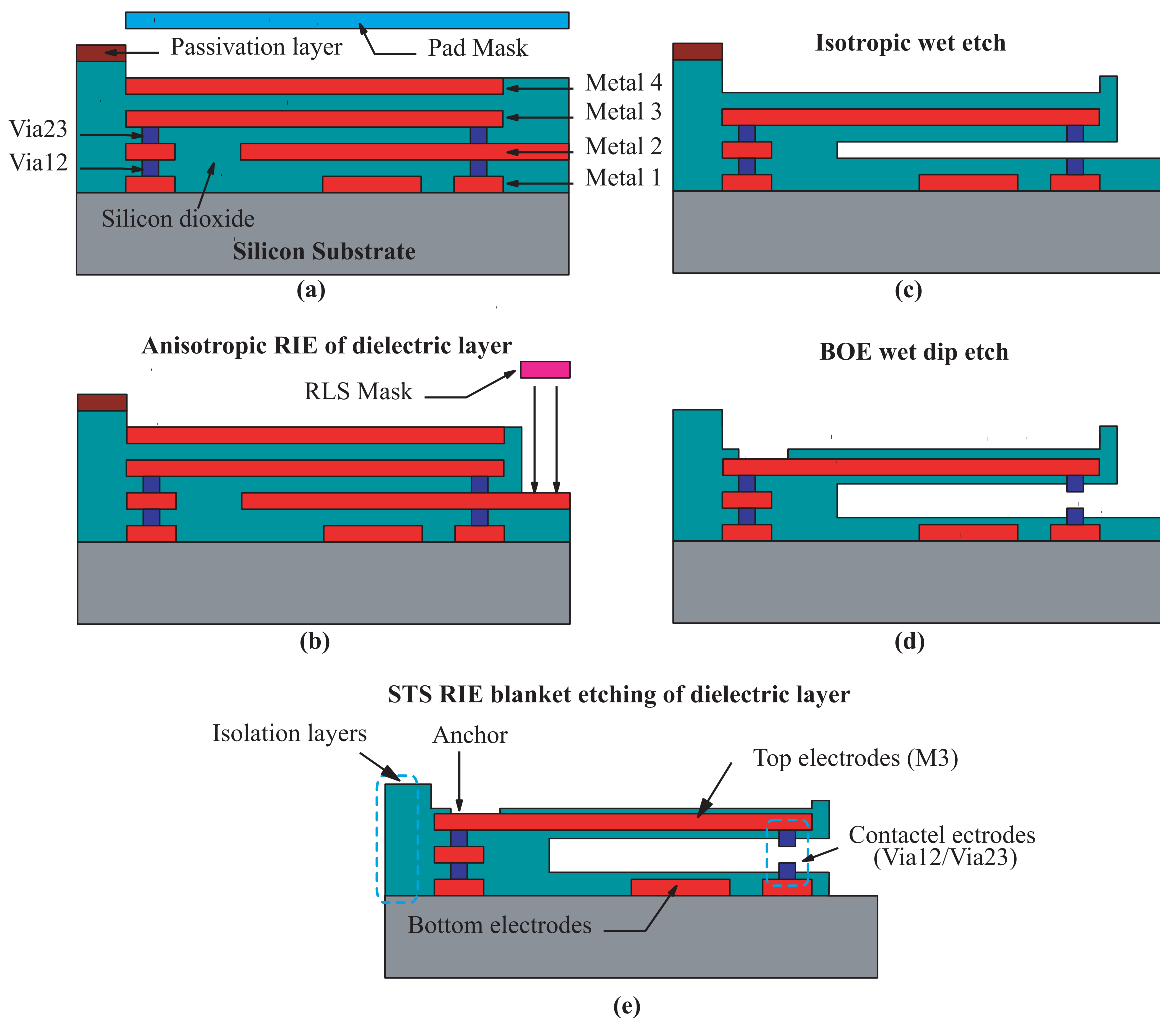

Figure 3. The process flow for fabricating the type-1 MEMS logic gate.

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Figure 4. The process flow for fabricating the type-2 MEMS logic gate.

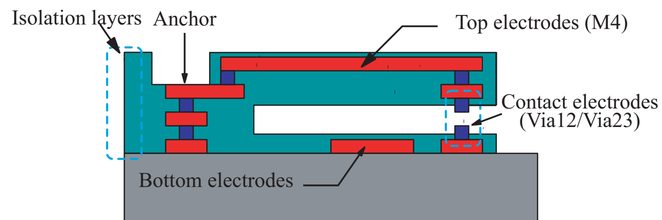

Figure 5. The cross-sectional view of the last step of the type-3 MEMS logic gate.

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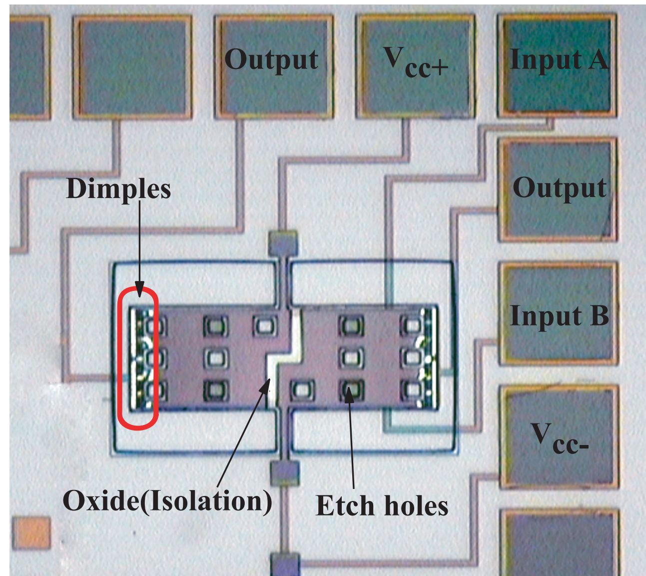

Figure 6. A photo of the fabricated type 1 MEMS logic gate.

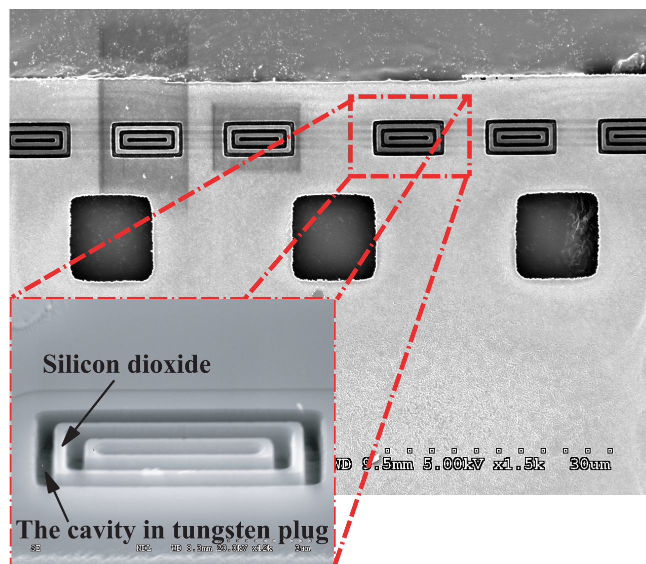

Figure 7. SEM photo of the tungsten plugs after the titanium wet etchant. The tungsten plugs were completely removed.

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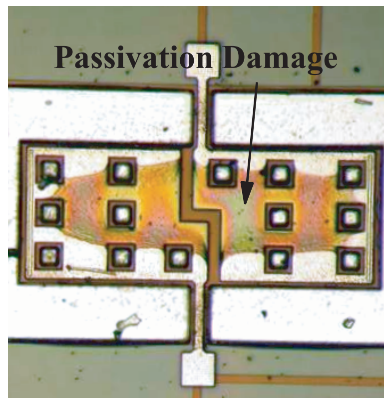

Figure 8. A photo of the type 2 and type 3 design after the Pad mask and RLS mask lithography. The passivation layer on top of the metal-4 is damaged.

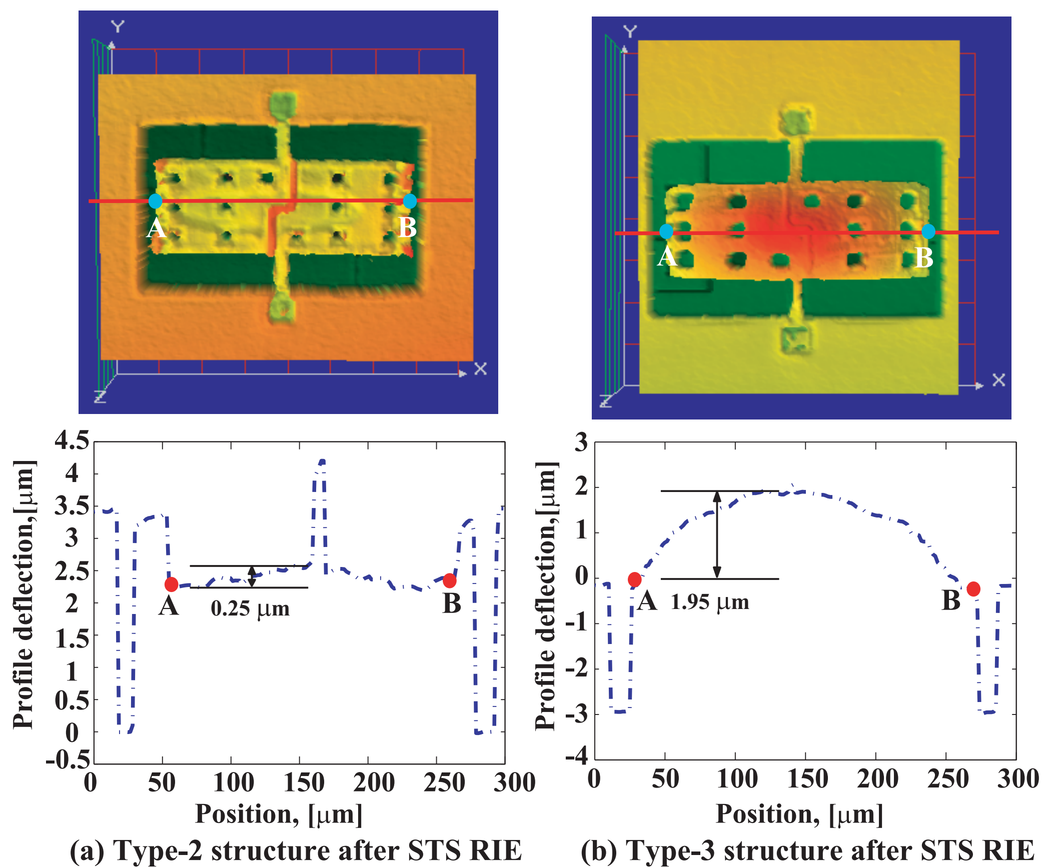

Figure 9. Deflection profiles of the type-2 and type-3 devices after the STS RIE process. (a) A type-2 structure bends down 0.25 μm. (b) A type-3 structure bends down 1.95 μm.

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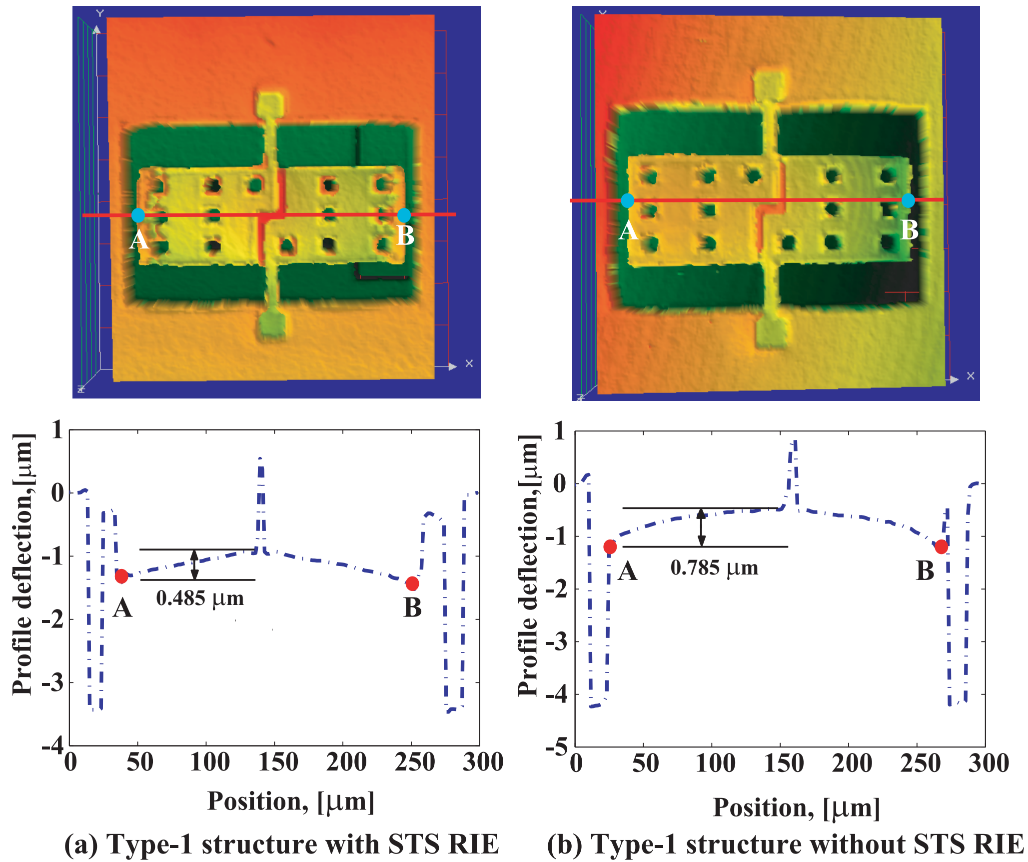

Figure 10. Deflection profiles the type-1 devices. (a) With the STS RIE process, the structure bends down 0.485 μm. (b) Without the STS RIE process, the structure bends down 0.785 μm.

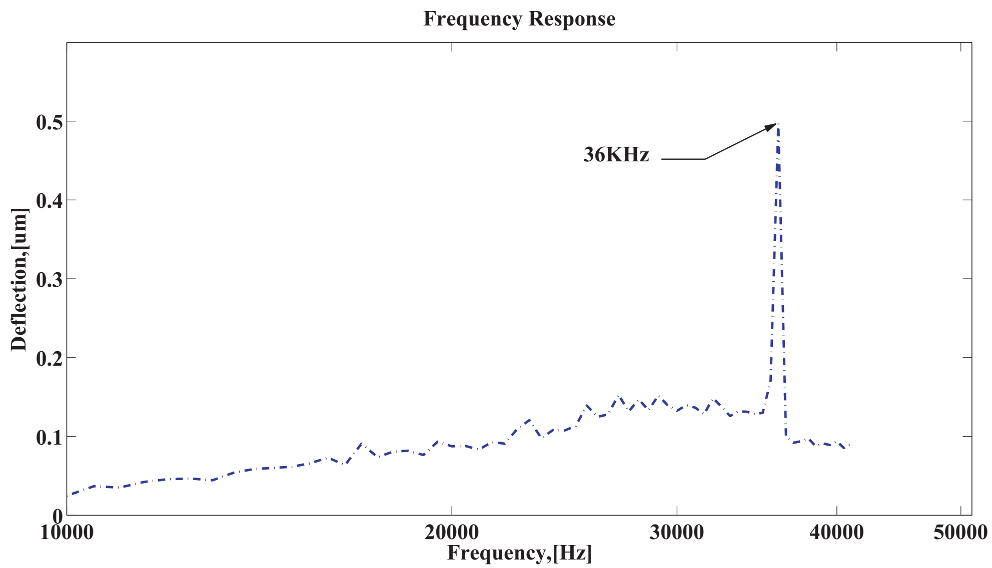

Figure 11. Frequency response of the MEMS logic gate. The resonant frequency is at around 36 kHz.

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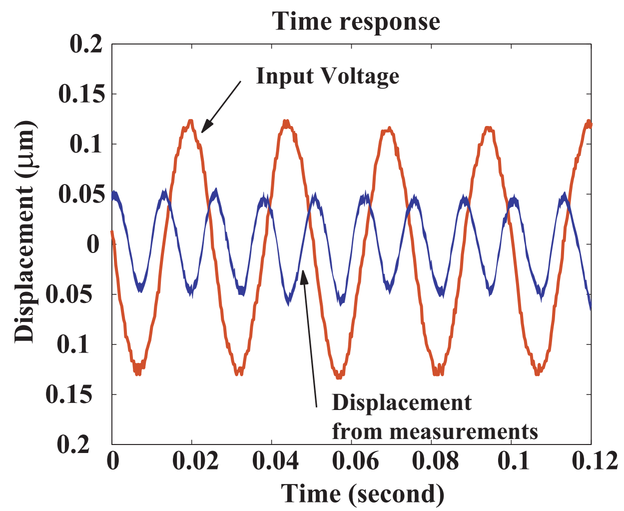

Figure 12. Time response of the MEMS logic gate. The input signal is 10 $\sin(2*10^3\pi t)$ V and the plate displacement is around 50 nm.

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