A CMOS 6-mW 10-bit 100-MS/s Two-Step ADC

Yung-Hui Chung and Jieh-Tsorng Wu
National Chiao-Tung University
Hsin-Chu City, Taiwan
Email: p9211830@alab.ee.nctu.edu.tw and jtwu@mail.nctu.edu.tw

***Abstract* — a 10-bit 100-MS/s two-step ADC was fabricated using a 90 nm CMOS technology. To reduce power dissipation, the ADC uses latch-type comparators for signal digitalization and an open-loop amplifier for residue amplification. The linearity of the residue amplifier is enhanced by digital background calibration. The resolution of the comparators is improved by analog offset calibration. The ADC consumes 6mW from a 1V supply. Measured SNR and SFDR are 58.2 dB and 75 dB respectively. Measured ENOB is 9.34b. The FOM is 100 fJ per conversion-step.**

I. INTRODUCTION

The transistors in nanoscale CMOS technologies are small and fast, but have low dc gain. Among analog building blocks, nanoscale transistors are more suitable to build latch-type comparators than to realize linear amplifiers. Thus, for high-speed medium-resolution (e.g. 10-bit) analog-to-digital conversion, the two-step architecture can offer power advantage against traditional pipelined ADCs.

Fig. 1 shows the proposed 10-bit two-step ADC architecture. To save power, there is no dedicated input sample-and-hold amplifier. The input track-and-hold function is provided by the switch-capacitor operation in the residue amplifier (RAMP) and coarse ADC (CADC). During ϕ_1=1, the V_1 input is sampled onto the C_S capacitor of the RAMP and also sampled onto the input capacitors of the comparators in CADC. During ϕ_2=1, the CADC compares the V_1 input with 33 V_{RC} references and generates the D_1 coarse code. The D_1 drives a resistor-string DAC (RDAC) to generate an estimate of V_1, denoted V_{da}. The difference between V_1 and V_{da} is amplified by the residue amplifier, RAMP. By the end of ϕ_2=1, RAMP's output, V_2, is digitized by the Fine ADC (FADC), generating the D_2 fine code. The FADC requires 65 V_{RF} references. The RAMP's voltage gain relaxes the accuracy requirement for the FADC. The FADC provides an extra input range of 32 LSB for over-range protection. Both the gain error and nonlinearity error of the RAMP are corrected by a digital calibration processor (CP). It receives the D_2 code and generates the corrected D_2^C code. Finally, an encoder combines D_1 and D_2^C to generate the 10-bit output code, D_O.

The use of a residue amplifier in the two-step A/D architecture [1] reduces the complexity of the RDAC switch box and relaxes the resolution requirement of the FADC. The power consumption of the RAMP is reduced by utilizing digital calibration. To reduce the power consumption of the CADC and FADC, the comparators are regenerative latches with offset calibration. The ADC is fabricated using a standard 90 nm CMOS technology and operated under a single 1 V supply. The differential input signal range is $2V_{P-P}$.

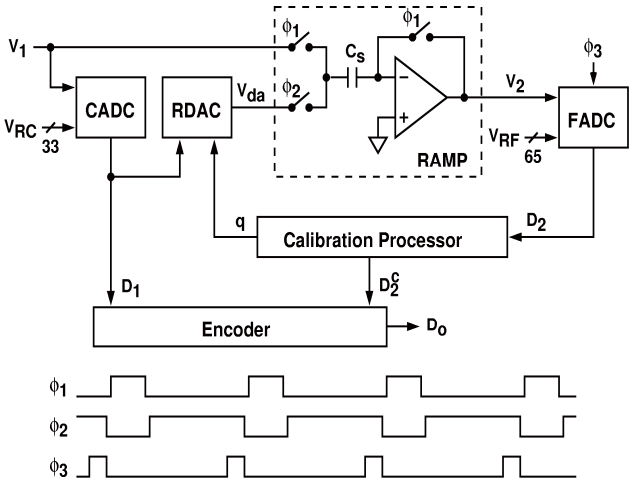

Figure 1. Architecture of the proposed ADC.

II. CIRCUIT DESIGN

A. Comparators

Both CADC and FADC are flash-type ADCs. The CADC comprises 33 comparators. The FADC comprises 65 comparators. A conventional comparator usually consists of a preamplifier followed by a regenerative latch. The gain of the preamplifier reduces the effect of the latch's offset. The preamplifier's offset can be reduced by either averaging or switched-capacitor operation. The comparator's power consumption is dominated by the preamplifier. In our design, the preamplifier is eliminated altogether.

Fig. 2 shows the schematic of the comparator for CADC. It is essentially a regenerative latch with an analog offset calibration (AOC) loop. Similar design is found in [2]. This comparator operates in two phases, i.e., calibration phase (ϕ_1) and comparison phase (ϕ_2). During ϕ_1=1, the V_1 input is sampled onto the C_1 capacitor and the latch input, V_a, is connected to a fixed common-mode voltage, V_{CM}. The latch then makes a comparison between V_a and V_b. The difference between V_a and V_b represents the equivalent input offset voltage of the comparator. The resulting D_C digital output is translated into an up or down pulse to charge or discharge the C_2 capacitor. The voltage on the capacitor, V_b, adjusts the

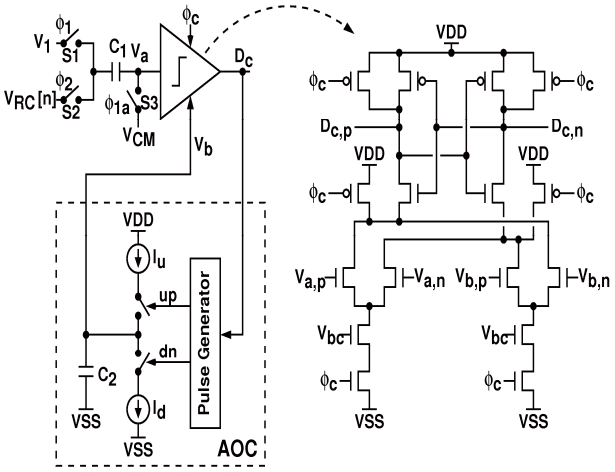

Figure 2. Schematic of the comparator in CADC

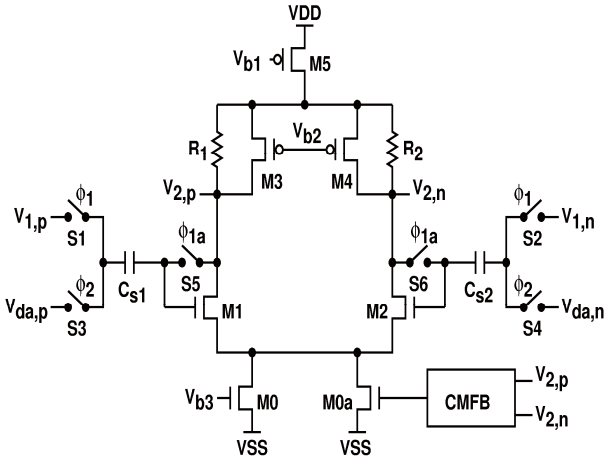

Figure 3. Schematic of the RAMP

equivalent input offset voltage of the latch. In our design, V_b is changed by an amount of 1/32 LSB every calibration cycle. During ϕ_2=1, the difference between V_1 and V_{RC}[n] is generated at the latch input, V_a. The latch then makes another comparison, yielding the CADC digital output, D_1. Including the AOC loop, this comparator consumes 18μW at 100 MHz sampling rate. Including the ROM digital output decoder, the total power consumption of the CADC is 0.8mW.

The comparators in the FADC are similar to those in the CADC, except they do not have the switched-capacitor track-and-hold input network, and they include three input source-coupled pairs connected to V_2, V_{RF}[n] and V_b, respectively. Each comparator in the FADC consumes 22μW. Including the ROM digital output decoder, the entire FADC consumes 1.7mW at 100 MS/s.

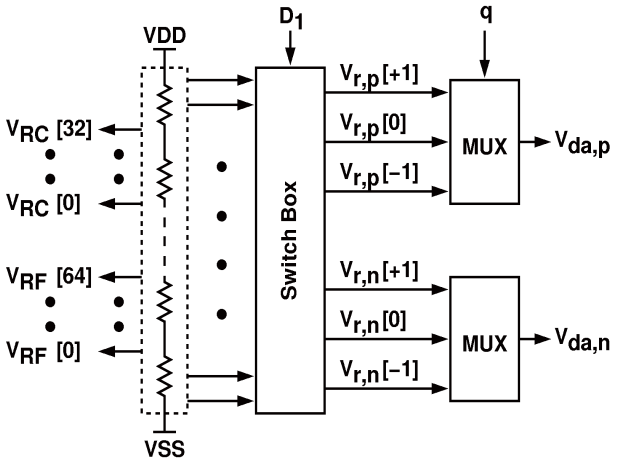

Figure 4. Block diagram of the RDAC.

B. Residue Amplifier (RAMP)

Fig. 3 shows the schematics of the RAMP. The RAMP is implemented as an open-loop differential amplifier [3]. To achieve the required linearity and speed, switches S1~S6 are constant-V_{gs} bootstrapped switches [4]. The input capacitors, C_{S1} and C_{S2}, have a capacitance of 250fF. During ϕ_1=1, the V_1 input is sampled onto the C_{S1} and C_{S2} capacitors. The amplifier is connected as a unity-gain feedback amplifier for input-offset cancellation. The input offset voltage of the RAMP is reduced to less than 2 LSB. It is necessary to keep the offset small. Large offset reduces the effective working input range of the FADC. During ϕ_2=1, V_1 is subtracted by the RDAC output, $V_{da,}$. The difference is then amplified by the RAMP. The RAMP provides a nominal voltage gain of 8, which is realized by the M1-M2 source-coupled pair and resistive loads, R_1 and R_2. Transistors M3 and M4 are biased in the saturation region. They function as current sources. Moreover, transistor M5 is added to improve the power supply rejection ratio of the RAMP. The RAMP consumes 1.1mW at 100 MS/s. The gain error and 3rd-order nonlinearity of the RAMP are corrected in the digital domain.

C. RDAC

Fig. 4 shows the functional block of the RDAC. The RDAC includes a resistor string that also generates the 33 V_{RC} references and the 65 V_{RF} references. The D_1 signal from the CADC controls a switch box that generates 3 sets of differential voltages: V_r[0], V_r[+1], and V_r[−1]. The V_r[0] signal is the nominal RDAC output corresponding to the D_1 input, while V_r[+1] is V_r[0]−1 LSB and V_r[−1] is V_r[0]+1 LSB. The q is a triple-valued random signal generated by the CP described below. Its value is among {0, +1, −1}. The final RDAC output is selected by q such that V_{da}=V_r[q]. This operation injects a random calibration signal into the RAMP. Its magnitude is among {0, +8 LSB, −8 LSB}. The RDAC consumes 1mW.

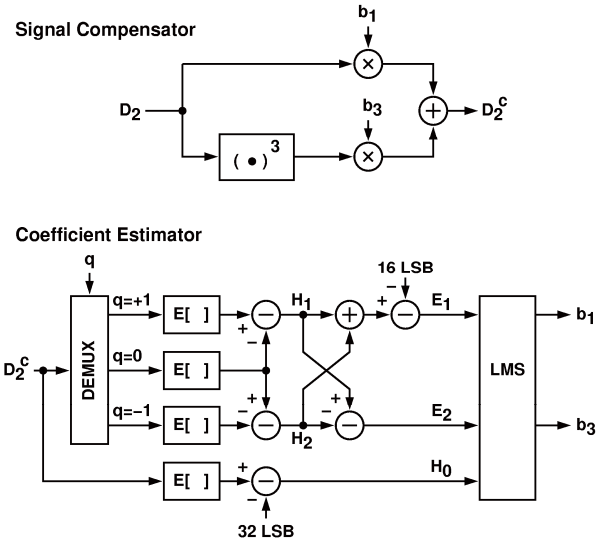

Figure 5. Block diagram of the Calibration Processor.

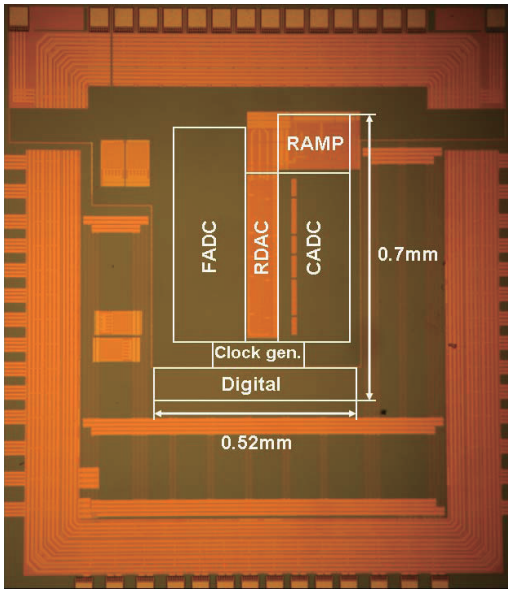

Figure 6. ADC chip micrograph.

D. *Calibration Processor (CP)*

The calibration processor shown in Fig. 5 is used to correct the gain error and 3rd-order nonlinearity of the RAMP. It consists of a signal compensator and a coefficient estimator. The signal compensator uses the 1st-order coefficient, b_1, and the 3rd-order coefficient, b_3, to correct the D_2 signal from the FADC, yielding the corrected D_2^C signal. The coefficient estimator generates the b_1 and b_3 coefficients without interrupting the normal ADC operation. The estimator averages the D_2^C data under different q conditions. The q sequence is generated from a pseudo random number generator. Based on the three different values of q, the output code D_2^C has relative code shifts. The H_1 is the difference between the averaged values of D_2^C when q=+1 and q=0. The H_2 is the difference between the averaged values of D_2^C when q=0 and q=−1. If the RAMP is ideal, the nominal value of H_1+H_2 is 16LSB and the nominal value of H_1-H_2 is 0 LSB. Deviations from the nominal values are denoted E_1 and E_2. The b_1 and b_3 coefficients are estimated from E_1 and E_2 by applying a least-mean-square (LMS) algorithm as follows:

$$b_1(k+1) = b_1(k) - \mu_1 \cdot \mathrm{sgn}(E_1 \cdot (16 \cdot b_1^3(k) - 5 \cdot b_3(k)) - 12 \cdot E_2 \cdot b_3(k) \cdot H_0) \quad (1)$$

$$b_3(k+1) = b_3(k) - \mu_3 \cdot \mathrm{sgn}(5 \cdot E_1 + 12 \cdot E_2 \cdot H_0) \quad (2)$$

where $\mu_1=1/256$ and $\mu_3=1/256$ are the step sizes for coefficient updating. H_0 is the difference between the average of all D_2^C data and the mid-code of the FADC (32 LSB). The calibration time, from the initial values to the settled values, is 2^{19} sampling periods, which is about 5ms at 100 MS/s.

The CP operates constantly in the background to perform calibration and real-time signal compensation. At 100 MS/s, it consumes 1mW.

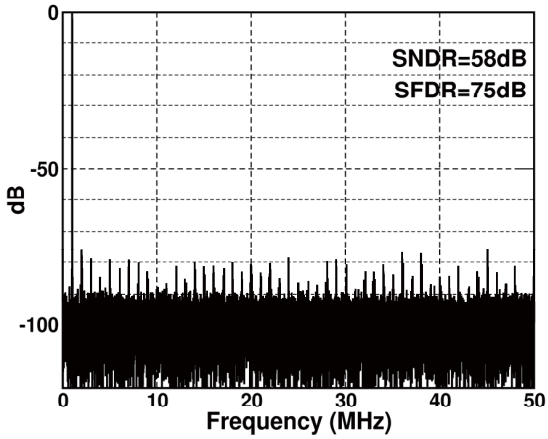

Figure 7. Measured FFT for Fin=1MHz at 100MS/s.

III. Measurement Results

Fig. 6 shows the micrograph of the ADC chip fabricated using a 1P6M 90nm CMOS technology. It occupies an area of 0.36mm^2. Operating at 100MS/s sampling rate, the ADC consumes 6mW of power from a 1 V supply. The dynamic performance of this converter is shown in Fig. 7. The input is a 1 MHz 2 V_{P-P} differential sinewave. The measured SNR, SFDR and SNDR are 58.2 dB, 75 dB and 58 dB respectively. When the input frequency is increased to 50 MHz, the measured SNR, SFDR and SNDR are 54 dB, 64 dB and 53.7 dB respectively. The measured dynamic performance versus input frequencies and sampling frequencies are shown in Fig. 8 and Fig. 9 respectively. The ERBW is about 46MHz. The measured DNL and INL are shown in Fig. 10 and Fig. 11 respectively. Without digital calibration, the measured DNL and INL are −1/+4 LSB and −17/+17 LSB respectively. When the digital calibration is enabled, the measured DNL

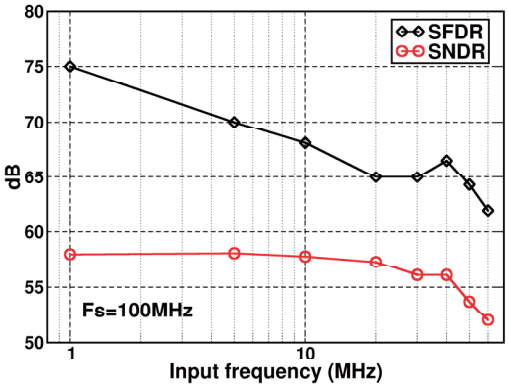

Figure 8. SNDR and SFDR versus input frequencies.

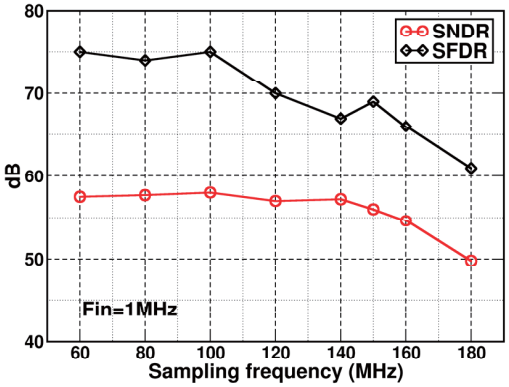

Figure 9. SNDR and SFDR versus sampling frequencies.

TABLE I. ADC PERFORMANCE SUMMARY

Resolution	10 bits
Sampling Rate	100 MS/s
Process	90nm 1P6M digital CMOS
Supply	1 V
Input Range	2.0 V_{PP} differential
DNL	-0.5/+0.6 LSB
INL	-0.9/+0.9 LSB
SNDR @ Fin=1MHz Fin=50MHz	58 dB 53.7 dB
SFDR @ Fin=1MHz Fin=50MHz	75 dB 64 dB
Total power	6 mW
CADC power FADC power RAMP power RDAC power Digital power	0.8 mW 1.7 mW 1.1 mW 1.0 mW 1.4 mW
FOM1 (Power/2^{ENOB}xFs) FOM2 (Power/2^{ENOB}x2ERBW)	92 fJ/conversion-step 100 fJ/conversion-step
Active Area	0.36 mm^2

and INL become −0.5/+0.6 LSB and −0.9/+0.9 LSB respectively. The ADC performance is summarized in Table I.

IV. CONCLUSIONS

A 10-bit 100-MS/s two-step ADC fabricated in a 90nm digital CMOS process is presented. It effectively takes advantage of the nanometer CMOS technology to achieve low power dissipation. Its internal coarse ADC and fine ADC are realized by latch-type comparators with automatic offset calibration. The gain error and nonlinearity of the residue amplifier is corrected in the digital domain. The ADC consumes only 6mW from a single 1 V supply. No external reference buffer is used.

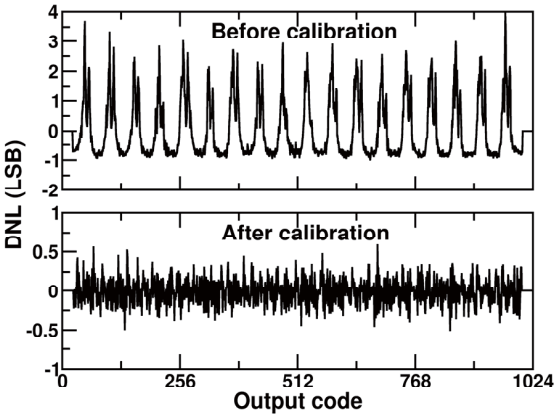

Figure 10. Measured DNL.

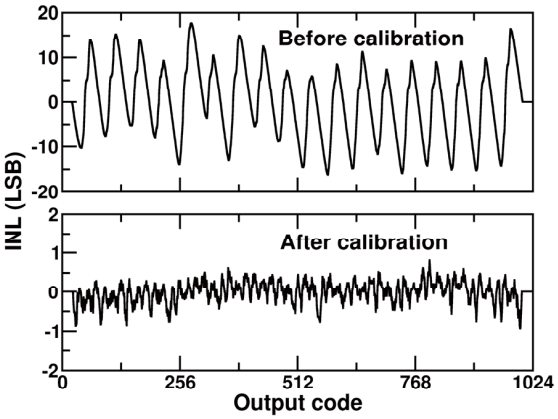

Figure 11. Measured INL.

ACKNOWLEDGMENT

The authors would like to thank Faraday Technology Corporation (FTC) for design assistance and chip fabrication.

REFERENCES

[1] H. van der Ploeg and R. Remmers, "A 3.3V, 10-b, 25-Msamples/s two-step ADC in 0.35µm CMOS," IEEE J. Solid-State Circuits, Vol. 34, No. 12, pp. 1803-1811, Dec. 1999.

[2] Z. Cao, S. Yan and Y. Li, "A 32mW 1.25GS/s 6b 26/step SAR ADC in 0.13µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 542-543, Feb. 2008.

[3] Murmann, B. and Boser, B. E., "A 12b 75 MS/s pipelined ADC using open-loop residue amplification," ISSCC Dig. Tech. Papers, pp. 328-329, Feb. 2003.

[4] M. Dessouky and A. Kaiser, "Very Low-Voltage Digital-Audio Delta-Sigma Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping," IEEE J. Solid-State Circuits, Vol. 36, No. 3, pp. 349-355, Mar. 2001.