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A Pseudo-Differential OTA with Linearity Improving by HD3 Feedforward

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***Abstract*—This paper presents a fully balanced structure of a CMOS operational transconductance amplifier (OTA) with high linearity for frequency up to 50MHz. The proposed circuit is based on a conventional pseudo-differential structure with a third-order harmonic distortion (HD3) feedforward technique to cancel out the output 3rd harmonic component. The OTA was fabricated in the TSMC CMOS 0.18µm technology. The measurement results show the HD3 of -62dB with 0.4-Vpp 50MHz input signal and the power consumption of 0.47mW at a 1.2-V voltage supply.**

I. Introduction

Integrated analog filters play important roles in present communication systems and system-on-chip (SOC) solutions. The most popular technique for realizing such an analog filter is a continuous-time filter, which can process high-speed signals continuously in time domain. There are three main techniques to implement an integrated continuous-time filter: 1) active-RC, 2) MOSFET-C and 3) Gm-C. The active-RC filter can provide very good linearity, but occupy enormous die area for resistors and capacitors. The configuration of MOSFET-C filter has poor linearity due to the nonlinearity characteristics of the MOS transistors.

On the other hand, the Gm-C filter is formed by the capacitors and operational transconductance amplifiers (OTAs) which are basic and important building blocks for various current-mode analog circuits and systems [1]-[3]. The Gm-C filter has a better frequency response than the active-RC and MOSFET-C structures because of the open-loop operation of the OTA. The performance of the Gm-C filter highly depends on the OTA building block, including the linearity and speed. Therefore, most researches focus on the linearity improvement in the voltage-to-current conversion blocks of this filter [4]-[7].

In an advanced CMOS process, short-channel effects influence the performance seriously, especially in linearity. Therefore, many compensation methods were proposed to improve linearity performance of a conventional OTA circuit. Mobility compensation [8] uses a well-sized weak-inversion transistor to compensate the short-channel effect. Besides, two out-of-phase transconductors with unequal Gm values can cancel the unwanted components of output signal [9]. However, the overall Gm may be reduced through this way.

In this paper, an HD3 feedforward technique is proposed for linearity improvement while a pseudo-differential (PD) topology is applied at the circuit level for low-voltage and high-frequency operations.

The basic circuit of a conventional pseudo-differential circuit is discussed in Section II. Section III describes the HD3 feedforward technique and circuit design of the modified pseudo-differential topology. The measured results are reported in Section IV. Finally, conclusions are addressed in Section V.

II. Conventional Pseudo-Differential OTA

Fig. 1 shows the basic schematics of the conventional PD and fully-differential structures. Compared with the fully-differential structure, the PD structure can be employed under a low supply voltage because it avoids the voltage drop across the tail current source and achieves a larger signal swing. However, the PD structure has an equal input common-mode gain (A_{CM}) as the input differentia-mode gain (A_{DM}), i.e., the common mode rejection ratio (CMRR= A_{DM}/A_{CM}) is unity, or

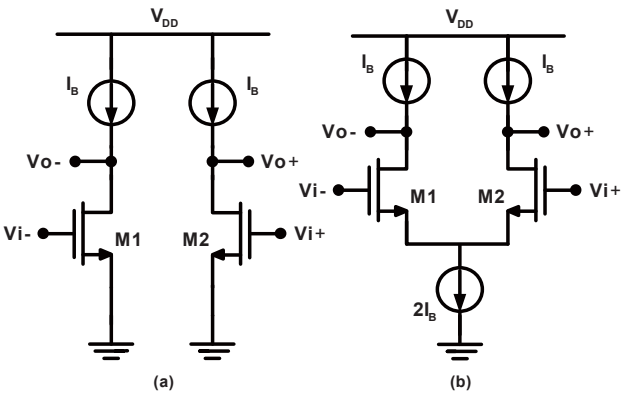

Fig. 1. Differential transconductors: (a) pseudo-differential (b) fully-differential topologies.

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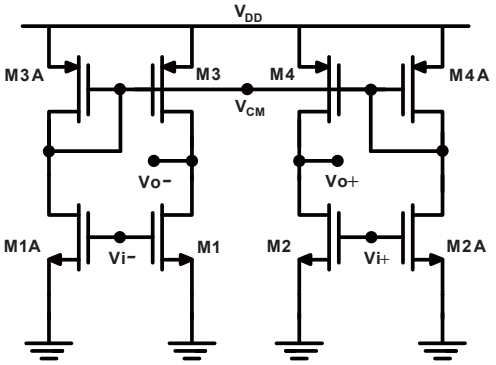

Fig. 2. Basic PD structure with a common-mode feedforward technique.

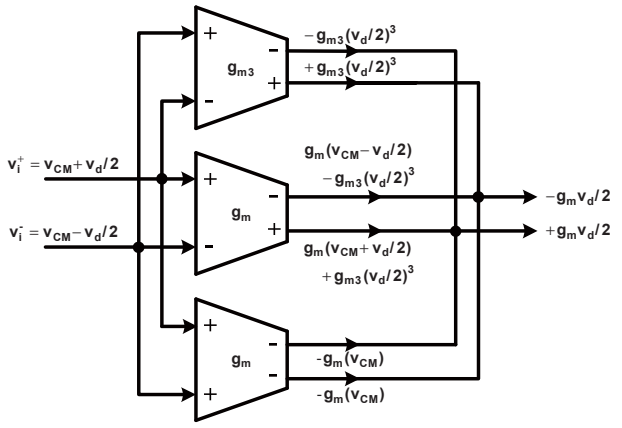

Fig. 3. Conceptual graph of an HD3 feedforward implementation.

zero dB in the logarithmic scale. Thus, a common-mode feedforward technique is needed for an input common-mode control or the OTA will suffer from a large common-mode variation at output [10]. The schematic of the PD structure with the common-mode feedforward technique is shown in Fig. 2. A common-mode component is generated through another path and mirrored to the output port through a current mirror; thus, the input common-mode signal can be cancelled. In this PD structure, the transistors M1A and M2A have the same aspect ratio as the transistors M1 and M2. Besides, the DC component of output current is removed by a feedforward path consisting of transistors M3 and M3A, M4 and M4A of the current mirrors. Assume the input V_{id} includes two parts: 1) V_C, and 2) V_d, which represent the common -mode and differential-mode signals, respectively. By derivation, the voltage signal at node V_{CM} will deliver the common-mode information of the input signal to the output. Considering the I-V characteristics of the transistor, the common-mode control voltage can be expressed as

$$V_{CM} = V_{DD} - \sqrt{(\beta_1/\beta_3)}(V_C - V_{TN}) + V_{TP} \quad (1)$$

where β is the design parameter of the transistor, and V_{TN} and V_{TP} are the threshold voltage of NMOS and PMOS, respectively.

Thus, the current mirror control voltage V_{CM} will be a DC-only signal while V_d is eliminated because the average of the PMOS gate voltage determined by current I_{D1A} and I_{D2A} will be detected.

From the ideal square-law equation under the saturation region, the output current is a linear function of the input voltage for a conventional pseudo-differential topology. However, the short-channel effect would cause nonlinear terms. According to the transistor model with short-channel effect, the third-order harmonic term can be expressed as

$$HD3 = \frac{\theta V_i^2}{8V_{OV}[1+\theta(V_{OV}-V_{tn})]^2[2+\theta(V_{OV}-V_{tn})]} \quad (2)$$

where θ is the mobility reduction coefficient and V_{OV} is the gate overdrive voltage of the input transistors M1 and M2, shown in Fig. 2.

III. PD OTA WITH HD3 FEEDFORWARD TECHNIQUE

In an ideal differential structure, all the even-order terms are cancelled. From the definition of total harmonic distortion (THD) illustrated in (3), we can find that the third order harmonic term (HD3) dominates the distortion performance. Thus, as we remove the HD3 term, the performance of THD will be suppressed dramatically without the cost of the overall transconductance and be dominated by the higher-order term which is much less than HD3.

$$THD = \frac{\sqrt{H_3^2 + H_5^2 + H_7^2 + ...H_N^2}}{H_1} \approx \frac{H_3}{H_1} \quad (3)$$

where H_N represents the amplitude of the N-th order harmonic tone of the signal and N is an odd number.

The proposed HD3 feedforward technique is based on the relation between THD and HD3 described above. In Fig. 3, the middle path is the original transconductor cell, the lower path is the common-mode feedforward path, and the upper path is the proposed HD3 feedforward path. Similar to the way of drawing out the common-mode component in the common-mode feedback system, an HD3 component can be obtained by the other signal path as well.

Fig. 4 shows the circuit schematic of the proposed pseudo-differential OTA with an HD3 feedforward technique, and transistors M1 to M4 are the input stage of the original OTA. With the same input Gm and power dissipation, twice the output current signal can be obtained by the cross-coupled output connections. The common-mode feedback circuit is also needed to stabilize the output common-mode voltage and feeds back a control voltage to the gate nodes of M5 and M7. The Gm tuning scheme can be achieved by the resistor R_{TUNE}, which is implemented by a transistor in the triode region and tuned by the gate voltage. The tunable resistor affects the effective resistance seen into the gate of M6 and M8. The current divided into r_{GS6} (r_{GS8}) will decrease as R_{TUNE}

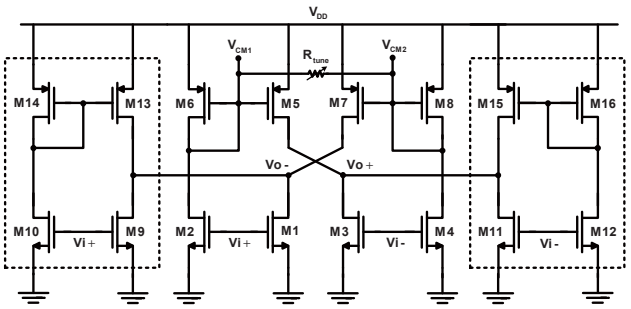

Fig. 4. Proposed PD transconductor with an HD3 feedforward technique.

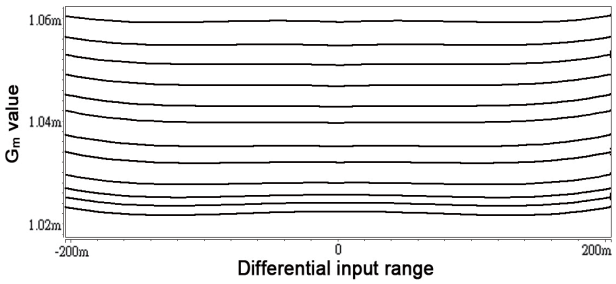

Fig. 5. Simulated Gm value with various tuning voltages.

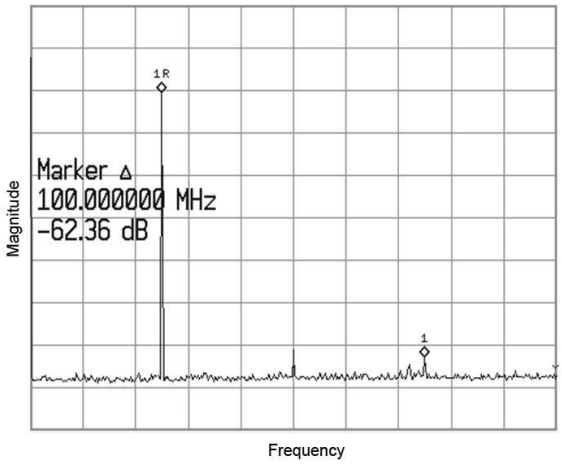

Fig. 6. Measured HD3 with 0.4-Vpp input signal at 50MHz.

decreases. And then the Gm decreases because the current reduces in M5 (M7) which is directly mirrored from M6 (M8), and vice versa.

The transistors M9 to M16 framed by dashed lines in Fig.4 are employed for an HD3 generation. The transistors M9 and M10 (M11 and M12) have unequal sizes. When the current of M10 (M12) is mirrored to M13 (M15) through M14 (M16), the current I_{D9} -I_{D10} (I_{D11}-I_{D12}) is obtained and delivered to the output. Ideally, the HD3 generator generates only HD3 but no HD1 which is the signal we want, or the overall Gm value will decrease. However, it is hard to reach such performance. The third-order term of the Taylor expansion of the output current from unmatched transistor pair, M9 and M10, with the short-channel effect can be expressed as

$$I_{D,3\text{-}rd} = \left[\frac{\beta_9 \theta}{16(1+\theta V_{OV9})^4} - \frac{\beta_{10} \theta}{16(1+\theta V_{OV10})^4} \right] V_{id}^3 \qquad (4)$$

The magnitude of $I_{D,3\text{-rd}}$ can be adjusted to the value of the 3-rd harmonic in the input stage by changing the size of M9 and M10. Meanwhile, some of the first-order term in Taylor expansion series is also generated as described in (5). This term degrades the Gm value of the original PD circuit.

$$I_{D,1\text{-}st} = \left[\frac{\beta_9 V_{OV9} - \left(\beta_9 \theta V_{OV9}^2\right)/(2+2\theta V_{OV9})}{2+2\theta V_{OV9}} - \frac{\beta_{10} V_{OV10} - \left(\beta_{10} \theta V_{OV10}^2\right)/(2+2\theta V_{OV10})}{2+2\theta V_{OV10}} \right] V_{id} \qquad (5)$$

When signals supply to input node Vi+ and Vi-, two signal paths will be constructed. One is the conventional PD transconductor with a common-mode feedback, which provides a main voltage-to-current conversion. The other one is the third-order harmonic term generator, which promotes the overall linearity. When the current of the two paths are summed at the output node, as shown in Fig.3, an output without HD3 component will be obtained.

IV. Simulation And Measurement Results

Fig. 5 shows the simulated transconductance value of the OTA with various tuning voltages. The Gm values are around 1.04mA/V. In the circuit-level post-layout simulation, about 20dB enhancement in HD3 can be obtained by the proposed HD3 feedforward technique as compared with the conventional PD OTA at 50MHz. This progress means the linearity of the proposed circuit is indeed improved. The measured result of the proposed circuit is shown in Fig.6. The magnitude level difference between the signal and third-order harmonic is -62.36 dB when an input signal is 0.4-Vpp at 50MHz. The second-order harmonic, which does not present in simulation, is observed in the measurement with a magnitude of -62 dB because of the process mismatch of CMOS fabrication.

The OTA was fabricated in the TSMC 0.18-μm CMOS process. The chip micrograph is shown in Fig. 7 with the active area less than 0.01 mm^2. The circuit operates at a 1.2-V supply with the power consumption of 0.47mW. Compared with other researches shown in table I, this OTA consumes very low power because of the elimination of the output stage and low power supply voltage; thus a power saving OTA is obtained.

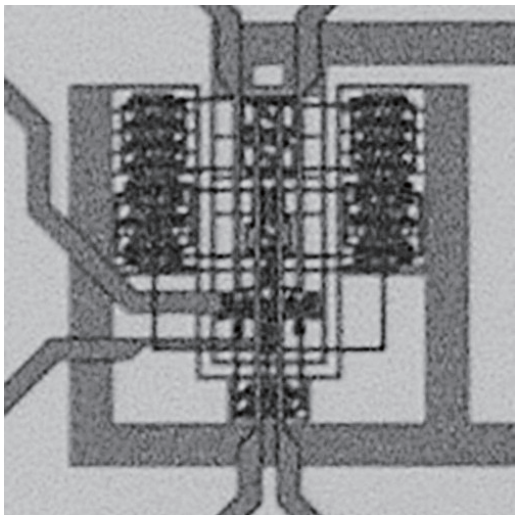

Fig. 7 Chip micrograph.

TABLE I.
PERFORMANCE SUMMARY OF THE OTA

Reference	[10]	[11]	This work
Technology	0.5-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Supply Voltage	3.3	1.5	1.2
Vin p-p	0.9V	0.9V	0.4V
HD3/IM3	-43dB HD3 @30MHz	-60dB IM3 @40MHz	-62dB HD3 @50MHz
Power Consumption	86mW*	9.5mW	0.47mW

*Filter constructed by 8 OTAs

V. CONCLUSIONS

This paper presents a design with a new concept of harmonic distortion feedforward technique. This concept is realized in a pseudo-differential structure. The HD3 generator feeds its HD3 to output and thus the HD3 of final output can be cancelled. The measured HD3 of the proposed OTA achieves -62 dB while the OTA consumes only 0.47mW.

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