IEEE Asian Solid-State Circuits Conference
November 16-18, 2009 / Taipei, Taiwan

A Micro-Network on Chip with 10-Gb/s Transmission Link

Wei-Chang Liu[(1)], Chih-Hsien Lin[(1)], Shyh-Jye Jou[(1)], Hung-Wen Lu[(2)], Chau-Chin Su[(2)], Kai-Wei Hong[(3)], Kuo-Hsing Cheng[(3)], Shyue-Wen Yang[(4)], Ming-Hwa Sheu[(4)]
Department of Electronics Engineering National Chiao Tung University[(1)]
Department of Electrical and Control Engineering National Chiao Tung University[(2)]
Department of Electrical Engineering National Central University[(3)]
Graduate School of Engineering Science & Technology National Yunlin University of Science & Technology[(4)]

***Abstract*—In this paper, a micro-network on chip (MNoC) with 10-Gb/s transmission link is proposed. A prototype system with two 5-port packet-based on-chip micro-switches and a 10-Gb/s data transceiver with an all digital data recovery circuit and a self-calibration clock generator are designed. This chip is implemented in 0.13µm CMOS technology. The core area of this chip is 990µm*1600µm and the power consumption is 155mW (60mW for micro-switches and 95mW for 10-Gb/s data transceiver) at 1.2V supply voltage with 10-Gb/s transmission data rate.**

I. Introduction

As a result of the advancement in process and design technologies, more than 100 million transistors are now able to be integrated in a single chip. Therefore, many different functional IPs (Intellectual Property) integrated in a SoC is a trend. Unfortunately, the communication between the IPs becomes a critical problem due to the limited bus bandwidth.

Recently, the concept of MNoC (Micro-Network on Chip) [1] is proposed to conquer the limitation of on chip bus bandwidth. MNoC uses the package-based transmission, similar to network, to transfer the data between IPs on chip. The issues of arbitration fairness, hardware cost and time delay are the major consideration while designing a usable router (or switch) in MNoC. In this paper, a distributed and fair crossbar scheduling algorithm is adopted. It not only contains arbitration fairness, has less latency but also consumes lower power than other traditional distributed or centralized ones.

Besides, in SoC transmission links, the serial transmission method has lower area and achieves higher speed than the parallel ones. An all digital serial link 10-Gb/s data transceiver is also proposed and integrated in the MNoC system. It includes serializer [2], deserializer, LVDS driver [3-4], RX front end and 2.5-GHz 8-phase PLL [5], which provides 2.5-GHz 8-phase clock signal to the system. An illustration of MNoC with 10-Gb/s transmission link is shown in Fig. 1.

This paper is organized as following: a MNoC switch with fast fair crossbar scheduler is described in section II. Next, a low jitter self-calibration PLL and a 10-Gb/s data transceiver with an all digital data recovery circuit are shown in section III. In section IV, an integrated test chip of MNoC with 10-Gb/s transmission link will be described. The experiment result of the proposed architecture is shown in section V. Finally, a conclusion is given in section VI.

II. Micro-Network on Chip Switch with Fast Fair Crossbar Scheduler

A high-speed, area efficiency and low power crossbar

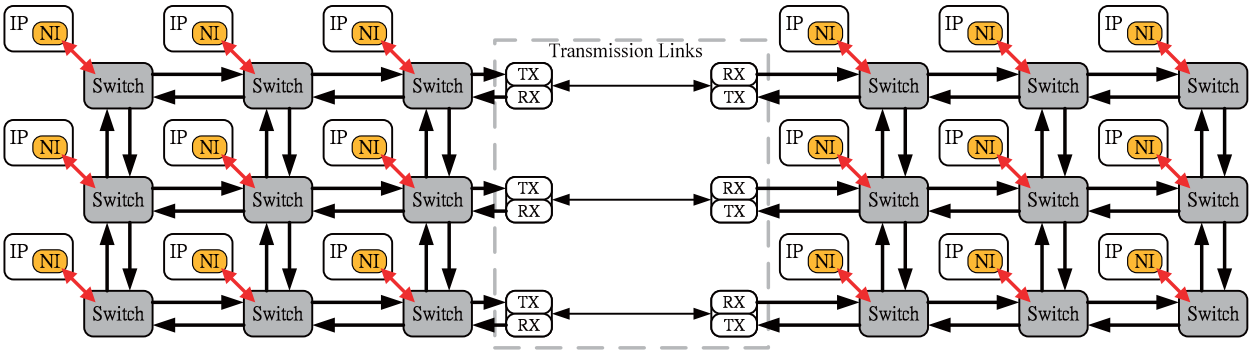

Fig. 1. An illustration of micro-network on chip with 10-Gb/s transmission links.

This work was supported by the Ministry of Economic Affairs under Contract MOEA95-EC-17-A-01-S1- 037 of Taiwan.

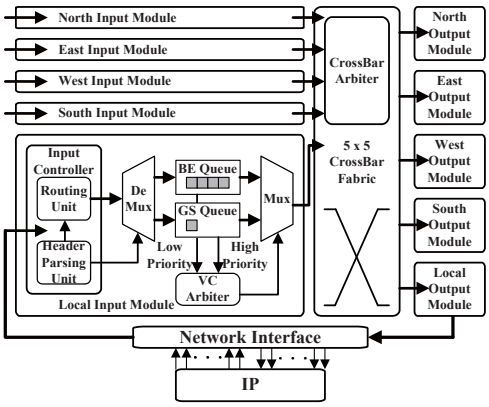

Fig. 2. 5-Port MNoC Switch Architecture.

switch for on-chip network was proposed. Fig. 2 shows the architecture of proposed 5-port MNoC switch.

A. Micro-Network on Chip Switch Architecture

The 5-port switch includes five input and output modules. The local port communicates with the IP by way of NI (Network Interface). Each input module contains an input controller, MUX, DeMUX, a BE (Best Effort Service) queue, a GS (Guarantee Service) queue, a VC arbiter used to decide which flit in queues can pass the MUX, a 5x5 crossbar and crossbar scheduler. Also, a handshaking module is designed in the output modules to prevent the dead lock loop.

B. Fair Arbitration Algorithm

When the switch received a package, the input controller will first decode the header of package to decide the transmission direction. The header also contains the service information of the package. After decoding, the header parsing unit assigns the BE packages to BE queue and GS packages to GS queue. The VC arbitrator will give GS packages a higher priority and transmit the GS packages from GS queue first and then transmit BS packages from BS queue.

For scheduling, a fair distributed arbiter is proposed. It combines the advantages of the centralized and the distributed arbiters. It provides fair arbitration scheme, lower area cost and lower latency. In order to improve the disadvantage of unfair arbitration of traditional distributed arbiter, a MC (Mask Circuit) is added as proposed in the previous work [1].

C. FPGA Demo System

Fig. 3 shows the MNoC switches verification environment on FPGA. The MNoC was verified running at 325-MHz system clock with 32 parallel lines, which achieves more than 10-Gb/s data rate. Fig. 4 demonstrates a real time image system using the proposed MNoC switches on two FPGA boards to perform the MNoC transmission system.

III. 10-Gb/s Data Transceiver

For the situation to connect two far away switch networks on chip, a serial transmission is a better policy than the parallel one as a result of comparing to the connection area cost. Therefore, this paper also proposes a 10-Gb/s data

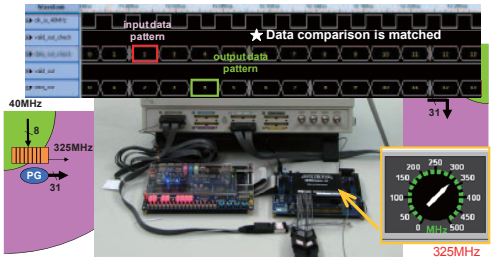

Fig. 3. MNoC Switches Measurement Resutl using FPGA.

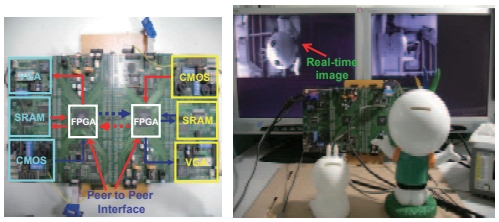

Fig. 4. System Demo of MNoC Switches on FPGA.

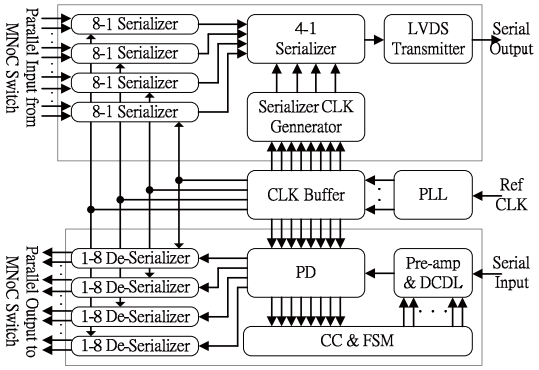

Fig. 5. 10-Gb/s Data Transceiver Architecture.

transceiver module as the serial transmission link to overcome the situation. In our previous works [4-5], the components of 10-Gb/s data transceiver were presented. The data from MNoC switch is processed by the parallel scrambler and then be framed for synchronization and transmitted in the PHY layer. Then after the serializer, the data is transformed into 10-Gb/s data rate. The data is then transmitted by serial link transmitter. After the on chip transmission line, the RX front-end received the data. The 10-Gb/s data is transformed into 312.5-Mb/s parallel data of 32 lines. Then the data transmitted into the MNoC switch. The architecture is shown in Fig. 5.

A. Low Jitter Self-Calibration PLL

The PLL module adopts the multi-band voltage control oscillator (VCO) with self-calibration circuit [5]. The VCO is a ring oscillator type for area saving. It also provides low KVCO for reducing P/G and substrate noise effect. The SCC (Self-Calibration Circuitry) is used to control the multi-band VCO and make the output frequency to cover PVT variations in 2.5-GHz. The VCO circuit uses symmetry load architecture delay cells, which maintain relatively steady swing of signal, reduce sensitivity to power supply noise and provide a wide operating frequency range.

Overall, this self-calibration PLL provides low jitter performance and 2.5-GHz 8-phase clock signal to the system.

B. Serializer and LVDS I/O

The tree-topology serializer [2] using a multiphase low-frequency clock is normally applicable to single-stage MUXs only. By multiplexing only two inputs, the parasitic effects at each stage are minimized. Therefore, the jitter caused by process variation and ISI is reduced, and the data rate is increased.

The pre-driver and pre-amplifier [3] are able to achieve a high scalability with different cell libraries, technologies, and supply voltages. The proposed inductive biasing circuit raises the bandwidth and reduces the ground noise. Related small-signal model analysis helps adjust the peaking effect. The adopted digital LVDS drivers with orderly turned-on and duty cycle adjustment methods are effective for SSN reduction [4]. The programmable drivers are applied to solve a process variation problem and to obtain an expected offset and swing. Furthermore, by merging the 100Ω differential termination resistance into the driver, the power consumption is reduced by half.

C. Deskew Buffer

It features a digital delay cell schemes and optimized logic functions to improve the data rate and reduces hardware overhead. With an identical architecture, the digital delay can operate at high data rate while with amplifying low-swing differential inputs. Besides, the critical path of the programmable digital loop filter and the phase-control FSM both are optimized with the pseudo-N logic gates and the combinational logic function. It results in a low loop latency and the circuit sizes is thus greatly reduced. Besides circuit level improvement, the system level parameters including the frequency tolerance and the loop bandwidth and tracking time are predicted by equation.

IV. MICRO-NETWORK ON CHIP WITH 10-GB/S TRANSMISSION LINK CHIP INTEGRATION

An experimental chip is integrated to realize the concept of MNoC transmission with 10-Gb/s transmission link and prove the performance of the proposed circuits. The proposed MNoC with 10-Gb/s transmission link architecture is presented in Fig. 6. It contains two 5-port MNoC switches and a 10-Gb/s data transceiver module. With additional MUX circuits, this architecture provides 8 testing modes, which including the switch testing mode, 10-Gb/s data transceiver testing mode and MNoC with 10-Gb/s transmission link testing mode, to verify the design.

As a result of the pad limited design, this experimental chip provides 1 data input pin and 1 data output pin, both of them are MSB of the 32-bits switch I/O, for functional observation. In order to gain the observability and controllability, three assistant modules, BA (Byte Aligning) module, 1 to 32 SR (Shift Register) module, PG (pattern generator) module are added.

The byte aligning module is designed to detect and correct the rotation and delay of the received data caused by the P2S

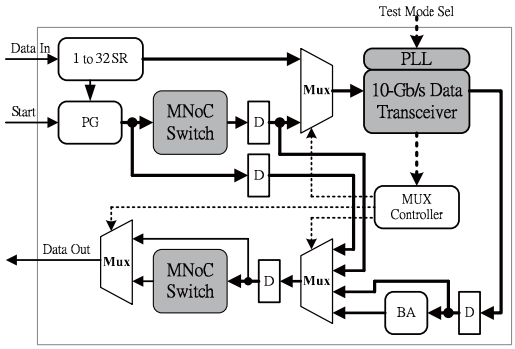

Fig. 6. Architecture of 10-Gb/s on Chip Transmission Link Test Chip.

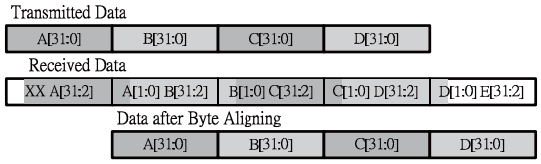

Fig. 7. Byte Aligning Operation.

and S2P processes. As Fig. 7 shows, the received data is not guaranteed to be aligned; therefore by using the pre-defined preambles to train the BA to detect and recover the transmitted data is necessary. Also, a 1 to 32 SR is added to provide 32-bits data input for 10-Gb/s data transceiver in 10-Gb/s data transceiver testing mode.

For MNoC with 10-Gb/s transmission link testing mode, the PG module provides MNoC training preamble and 31-bits random pattern combing with the 1-bit input data to generate the 32-bits input data for MNoC switch. In order to verify the NMoC function, the data is sent to the northern port of the upper switch, then the output data from eastern port will transmitted by the 10-Gb/s data transceiver. After byte aligning, the transmitted data will be sent to the western input port of the lower switch. Finally, the data from the eastern output port will be observed to verify the system function.

V. EXPERIMENT RESULT

The proposed MNoC with 10-Gb/s transmission link has been realized in 0.13μm standard CMOS technology. The chip area is 1.584mm^2; including two MNoC switches, 10-Gb/s data transceiver, PLL, 1 to 32 SR, PG and BA, and I/O pads. The active area of MNoC switches and assistant modules is 0.52mm^2 and the 10-Gb/s data transceiver with PLL occupies 0.36mm^2.

The die photo, PCB including the chip and measurement set up is shown in Fig. 8. The measured input data and output data waveform are shown in Fig. 9. The "Agilent 81130A Pattern Generator" generates two reference clocks, one for PLL and the other for "Agilent N4901B Serial BERT". After BERT, a synchronized clock for digital domain, a PLL reference clock and 1-bit random pattern data were sent to the chip under measurement. The input data and output data were measured and displayed by "Agilent 54832D Infiniium MSO". In summary, the power consumption of the total chip is 155mW, operation at 312.5-MHz clock frequency and 10-

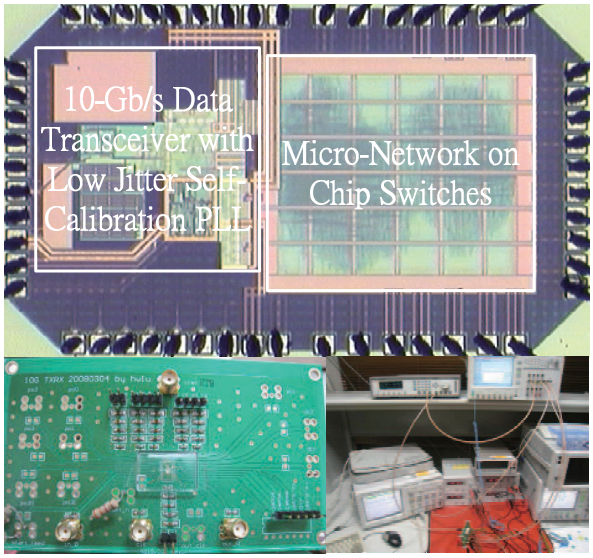

Fig. 8. Die Photo of MNoC with 10-Gb/s Transmission Link Test Chip and Measurement Enviroment.

Gb/s transmission rate. The power dissipation of MNoC switches and assistant modules is 60mW and the 10-Gb/s data transceiver with self-calibration PLL consumes 95mW. The experiment results are listed in Table 1. The comparison of the 10-Gb/s data transceiver is listed in Table 2.

VI. CONCLUSIONS

In this paper, a high-speed, area efficiency and low power crossbar switch for on-chip interconnection network is proposed and designed with distributed scheduling algorithm. A 10-Gb/s transceiver with all-digital SerDes scheme for multi-channel on-chip interconnects is presented.

Overall, a MNoC with 10-Gb/s transmission link chip is implemented. Also the data rate of the chip is verified to achieve 10-Gb/s at 312.5-MHz clock rate. This chip area is 1.584mm^2 with 155mW power consumption.

ACKNOWLEDGMENT

The authors thank National Chip Implementation Center (CIC), Taiwan, for technology supports and chip implementation.

TABLE I. EXPERIMENT RESULT.

Name	10-Gb/s on Chip Transmission Link	
Process	0.13um 1P8M	
Sub-Block	MNoC Switches	10-Gb/s Data Transceiver
Measured Operation Frequency	>312.5-MHz	10-Gb/s
Power Consumption	60mW	95mW
Total Power	155mW @1.2V	
Area	0.52 mm^2	0.36 mm^2
Total Area	1.584 mm^2 (990um*1600um)	

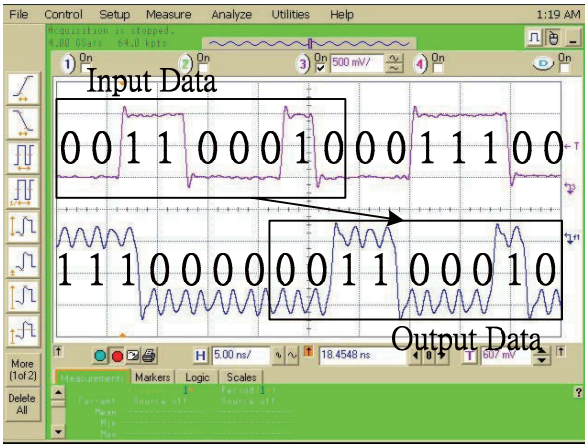

Fig. 9. Measured I/O Data Waveform of MNoC with 10-Gb/s Transmission Link.

TABLE II. COMPARISON TABLE OF 10-GB/S DATA TRANSCEIVER.

Reference	Speed (Gb/s)	Tech. (um)	Power (mW)	Area (mm^2)	Normalized Power (mW/Gb)
This work	10	0.13	95	0.12 (Core)	9.5
ISSCC 08 [6]	10	0.13	165	0.6 (Chip)	16.5
CICC 08 [7]	9	0.13	400	0.7 (Core)	44.4
VLSI 07 [8]	5-15	0.065	36@ 10G	-	3.6
ISSCC 05 [9]	0.6-9.6	0.13	152@ 6.25G	0.56 (Core)	23.3

REFERENCES

[1] S.W. Yang, M.H. Sheu, C.K. Yeh, C.Y. Wen, C.C. Lin, and W.K. Tsai, "Fast Fair Crossbar Scheduler for On-chip Router," IEEE International Symposium on Circuits and Systems, pp. 385-388, May 2007.

[2] H.W. Lu, C.C. Su, and C.N. Liu, "A Tree-Topology Multiplexer for Multiphase Clock System," IEEE Transactions on CAS I, Vol.56, Issue.1, pp.124-131, January 2009.

[3] H.W. Lu, C.C. Su, and C.N. Liu, "A Scalable Digitalized Buffer for Gigabit I/O," IEEE Transactions on CAS II, Vol.55, Issue.10, pp.1026-1030, October 2008.

[4] H.W. Lu, H.W. Wang, C.C. Su, and C.N. Liu, "Design of an All-Digital LVDS Driver," Accepted by IEEE Transactions on CAS I.

[5] K.H Cheng, Y.C Tsai, K.W Hong, and Y.H Wu, "A low jitter self-calibration PLL for 10Gbps SoC transmission links application", IEEE International Conference on Electronics, Circuits and Systems, pp. 786-789, Aug 2008.

[6] J.Y. Park, J. Kang, S.H. Park, M.P. Flynn,"A 9Gbit/s Serial Transceiver for On-chip Global Signaling over Lossy Transmission Lines," in Proc. of CICC, pp.347- 350, Sept. 2008.

[7] A. Lin, M. Loinaz, "A Serial Data Transmitter for Multiple 10Gb/s Communication Standards in 0.13µm CMOS," in IEEE ISSCC Dig. Tech. Papers, pp.108-599, Feb. 2008.

[8] G. Balamurugan, J. Kennedy, G. Banerjee, J.E. Jaussi, M. Mansuri, F. O'Mahony, B. Casper, R. Mooney, "A Scalable 5-15Gbps, 14-75mW Low Power I/O Transceiver in 65nm CMOS," in Sym. VLSI Circuits Dig. Papers, pp.270-271, June 2007.

[9] Krishna, K. et al, "A 0.6 to 9.6Gb/s binary backplane transceiver core in 0.13µm CMOS," in IEEE ISSCC Dig. Tech. Papers, pp.64-585, Feb. 2005