A 62.8 mW 4×4 MIMO-OFDM Modem with One-Symbol-Locked Timing Recovery, Frequency-Dependent I/Q Mismatch Estimation and Adaptive Equalization

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***Abstract*—A 4×4 multi-input multi-output (MIMO) orthogonal frequency-division multiplexing (OFDM) modem with one-symbol-locked timing recovery, anti-I/Q mismatch frequency recovery, frequency-dependent I/Q mismatch estimation and adaptive equalization is implemented in 0.13-μm CMOS library. This chip occupies 4.6×4.6 mm^2 and consumes 62.8 mW at 1.2 V.**

I. Introduction

The combination of multi-input multi-output (MIMO) transmission, orthogonal frequency-division multiplexing (OFDM) technology, and space-time block code (STBC) scheme comprises a potential solution for next-generation wireless communications [1]. However, MIMO-OFDM systems are sensitive to sampling clock offset and carrier frequency offset (CFO). In addition, direct-conversion receivers suffer from I/Q mismatch (IQM). IQM arises when the phase and gain differences between I and Q branches are not exactly 90° and 0 dB, respectively. Due to the impairment in the analog components, the mismatched low-pass filters result in frequency-dependent IQM (FD-IQM) [2]. In an MIMO-OFDM system with FD-IQM, the FD-IQM parameters for every subcarrier are different. Moreover, the ability of adaptive equalization is required due to time-varying environments. For successful transmissions, obtaining accurate channel frequency response (CFR) is extremely important. Owing to the above considerations, an MIMO-OFDM modem is proposed for fast timing recovery, anti-IQM frequency recovery, FD-IQM estimation and adaptive frequency-domain equalization.

II. System Overview

Fig. 1 shows the block diagram of 4×4 STBC MIMO-OFDM modem and the packet format. In Table 1, key parameters of this system are summarized. This system operates at 2.4 GHz band with 20 MHz bandwidth. In the transmitter, all the transmit chains uses the same oscillator as well as in the receiver. The first part of the packet consists of legacy training sequence identical to IEEE 802.11a/g. The second part of the packet is the high throughput (HT) training sequence identical to IEEE 802.11n. The receiver uses the preambles to complete packet detection , synchronization, and channel estimation. The CFO estimation is summed over all receive chains and applied to all received signals. A preamble-assisted estimation is applied to circumvent the FD-IQM with CFO. To equalize the CFR of the time-varying environments, this receiver applies an adaptive equalizer in conjunction with the STBC decoder. Spatial streams are then demodulated to bit-level streams, which are de-interleaved and merged into a data stream. Finally, the data stream is decoded by the forward error correction (FEC) decoder.

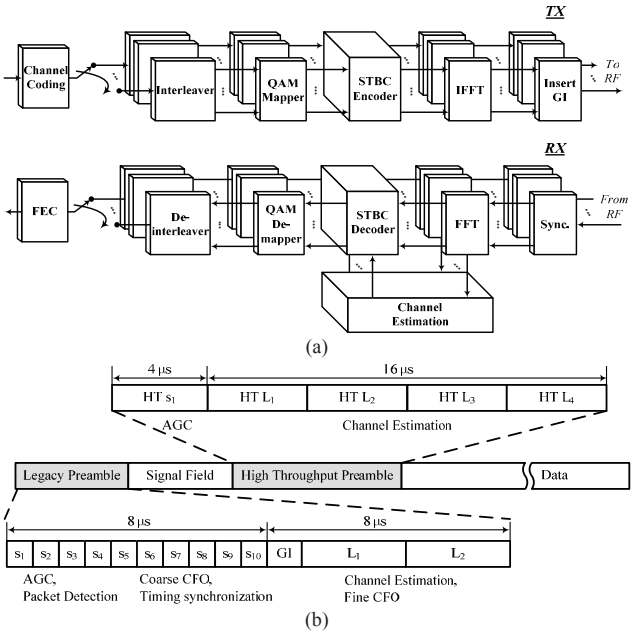

Fig. 1. (a) Block diagram of the 4×4 MIMO-OFDM system. (b) Packet format.

TABLE I
System Parameters

RF Frequency	2.4 GHz
Signal bandwidth	20 MHz
# of data carriers	52
FFT size	64
Modulation	BPSK, QPSK, 16-QAM, 64-QAM
Subcarrier spacing	312.5 KHz
Symbol duration	4 μs

III. Architecture and Circuit Design

The receiver architecture is shown in Fig. 2, consisting of four major parts: timing recovery, frequency recovery, FD-IQM estimation and adaptive equalization.

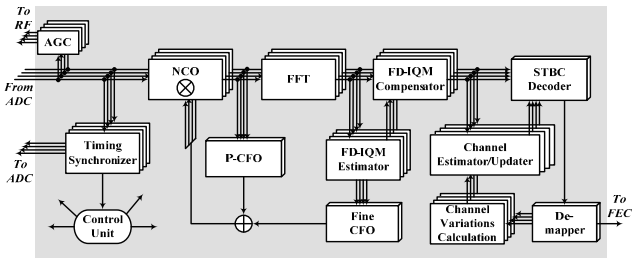

Fig. 2. Block diagram of the 4×4 MIMO-OFDM receiver.

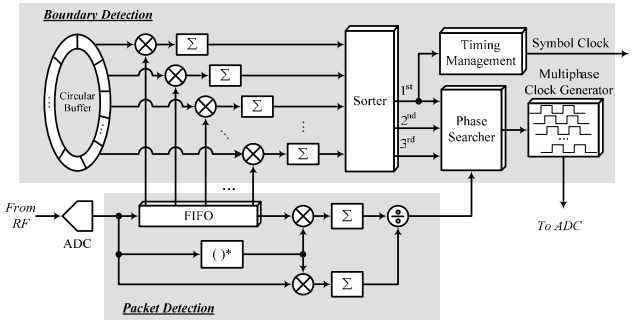

Fig. 3. Architecture of the timing synchronizer.

A. One-Symbol-Locked Timing Recovery

Fig. 3 shows the proposed timing recovery circuit. The synchronization includes packet detection and boundary detection. For packet detection, auto-correlation method is applied to determine the signal. Due to multiple receive antennas, correlation functions are summed over all the antennas to maximize detection performance. To perform the boundary detection, the modem then correlates the received signal with ideal short preamble. With the parallel cross correlation, the correlation power is obtained to indicate the symbol boundary index. The phase searcher then works in conjunction with a 22-phase multiphase generator to lock the optimal phase in one symbol period.

B. Anti-I/Q Mismatch Auto-Frequency Controller

Since the simultaneous occurrence of CFO and IQM significantly degrades the system performance, an anti-IQM auto frequency controller is developed by the pseudo CFO (P-CFO) technique [3]. The P-CFO algorithm rotates three training symbols by adding extra frequency offset into the received training sequence to improve CFO estimation. The purpose of extra CFO is to resolve the transformation error resulting from noise disturbances. Let s_i and $\Delta\theta$ be the rotated short preambles and the pseudo offset, respectively. The CFO Δf can be obtained as follows (please refer to [3] for detailed derivation),

$$\Delta f = \frac{1}{2\pi N_s T_s}\cos^{-1}\left(\frac{\mathrm{Im}\{s_3\}\mathrm{Re}\{s_1\}-\mathrm{Im}\{s_1\}\mathrm{Re}\{s_3\}}{\mathrm{Im}\{s_2\}\mathrm{Re}\{s_1\}-\mathrm{Im}\{s_1\}\mathrm{Re}\{s_2\}}\right)-\Delta\theta \tag{1}$$

where N_s and T_s denote the samples of a short preamble and the sampling period, respectively.

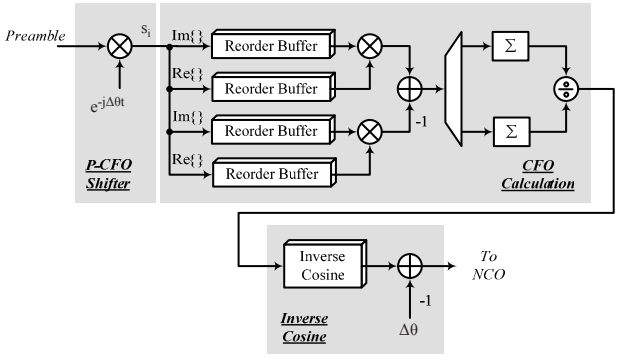

Fig. 4. Architecture of the anti-I/Q mismatch auto-frequency controller.

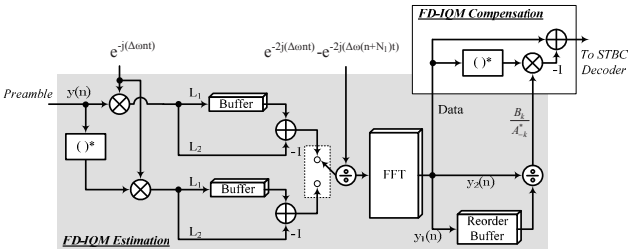

Fig. 5. Architecture of the frequency-dependent I/Q mismatch estimator.

Fig. 4 shows the P-CFO architecture. The P-CFO is comprised of P-CFO shifter, CFO calculation and inverse cosine. When preambles are arrived, P-CFO shifter module multiplies the received preambles by additional pseudo offset. CFO calculation module then uses these rotated preambles to do correlation. After CFO calculation, the result is sent to inverse cosine look-up table. Inverse cosine module finds the angle, and removes the pseudo offset to extract the final CFO.

C. Frequency-Dependent I/Q Mismatch Estimation

Let $r(n)$ and $w(n)$ be the received signal and additive white Gaussian noise, respectively. The baseband signal with CFO Δf and FD-IQM is given by [2], [4]

$$\begin{aligned} y(n) = &\left((\alpha\psi(n)+\beta^*\xi(n))\otimes r(n)\right)e^{j2\pi\cdot\Delta f\cdot nT_s} \\ &+\left((\beta\psi(n)+\alpha^*\xi(n))\otimes r^*(n)\right)e^{-j2\pi\cdot\Delta f\cdot nT_s}+w(n) \end{aligned} \tag{2}$$

where α and β denote the constant IQM parameters, $\psi(n)$ and $\xi(n)$ represent the FD-IQM parameters. The symbol "$\otimes$" represents the convolution operator. Fig. 5 depicts the architecture of FD-IQM estimator. The basic strategy for extracting IQM parameters is to employ long preambles. Let $x(n)$ and $x(n+N_l)$ represent two consecutive long preambles, as defined in (2), where N_l is the samples of a long preamble. Firstly, two long preambles are multiplied by the estimated CFO. To reduce the image interference due to the IQM effect, the first long preamble subtracts the second long preamble. At the same time, the conjugate preamble follows the same procedure described above. Because the long preambles are periodic, the received signals, $r(n)$ and

$r(n+N_l)$ is replaced by $r(n)$. Therefore, the following equations hold:

$$y_1(n) = \frac{x(n)e^{-j(2\pi\Delta fnT_s)} - x(n+N_l)e^{-j(2\pi\Delta f(n+N_l)T_s)}}{e^{-2j(2\pi\Delta fnT_s)} - e^{-2j(2\pi\Delta f(n+N_l)T_s)}} \quad (3)$$
$$= (\beta\psi(n) + \alpha^*\xi(n)) \otimes r^*(n)$$

$$y_2(n) = \frac{x(n)^* e^{-j(2\pi\Delta fnT_s)} - x(n+N_l)^* e^{-j(2\pi\Delta f(n+N_l)T_s)}}{e^{-2j(2\pi\Delta fnT_s)} - e^{-2j(2\pi\Delta f(n+N_l)T_s)}} \quad (4)$$
$$= \left((\alpha\psi(n) + \beta^*\xi(n)) \otimes r(n)\right)^*$$

The IQM parameters can be obtained as follows.

$$\frac{B_k}{A_{-k}^*} = \frac{\mathrm{FFT}_N\left\{y_1(n)\right\}}{\mathrm{FFT}_N\left\{y_2(n)\right\}} \quad (5)$$

With the estimated IQM parameters, the frequency-domain compensation is given by

$$\mathrm{FFT}_N\left\{x(n)e^{-j(2\pi\Delta fnT_s)}\right\} - \frac{B_k}{A_{-k}^*}\mathrm{FFT}_N\left\{x^*(n)e^{-j(2\pi\Delta fnT_s)}\right\}$$
$$= \underbrace{\left(A_k - \frac{B_k B_{-k}^*}{A_{-k}^*}\right)}_{compensation\ \ gain} H_k X_k \quad (6)$$

From (6), the compensation gain can be balanced by the channel equalizer.

D. Adaptive Frequency-Domain Equalizer

In this 4×4 STBC MIMO-OFDM modem, the following code matrix is chosen

$$\mathbf{C} = \begin{bmatrix} c_1 & -c_2^* & -c_3^* & c_4 \\ c_2 & c_1^* & -c_4^* & -c_3 \\ c_3 & -c_4^* & c_1^* & -c_2 \\ c_4 & c_3^* & c_2^* & c_1 \end{bmatrix} \quad (7)$$

where c_i represents the transmitted complex data on the subcarrier. Let $r_{i,k}$ denote the *k*th received subcarrier at the *i*th symbol duration. The received data over four consecutive symbol periods at receiver one is expressed as

$$\begin{bmatrix} r_{1,k} \\ r_{2,k}^* \\ r_{3,k}^* \\ r_{4,k} \end{bmatrix} = \begin{bmatrix} h_{1,k} & h_{2,k} & h_{3,k} & h_{4,k} \\ h_{2,k}^* & -h_{1,k}^* & h_{4,k}^* & -h_{3,k}^* \\ h_{3,k}^* & h_{4,k}^* & -h_{1,k}^* & -h_{2,k}^* \\ h_{4,k} & -h_{3,k} & -h_{2,k} & h_{1,k} \end{bmatrix} \begin{bmatrix} x_{1,k} \\ x_{2,k} \\ x_{3,k} \\ x_{4,k} \end{bmatrix} + \begin{bmatrix} w_{1,k} \\ w_{2,k}^* \\ w_{3,k}^* \\ w_{4,k} \end{bmatrix} \quad (8)$$

$$\Rightarrow \mathbf{R}_k = \mathbf{H}_k\mathbf{X}_k + \mathbf{W}_k = \left[\begin{array}{c|c} \mathbf{H}_{11,k} & \mathbf{H}_{12,k} \\ \hline \mathbf{H}_{21,k} & \mathbf{H}_{22,k} \end{array}\right]\mathbf{X}_k + \mathbf{W}_k$$

where $h_{i,k}$ is the channel frequency response for the *k*th subcarrier from the *i*th transmit antenna to the receiver and $w_{i,k}$ is the noise term. The received symbols can be decoded by the STBC decoder with the estimated CFR, i.e., $\hat{\mathbf{X}}_k = \mathbf{H}_k^{-1}\mathbf{R}_k$. The CFR matrix $\mathbf{H}_k$ can be inverted blockwise using the following inversion formula [5]

$$\mathbf{H}_k^{-1} = \begin{bmatrix} \mathbf{H}_{11,k}^{-1} + \mathbf{H}_{11,k}^{-1}\mathbf{H}_{12,k}\mathbf{D}_k^{-1}\mathbf{H}_{21,k}\mathbf{H}_{11,k}^{-1} & -\mathbf{H}_{11,k}^{-1}\mathbf{H}_{12,k}\mathbf{D}_k^{-1} \\ -\mathbf{D}_k{}^{-1}\mathbf{H}_{21,k}\mathbf{H}_{11,k}^{-1} & \mathbf{D}_k^{-1} \end{bmatrix} \quad (9)$$

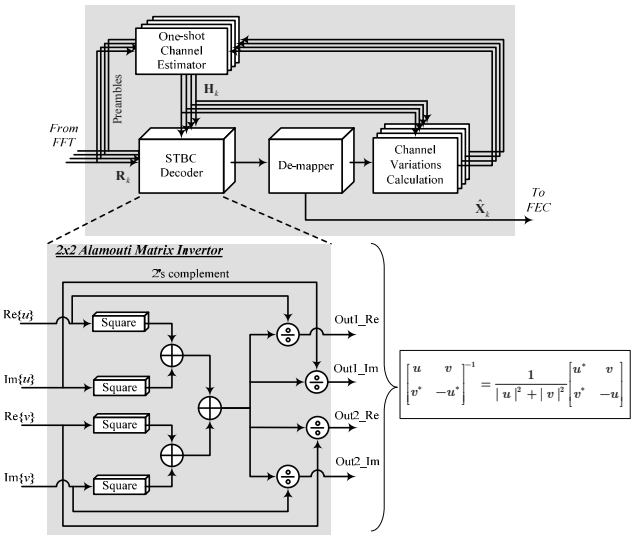

Fig. 6. Architecture of the adaptive equalizer.

where $\mathbf{D}_k = \mathbf{H}_{22,k} - \mathbf{H}_{21,k}\mathbf{H}_{11,k}^{-1}\mathbf{H}_{12,k}$. It can be verified that all submatrices in $\mathbf{H}_k$ are Alamouti-like matrices [6]. Due to time-varying effects, the estimated CFR is not consistent within the entire packet. Therefore, the received data can be rewritten as

$$\mathbf{R}_k = (\mathbf{H}_k + \Delta\mathbf{H}_k)\mathbf{X}_k + \mathbf{W}_k \quad [10]$$

In the adaptive procedure, the residual term $\Delta\mathbf{H}_k\mathbf{X}_k$ is calculated to update the channel state information.

Fig. 6 shows the adaptive equalizer. In this adaptive equalizer, data carriers are applied to measure channel variations, namely, virtual pilots. The one-shot estimator is adopted to measures an initial CFR obtained from long preambles. The de-mapper outputs the point of QAM constellation that has the minimum distance to its input. Due to time-varying fading, the decoded symbol contains a residual term that causes a decision error. The difference between ideal code sets and received symbols is used to extract channel variations. After calculating channel variations, CFR is updated. Notably, the inverse of an Alamouti matrix is still an Alamouti-like matrix. Only half of the Alamouti-like matrix must be computed – the other half can be obtained from the first half via sign-flipping operations. This characteristic is extremely useful as it can be exploited to derive an efficient architecture.

IV. Verification and Implementation Results

Fig. 7(a) displays the experiment setup for verification. The in-house RF front-ends are used in the transmitter as well as in the receiver. Therefore, there is also IQM at the transmitter part. Some compensation methods for transmitter IQM are available in the open literature. A pre-compensation scheme is applied to reduce the transmitter IQM [7]. The basic concept is that a training sequence is utilized to estimate the transmitter IQM. After IQM parameters estimation, the transmitter can compensate for the transmitter IQM using the baseband processing. This design is mapped onto the FPGA chips (Xilinx Virtex-II) with on-board 14-bit digital-to-analog

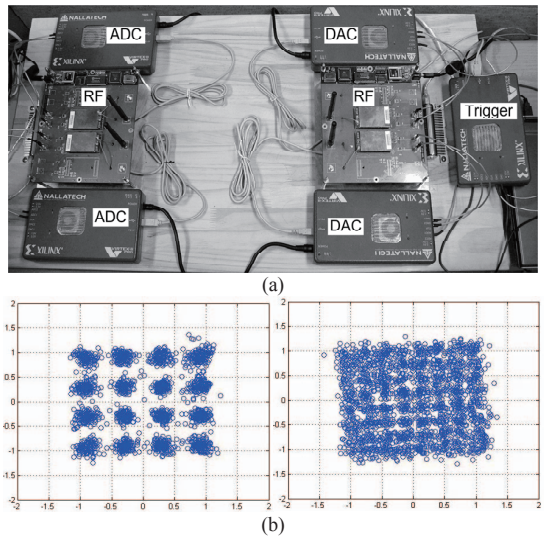

Fig. 7. (a) Verification platform. (b) QAM constellation performance.

converters (DACs). The signal is then transmitted by the in-house RF front-end. Since it is essential to make MIMO transmission coherent at all antennas, there is an additional DAC as a hardware trigger, namely "Trigger". At receiver part, the down-converted signal is fed into 14-bit analog-to-digital converters (ADCs) for further processing. Fig. 7(b) shows the constellation performance. The error vector magnitude (EVM) after the compensation is 8.6% (–21 dB).

This design is implemented in a standard 0.13-μm CMOS library. In this chip, the Viterbi decoder is not implemented (limited by chip area). The efficient throughput is 62.4 Mb/s with a 64-QAM modulation at 20 MHz in 4×4 STBC mode since one adaptive procedure requires 24.6 μs to measure 4 OFDM symbols (256 carriers). The memory requirement for the adaptive equalization is 50 K bits. The power consumption is about 62.8 mW with 266 Hz Doppler frequency tolerance at 1.2 V voltage. Die photograph and chip summary are shown in Fig. 8. Table II summarizes the current MIMO-OFDM system implementation results. This work provides a prototype for 4×4 STBC MIMO-OFDM system design.

V. Conclusions

This paper presents a 4×4 MIMO-OFDM modem with one-symbol-locked timing recovery, anti-IQM frequency controller, FD-IQM estimation and adaptive frequency-domain equalization. This 4×4 MIMO-OFDM modem is fabricated in a 0.13-μm CMOS process with 4.6×4.6 mm^2 area and 62.8 mW power consumption at 1.2 V.

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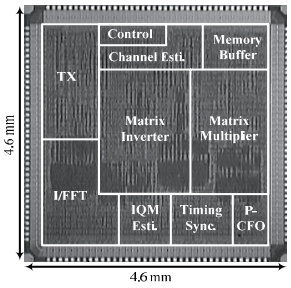

Chip Summary

Process	0.13-μm 1P8M CMOS
Package	160 CQFP
Die size	4.6×4.6 mm^2
Gate count	2580 K
Supply voltage	1.2 V Core, 3.3 V I/O
System clock	20 MHz
Core power	62.8 mW @ 1.2 Core

Fig. 8. Die photograph and chip summary.

TABLE II
Summary of Related Works

	[8]	[9]	[10]	**This work**
System	2×2 MIMO OFDM	2×2 MIMO OFDM	3×3 MIMO OFDM	4×4 MIMO OFDM
Process	0.18	0.18	0.18	0.13
Package	165 BGA	208 LQFP	304 BGA	160 CQFP
Modulation	B/Q-PSK, 16/64-QAM	B/Q-PSK, 16/64-QAM	B/Q-PSK, 16/64-QAM	B/Q-PSK, 16/64-QAM
Design	MAC + Baseband	Baseband	MAC + Baseband	Baseband
Gate count	N/A	4.8 M	14.2 M	2.58 M
Supply voltage	1.8 V Core	1.8 V Core, 3.3 V I/O	1.8 V Core, 3.3 V I/O	1.2 V Core, 3.3 V I/O
Power (RX)	275 mA (current)	774 mW @ 120 Mb/s	972 mW	62.8 mW @ 62.4 Mb/s
Die area	18 mm^2	15.2 mm^2	62.1 mm^2	21.2 mm^2

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