

# A Sub-100 $\mu$ W Area-Efficient Digitally-Controlled Oscillator Based on Hysteresis Delay Cell Topologies

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**Abstract**—This work addresses an all digitally-controlled oscillator (DCO) design with three newly proposed hysteresis delay cells (HDC). According to circuit topologies, the three HDCs are defined as on-off, cascaded, and nested HDCs that provide different propagation delay. These HDCs comprise architecture, a power-of-two delay stage DCO (P2DCO), that every delay stage provides half delay than the previous one in a descending order, resulting in low power and low cost features. A self-calibration method is accompanied to maintain the monotonicity of the P2DCO under PVT variations. The P2DCO is verified in a 90nm CMOS technology. The LSB control word provides a 2.04ps delay resolution. The post-layout simulations show that the dynamic power is 75.9 $\mu$ W and 5.2 $\mu$ W in the 239.2MHz and 3.89MHz, respectively. The area of the P2DCO is 60\*20 $\mu$ m<sup>2</sup>.

## I. INTRODUCTION

Digitally-controlled oscillator (DCO), as a key module in digitally-controlled-based frequency synthesis applications [1], shows several advantages over conventional voltage-controlled oscillator (VCO). DCO possesses the merits of easier porting between different process and voltage scaling and minimizes control and integration efforts. However, it is reported [2] that 50%~70% power of a clocking circuit comes from the DCO, playing the major bottleneck in total power reduction. In other words, power reduction in a DCO design effectively cuts down the overall system power, especially in low-power SoC applications.

DCO has been proposed in several architectures. The current-starved DCO provides high delay resolution but features high static power consumption. The standard-cell based DCO with straightforward delay elements, buffer/inverters and or-and-inverter logic cells, presents 100 $\mu$ W-order power and poor linearity with insufficient delay resolution, whereas the digitally-controlled varactor (DCV) improves delay resolution but with similar power scale. Therefore, a hysteresis delay cell (HDC) was proposed for tradeoff between power and delay resolution [3][4]. However, the resultant power saving is limited especially in low operating frequency, since the state-of-the-art DCO designs all require a large-area delay line to reach sufficient delay combinations. Consequently, this work addresses (i) a set of

HDCs with novel structures (on-off, cascade, and nested) which are power efficient, especially in low operation frequency, (ii) a power-of-two (P2) delay stage architecture which largely reduces the DCO area with the proposed HDC set. However, because the delay variation of the proposed HDCs is large under different process, voltage and temperature (PVT) conditions, a binary recovery self-calibration (BRSC) algorithm is proposed to improve the monotonicity of the proposed DCO. These three features accordingly overcome the challenge in the DCO power reduction and make the proposed DCO a preferred choice in power-thirsty or battery-less systems, especially in a sub-100MHz design.

## II. SYSTEM OVERVIEW

The system includes a power-of-two DCO (P2DCO) and the BRSC block as shown in Fig. 1. The P2DCO features low power and small area properties, which is accomplished by utilizing novel HDCs. The BRSC block, which includes a distortion estimator and a codeword mapper, is to compensate the non-monotone effect of the P2DCO under PVT variations.

The proposed P2DCO includes three tuning stages: the coarse tuning stage and two fine tuning stages as illustrated in Fig. 2. For each tuning stage, the delay segment of each control code bit is organized in a P2 structure where each delay segment produces half of the delay time of the one placed prior to it in the delay line. This architecture exempts the need for a binary to decimal converter, which is typical in the state-of-the-art DCO designs. The control method in a coarse tuning stage is to choose a path by a multiplexer for different propagation delay. In the fine tuning stages, it is by the direct control of the delay cells.

Each stage utilizes different types of HDCs as its delay cells. The coarse stage tuning applies cascaded HDCs (CHDC) and nested HDCs (NHDC) while the 1<sup>st</sup> fine tuning stage uses on-off HDCs (OHDC). In the 2<sup>nd</sup> fine tuning stage, MOS gate

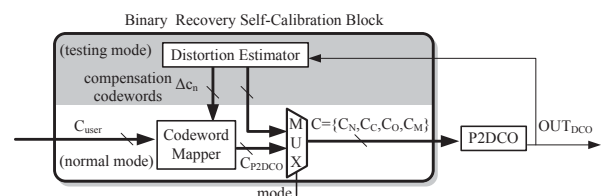


Fig. 1. System block diagram of the P2DCO and the BRSC algorithm

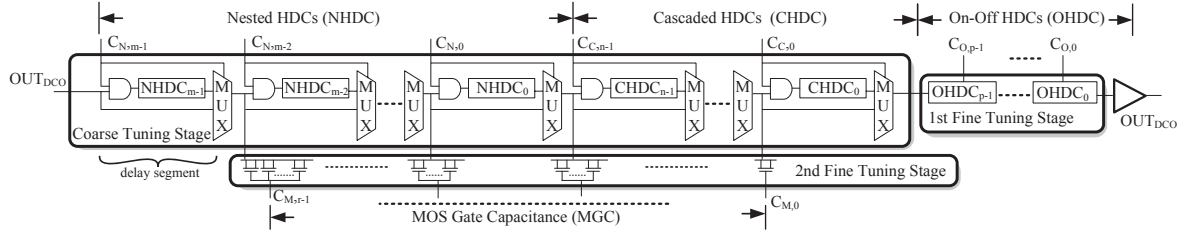


Fig. 2. Architecture of the P2DCO

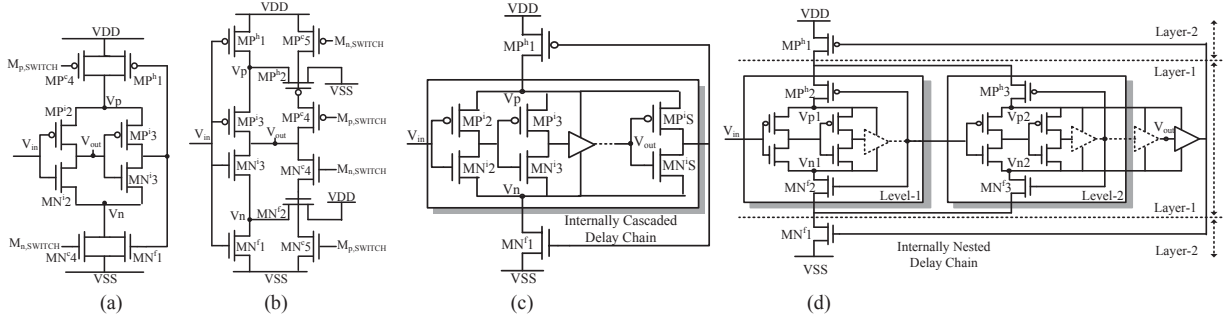


Fig. 3. The proposed HDCs (a)On-Off HDC (b)On-Off HDC (c)Cascaded HDC (d)Nested HDC

capacitance (MGC) is applied to generate variant combinations of output loadings for delay fine tunings. The gate capacitance is also arranged in the P2 ordering style by combining a number of controlled transistors.

The non-monotone behavior in a P2DCO design comes from inconsistent delay variations among different HDC structures under PVT variations. Therefore, the BRSC block is proposed to maintain monotone with a codeword transformation. It also eases the design effort of precise tuning to fulfill the P2 requirement. In the BRSC testing mode, the distortion estimator computes the compensation codewords ( $\Delta c_n$ ) automatically. After that in the normal mode, the codeword mapper uses  $\Delta c_n$  to generate  $C_{P2DCO}$  and passes it to the P2DCO.

### III. PROPOSED HYSTERESIS DELAY CELLS

The feasibility of Schmitt trigger circuits in low power operation has been discussed in [5][6]. This work further exploits this concept of the hysteresis phenomena and proposes three topologies for HDC designs that are able to generate delays in a wide range and possess better power efficiency compared with the state-of-the-art delay cells.

#### A. On-off HDC

An on-off HDC (OHDC) is designed on a Schmitt-trigger circuit basis, as shown in Fig. 3(a)(b). By adding two controlling transistors  $MP^4$  and  $MN^4$ , the delay cell can be determined to operate as a normal inverter or a hysteresis inverter. Therefore, a delay difference is derived between these two modes. This is able to generate finer resolution than simply using the hysteresis cell as a delay element.

The concept of maintaining or destroying hysteresis property can be applied to various forms of Schmitt-trigger circuits. This work only demonstrates two possible types of circuit for the consideration of power consumption and delay range. The extra controlling transistors  $MP^5$  and  $MN^5$  in

Fig.3(b) is used to prevent potential short current paths which may cause extra power consumption and unbalanced fall time and rise time current, resulting in poor jitter performance.

#### B. Cascaded HDC

A general form of cascaded HDCs (CHDC) is shown in Fig. 3(c). It can be viewed as an on-off HDC in the Schmitt-trigger mode with longer internal inverter chain. The header transistor  $MP^1$  and the footer transistor  $MN^1$  play a role as voltage gating cells that scale down the actual supply voltage of an internal inverter chain and confine the short current generated from internal nodes during voltage transitions. As a result, the power of this cascaded HDC is much lower than that of a normal inverter chain.

#### C. Nested HDC

A general form of nested HDCs (NHDC) is shown in Fig. 3(d). It can be viewed as a cascaded HDC with its internal delay chains composed of cascaded HDCs. A signal transition at the input propagates through all the inverter chains in each separate level from lower layers to higher layers. Here a two-layer nested HDC is demonstrated. It can be nested deeper as long as the threshold voltage is small enough. However, the footer and header transistors should be designed to reach the same status (on or off) when in steady state. This guarantees full-swing in each output node of internal delay chains so that each delay block has balanced delay time. The power-saving mechanism of nested HDCs is similar to that described for cascaded HDCs only with a more evident improvement since the supply voltage for the internal delay chain propagation is scaled down to a greater degree.

### IV. BINARY RECOVERY SELF-CALIBRATION ALGORITHM

The non-monotone behavior of a P2DCO is demonstrated in Fig. 4 where some delay segments fail the P2 ordering style because of unbalanced change of delay time among the delay segments under PVT variations. Therefore, when a user-

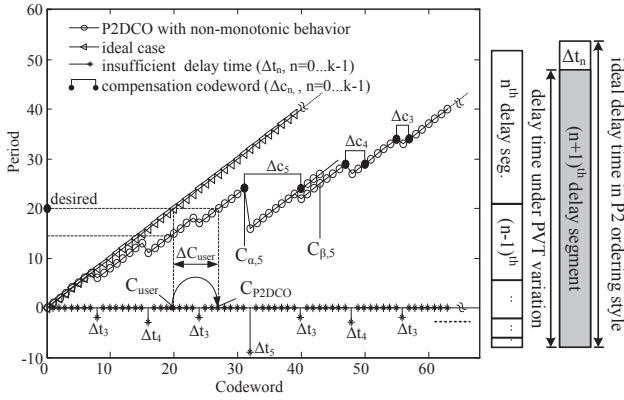


Fig. 4. A model for BRSC algorithm

defined codeword ( $C_{user}$ ) is directly input to the P2DCO, the output period may show an offset due to variant PVT conditions. To solve this issue, a mapping from  $C_{user}$  to a new codeword  $C_{P2DCO}$ , which leads to the desired output period, is required. The mapping from  $C_{user}$  to  $C_{P2DCO}$  can be expressed as (1).

$$C_{P2DCO} = C_{user} + \Delta C_{user} \quad (1)$$

The BRSC algorithm is to reconstruct the P2 relation among delay segments by filling the insufficient delay time of each delay segments with the delay time of the others. This is done by representing the insufficient delay time ( $\Delta t_n$ ) of the  $(n+1)$ -th delay segment as a compensation codeword ( $\Delta c_n$ ) generating equivalent delay time as shown in Fig. 4. Whenever crossing a gap, a corresponding compensation codeword is added to the original codeword to maintain the monotonic behavior. Here only demonstrates the curve for the six LSBs of the control codeword. It could be further extended to the total length of the control codeword. As a result,  $\Delta C_{user}$  is the sum of the compensation codeword corresponding to all the gaps included in  $C_{user}$ .

$$\Delta C_{user} = \sum_{n=0}^{k-1} i_{C_{user},n} \Delta c_n \quad (2)$$

where  $k$  is the codeword length.  $i_{C_{user},n}$  is the number of gaps caused by the  $(n+1)$ -th delay segment in  $C_{user}$ .  $i_{C_{user},n}$  is expressed as (3) due to the P2 structure.

$$i_{C_{user},n} = \begin{cases} \lfloor (C_{user} - 2^n) / 2^{n+1} \rfloor + 1, & C_{user} - 2^n \geq 0 \\ 0, & C_{user} - 2^n < 0 \end{cases} \quad (3)$$

During the testing mode, the distortion estimator computes the key parameters  $\Delta c_n$  by using (4) and (5), which is similar in concept with (1) and (2). It states that the difference between a pair of codewords ( $C_\alpha, C_\beta$ ) equals to the sum of the compensation codewords needed to fill the gaps between them.

$$C_\beta = C_\alpha + \Delta C_{\beta-\alpha} + 1 \quad (4)$$

$$\Delta C_{\beta-\alpha} = \sum_{n=0}^{k-1} (i_{C_\beta,n} - i_{C_\alpha,n}) \Delta c_n \quad (5)$$

where  $C_\beta > C_\alpha$  and  $P(C_\beta) > P(C_\alpha) \geq P(C_\beta - 1)$ .  $P(C)$  represents the output period corresponds to a codeword  $C$ .

Therefore, the compensation codeword for each delay segments,  $\Delta c_n$ , can be solved by the simultaneous equations

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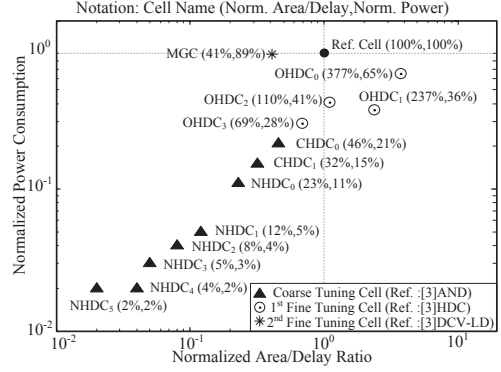


Fig. 5. Comparison for power and area/delay ratio

formed on the basis of (4) with  $k$  pairs of properly chosen codewords ( $C_{\alpha,n}, C_{\beta,n}$ ).  $C_{\alpha,n}$  is set to  $2^n - 1$  while  $C_{\beta,n}$  is derived by direct measuring the P2DCO. This method guarantees to include the information needed to solve  $\Delta c_n$ . Fig. 4 demonstrates an example of a codeword pair ( $C_{\alpha,5}, C_{\beta,5}$ ) generated from the above method.

## V. SIMULATION RESULTS

The proposed design, a P2DCO with BRSC algorithm is simulated in 90nm 1P9M CMOS process operating at 14MHz. Table I summarizes the HDCs used in this design based on the post-layout simulation results (partially from measurements). The simulation and measurement results of the delay cells used in [3] are listed as a comparison. The coarse tuning stage includes eight delay segments producing delay step from 0.5ns to 64ns. Each delay segment is mainly constructed with one HDC. In the 1st stage fine tuning, four OHDCs are combined to produce delay segment from 32ps to 0.5ns while the 2nd stage fine tuning is to produce delay segment from 1ps to 32ps with MGCs. Each delay segment is tuned to an approximate value, since the BRSC algorithm is able to compensate the imperfectness in P2 structure. Fig. 5 compares the performance of different HDCs and normalizes it with the performance of standard cells used in [3] at each tuning stage. The x-axis and y-axis implies the area and power saving from replacing standard cells with the proposed HDCs under the same operation frequency. It is reduced to a minimum of 2%, 28% and 89% of the original power in the coarse tuning stage and the two fine tuning stages respectively. Although some of the 1st fine tuning delay cells occupied larger area, the power reduction is the major concerns.

The power performance of a DCO design largely depends on its delay cells. It implies that the delay cell contributing the most delay time in an output period dominates the total power performance. Therefore, the total power consumption declines when the output period increases as shown in Fig. 6(a), since the proposed HDCs is the most power-efficient in coarse tuning stage. A P2DCO constructed with inverters is simulated for contrast. The power varies slightly in different output period since all delay cells possess the same delay time and power consumption.

Fig. 6(b) shows the post-layout simulation result to illustrate the improvement from the BRSC algorithm. The BRSC algorithm is applied at the coarse tuning stage, where the delay variation is most serious under different PVT

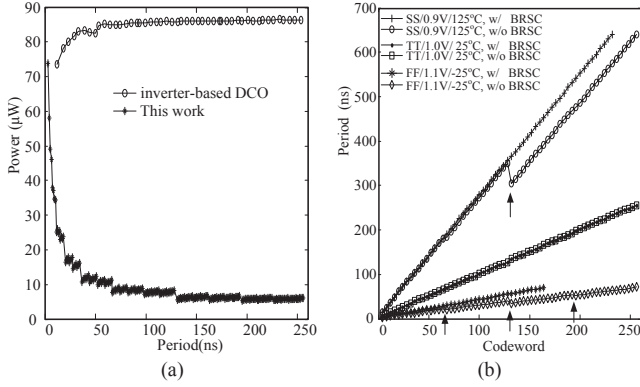


Fig. 6. Post-layout simulation result of (a) power consumption (b) the BRSC algorithm

condition. This prototype is well-tuned under 1V supply voltage and temperature at 25°C. Therefore, the curve in this condition is monotonic and overlapped with resultant curve after the BRSC algorithm. The simulation result under the other two different PVT conditions shows the non-monotonic behavior which is labeled with arrows. With the aid of the BRSC algorithm, the monotonic property is recovered.

The layout of the test chip is shown in Fig. 7. The area of the P2DCO is  $20 \times 60 \mu\text{m}^2$ . The rest includes the BRSC algorithm and some testing circuit. Table II shows the overall comparison of the P2DCO with the state-of-the-art oscillator designs. The P2DCO provides the least power consumption ( $5.2 \mu\text{W}@3.89\text{MHz}$ ,  $75.9 \mu\text{W}@239.2\text{MHz}$ ) with least area occupation compared to the state-of-the-art designs. Moreover, the proposed HDCs are compatible with the automated CAD tools and therefore save design efforts in system integration.

## VI. CONCLUSION

This work proposes three structures (On-Off, Cascaded, Nested) for the hysteresis-based delay cell design. Accompanied with the all-digital design scenario of the power-of-two delay stages, it enables the use of delay cells that have largely improved power/delay as well as area/delay density, resulting in both the least dynamic and static power consumption. Moreover, the monotonicity is well-maintained by the self-calibration scheme under different PVT variation. As a result, this work provides the most economic design approach, in terms of power and area, in the all-digital DCO in the state-of-the-art that it could be a suitable choice for low-power SoC applications.

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TABLE I. SIMULATION SUMMARIES OF DELAY CELLS

Tuning Stage	Delay Cell	Delay Res.(ns)	Power ( $\mu\text{W}$ )
Coarse Tuning	AND[3]	0.052 (0.052*)	103.93 (123.43*)
	NHDC <sub>5</sub>	65.016	1.74
	NHDC <sub>4</sub>	30.979	2.33
	NHDC <sub>3</sub>	16.069	3.04
	NHDC <sub>2</sub>	8.120	4.25
	NHDC <sub>1</sub>	4.003	5.54
	NHDC <sub>0</sub>	2.049	11.02
	CHDC <sub>1</sub>	1.040	15.93
	CHDC <sub>0</sub>	0.522	21.94
	1 <sup>st</sup> stage fine tuning	HDC[3]	0.083 (0.116*)
OHDC <sub>3</sub>		0.343	43.19
OHDC <sub>2</sub>		0.173	62.47
OHDC <sub>1</sub>		0.131	53.93
2 <sup>nd</sup> stage fine tuning	OHDC <sub>0</sub>	0.066	98.80
	DCV-LD[3]	0.738ps (1.21ps*)	153.95 (208.46*)
	DCV-SD[3]	0.61ps (0.85ps*)	159.95 (190.44*)
	MGC	1.02ps (1.22ps*)	137.02 (164.5*)

\*Measurement result

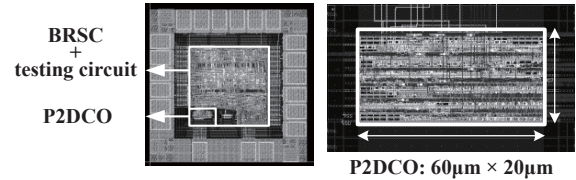


Fig. 7. Layout of the test chip

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TABLE II. COMPARISON WITH THE STATE-OF-THE-ART OSCILLATOR DESIGNS

	Proposed (simulation)	TCAS2'07[3] (measurement)	TCAS2'05[7] (measurement)	ISSCC'08[8] (measurement)
Process	90nm CMOS	90nm CMOS	0.35um CMOS	65nm CMOS
Approach	Digitally-Controlled Ring Oscillator	Digitally-Controlled Ring Oscillator	Digitally-Controlled Ring Oscillator	Voltage-Controlled Relaxation Oscillator
Supply Voltage (V)	1(0.9-1.1)	1	3.3	1.2(1.1-1.3)
Operation Range (MHz)	3.8-239.2	191-952	18-214	12
LSB Resolution(ps)	2.04	1.47	1.55	NA
Jitter	2.16ps (239MHz,p-p) 446fs (239MHz,rms)	49.05ps (417MHz,p-p) 8.18ps (417MHz,rms)	NA	-161.7dB@290K
Power Consumption	5.2µW(3.89MHz) 75.9µW(239.2MHz)	140µW(200MHz)	18mW (200MHz)	90µW(12MHz)
Area	1200µm <sup>2</sup>	NA	40000µm <sup>2</sup>	24000µm <sup>2</sup>