Amorphous InGaZnO Thin-Film Transistors Compatible With Roll-to-Roll Fabrication at Room Temperature

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***Abstract*—High-performance amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) are successfully fabricated on a colorless polyimide substrate using a top-gate self-aligned structure. All thin films are deposited by roll-to-roll-compatible sputtering processes at room temperature. The maximum field-effect mobility is 18 $cm^2/V \cdot s$, the threshold voltage is −1.35 V, the subthreshold slope is 0.1 V/decade, and the on/off current ratio is about 10^5. The results highlight that excellent device performance can be realized in a-IGZO TFTs without compromising manufacturability.**

***Index Terms*—Amorphous InGaZnO, roll-to-roll, thin-film transistor (TFT).**

I. INTRODUCTION

FLEXIBLE electronics are becoming increasingly important because of the advantages of flexibility, thin form factor, and light weight. In particular, the roll-to-roll process technology using flexible substrates is the most attractive because of its high-throughput capability and, thereby, very low manufacturing cost [1]. However, the device characteristics of low-temperature organic and a-Si thin-film transistors (TFTs) on flexible substrates of low glass transition temperature are insufficient to meet the requirements of active devices for high-performance applications. Recently, low-temperature amorphous indium–gallium–zinc oxide (a-IGZO) TFTs have attracted much attention for applications on next-generation displays and flexible electronics, owing to their high mobility and transparency [2]. Although excellent electrical characteristics have been shown in previous studies [3], [4], a-IGZO TFTs often require thermal annealing after device fabrication. The development of a-IGZO TFTs compatible with a room-temperature roll-to-roll process is less addressed.

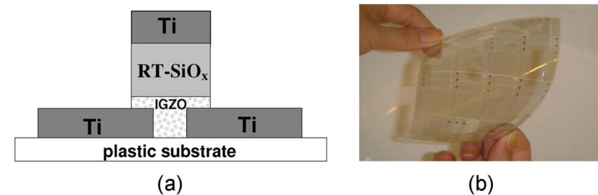

Fig. 1. (a) Device structure of the top-gate self-aligned a-IGZO TFT. (b) Top-gate self-aligned a-IGZO TFT on the PI substrate under bending condition.

In this letter, we successfully demonstrate a top-gate self-aligned IGZO TFT on a colorless polyimide (PI) substrate manufactured by a roll-to-roll-compatible process. The multichamber sputter tool that we used to deposit all films at room temperature and the photolithography and etching tools for device fabrication are all capable of continuous roll-to-roll manufacturing for large-size flexible applications. Excellent electrical characteristics applicable for future high-performance flexible electronics are reported for devices fabricated by a complete room-temperature process. In addition, the effects of thermal annealing after device fabrication are also discussed.

II. EXPERIMENTAL SECTION

A top-gate self-aligned a-IGZO TFT structure shown in Fig. 1(a) was fabricated in this study because of its superior manufacturability [5]. This structure reduces the number of required masks, using only two compared to four in a conventional bottom-gate non-self-aligned structure. First, colorless PI was spin coated on a 6-in glass carrier and baked at 220 °C for 4 h. The prepared PI substrate was 40 μm thick with high glass transition temperature (about 350 °C) and excellent transmittance. More details on the preparation of the PI substrate can be found in [6]. Source and drain electrodes were 50 nm of Ti deposited in a multichamber roll-to-roll sputter system, followed by photolithography patterning and wet etching. Then, 40-nm IGZO, 200-nm SiO_2, and 100-nm Ti were deposited in the same multichamber sputter system at room temperature. A base pressure below 1×10^{-6} torr, a deposition pressure of about 0.5 mtorr, an Ar flow rate of 50 sccm, an O_2 flow rate of 10 sccm, and an RF sputter power of 1000 W were used for the IGZO deposition. The composition of the IGZO target was 2 : 2 : 1 : 7 for In:Ga:Zn:O. After gate photolithography, the Ti gate electrode, SiO_2, and IGZO films were wet

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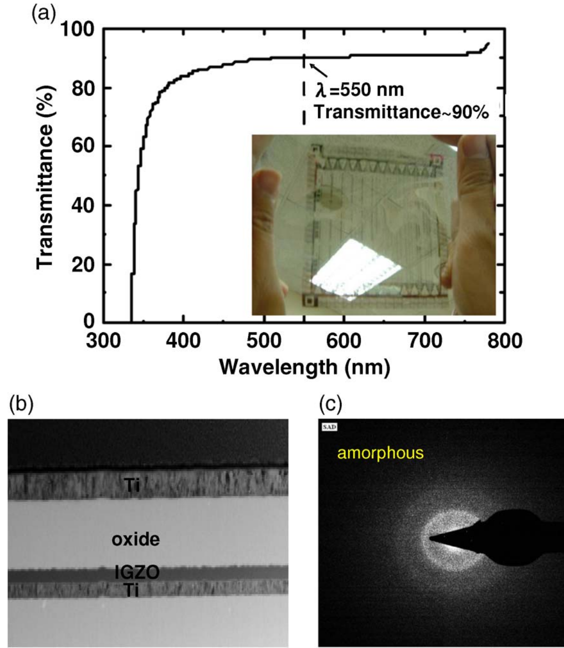

Fig. 2. (a) Optical transmission spectrum of the PI substrate. The inset shows the transparent PI substrate with metal lines on the top. (b) Cross-sectional TEM of the device structure. (c) Electron diffraction pattern of the a-IGZO film.

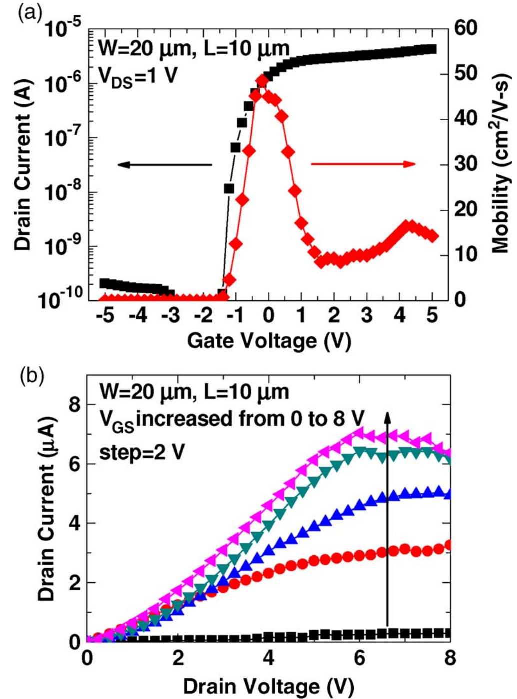

Fig. 3. Typical (a) transfer and (b) output characteristics of the top-gate self-aligned a-IGZO TFT.

etched using the same mask in a self-aligned manner until the source/drain metal is exposed. The etchants for Ti, SiO_2, and IGZO were $NH_4OH + H_2O_2$, BOE (20:1), and oxalic acid. The overlap between the gate and source/drain regions was less than 2 μm. At last, the PI substrate was debonded from the glass carrier. The I–V electrical characteristics were measured by an Agilent 4156C semiconductor parameter analyzer. Although the present device was fabricated on a small-size glass carrier with a spin-on flexible substrate for convenience, the scale-up to a mass-production roll-to-roll process on other commercial low-temperature flexible substrates such as polyethylene terephthalate would have minimal impact on the a-IGZO TFT characteristics because all process steps mentioned here were done in roll-to-roll-compatible equipment and at room temperature. Fig. 1(b) shows the top-gate self-aligned IGZO TFT on the PI substrate under bending condition.

III. Results and Discussion

Fig. 2(a) shows the optical transmission spectrum over the visible light range of the PI substrate. At $\lambda = 550$ nm, the measured transmittance was about 90%. The inset in Fig. 2(a) shows the highly transparent PI substrate with metal lines on the top. Fig. 2(b) shows the cross-sectional TEM of the device structure. An amorphous phase of the IGZO film by room-temperature deposition was conformed by the electron diffraction pattern in Fig. 2(c). The amorphous active channel is preferential for better device uniformity and reproducibility by mitigating the effects of grain boundaries [2].

Fig. 3(a) shows the transfer characteristics of the top-gate self-aligned a-IGZO TFT without any thermal annealing. The channel width and length were 20 and 10 μm, respectively, and the drain voltage was 1 V. The device had an on/off current ratio of around 10^5 at $V_G = \pm 5$ V, a very steep subthreshold slope of 0.1 V/decade, a threshold voltage of -1.35 V, and a maximum field-effect mobility of 48.5 $\mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$. The threshold voltage was determined from the maximum G_m method, while the field-effect mobility was extracted from the linear regime. The channel width of 20 μm was defined by the width of the source/drain rather than the width of the IGZO film, which was considerably wider in the self-aligned structure. Therefore, the effective channel width calibrated using devices with various channel widths was larger than 20 μm due to the fringing current effect. The mobility after calibration was decreased by 63% to 18 $\mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$. Table I compares the important device parameters of the a-IGZO TFT with those on various flexible substrates reported in the literature. The high mobility and steep subthreshold slope in the present work were among the best ever reported. The results highlight the excellent interface quality between the a-IGZO channel and SiO_2 even by a room-temperature roll-to-roll-compatible process.

Several aspects of device performance, namely, gate leakage current, contact resistance, and carrier mobility, may be further improved by the additional thermal treatment after device fabrication. Because the gate insulator was deposited by sputtering at room temperature, a large number of defects existed in the oxide film. These defects resulted in an increased off current because of gate leakage. In Fig. 3(a), the off current under negative gate bias was slightly higher, at around 200 pA at $V_G = -5$ V. Moreover, without any thermal annealing, the nonlinear I_{DS}–V_{DS} curve at the low-V_{DS} and high-V_{GS} regime in Fig. 3(b) suggests the nonideal Schottky source/drain contact. Extensive conditions of thermal annealing in atmospheres of nitrogen and air and in a vacuum over a range from 150 °C to 230 °C have been investigated. The best result was obtained by using the nitrogen annealing at 210 °C. Fig. 4 shows the transfer and output characteristics of the a-IGZO TFT after annealing. The thermal annealing densified the oxide film and reduced defects. By improving the quality of the gate insulator, the off current was suppressed to 20 pA at $V_G = -6$ V, as shown in Fig. 4.

TABLE I
COMPARISON OF VARIOUS a-IGZO TFTs FABRICATED ON FLEXIBLE SUBSTRATES

	Max. Process Temp.	operation voltage (V)	μ (cm²/V-s)	V_{th} (V)	SS (V/decade)	on/off ratio	substrate
this work	RT	5	18	-1.35	0.1	1×10^5	PI
[3]	200 °C	1.5	22.1	0.1	0.18	2×10^5	PI
[7]	<100 °C	10	5.3	1.13	0.55	8×10^4	PI
[8]	90 °C	6	12.1	1.25	0.35	$>10^5$	PET
[9]	RT	6	3.9	1.4	0.2	1.7×10^6	PET
[10]	RT	4	10.86	-0.34	0.46	4.13×10^6	PET
[11]	RT	20	34	1.9	0.8	2.9×10^4	Cellulose
[7]	RT	-	35	3.75	2.4	1×10^4	Cellulose
[12]	100 °C	10	1.2	1.9	0.65	1×10^4	Paper
[13]	300 °C	25	15	3	0.5	$>10^7$	Metal Foil

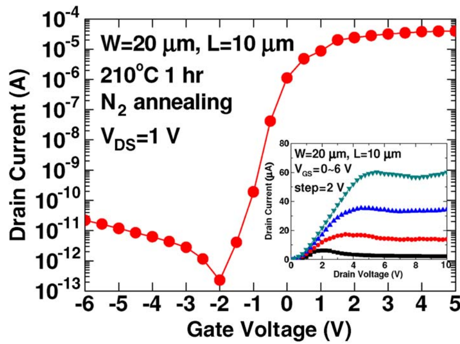

Fig. 4. Typical transfer characteristics of the top-gate self-aligned a-IGZO TFT after nitrogen annealing at 210 °C for 1 h. The inset shows the output characteristics.

In addition, the on current increased several times by improving the source/drain contact and increased mobility. Because the source/drain and the IGZO channel were deposited at room temperature, the intermixing of Ti and IGZO was very limited before annealing and resulted in higher contact resistance. The annealing process facilitated the intermixing at the interface and thus improved the contact resistance. The extracted mobility after annealing increased to about 32 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ after calibrating for the effective channel width. However, the subthreshold slope degraded to 0.25 V/decade, possibly due to the interaction between a-IGZO and SiO_2 at the annealing temperature.

IV. CONCLUSION

This letter has demonstrated the fabrication of a high-performance top-gate self-aligned a-IGZO TFT on a colorless PI substrate through a room-temperature sputtering process. The TFT has an on/off current ratio of about 10^5, a subthreshold slope of 0.1 V/decade, a threshold voltage of -1.35 V, and a field-effect mobility of 18 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. Moreover, all processes are completed using a roll-to-roll-compatible manufacturing facility. This device is suitable for active devices in large-area and low-cost flexible electronics and display applications.

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