Characteristics of n-Type Junctionless Poly-Si Thin-Film Transistors With an Ultrathin Channel

Horng-Chih Lin, *Senior Member, IEEE*, Cheng-I Lin, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—In this letter, we study the characteristics of n-type junctionless (JL) poly-Si thin-film transistors (TFTs) with an ultrathin and heavily phosphorous doped channel. The fabricated devices show excellent performance with a subthreshold swing of 240 mV/dec and an on/off current ratio of $> 10^7$. Moreover, the JL device shows 23 times increase in the ON-state current at a gate overdrive of 4 V as compared with the conventional control device with an undoped channel. The significant improvement in the current drive is ascribed to the inherently high carrier concentration contained in the channel of the JL device. These results evidence the great potential of the JL poly-Si TFTs for the manufacturing of future 3-D and flat-panel electronic products.**

***Index Terms*—Junctionless (JL), poly-Si, thin-film transistor (TFT).**

I. Introduction

RECENTLY, the concept of junctionless (JL) MOS devices, which have their channel doping of the same type and comparable level to that of the source and drain (S/D), has been proposed and explored [1], [2]. Such a scheme has also been demonstrated with poly-Si-based devices [3] which could be useful for 3-D device integration, such as stackable high-density nonvolatile memory [4]. These previous works [1]–[3] utilized NW channel and multigated configurations in order to effectively turn off the conduction which is essential for the successful operation of the JL devices. In this letter, we investigate and show that this concept can actually be realized on planar poly-Si thin-film transistor (TFT) devices if the channel is sufficiently thin, e.g., ∼10 nm. This scheme could further extend the feasibility of the JL devices for future 3-D-IC and flat-panel applications.

For a conventional inversion-mode (IM) MOSFET, the induced inversion charge per unit gate area for conduction, denoted as Q_c, is equal to $C_{\rm ox}(V_G - V_{\rm th})$ [5], where $C_{\rm ox}$, V_G, and $V_{\rm th}$ are the gate oxide capacitance per unit area, the gate voltage, and the threshold voltage, respectively. For typical operations, the number of induced conduction carriers Q_c/q (q is the electron charge) is around 10^{12} cm^{-2}. Such a value is easy to surpass in a planar JL device, in which Q_c/q is simply related to the product of carrier concentration and thickness of the channel, as the effects of gate bias and oxide charges are ignored. Fig. 1 shows the relations between the carrier concentration and the channel thickness at $Q_c/q = 5 \times 10^{12}$, 10^{13}, and 5×10^{13} cm^{-2}, respectively. These high values are not commonly seen in IM devices as oxide reliability and breakdown are concerned. Nonetheless, as shown in the figure, for the JL devices, it only demands an ultrathin channel ($\leqq$10 nm) to reach these high Q_c/q values if the carrier concentration is higher than 10^{19} cm^{-3}. This implies that a very high current drive is achievable with the JL devices which inherently contain abundant carriers inside the channel. However, the successful operation of the devices depends on whether the channel can be effectively depleted by the gate bias in order to shut off the conduction current. In normal situations, the voltage drop across the depletion region is limited by the material's bandgap which is around 1 eV for degenerately doped poly-Si [6]. Based on this criterion, we can calculate the maximum depletion width, and the results are also shown in Fig. 1, which can be regarded as a reference guideline for device design and fabrication.

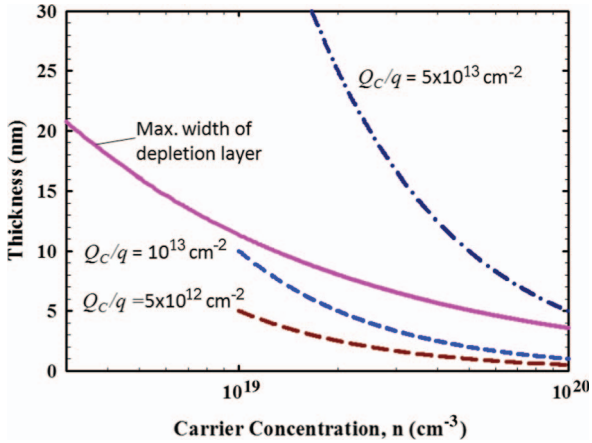

Fig. 1. Thickness values of the channel of the JL devices as a function of carrier concentration with fixed Q_c/q of 5×10^{12}, 10^{13}, and 5×10^{13} cm^{-2}. The calculated maximum width of the depletion region is also shown.

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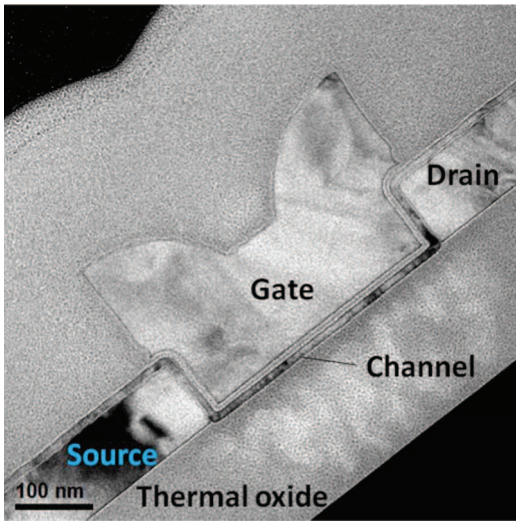

Fig. 2. Cross-sectional TEM image of a JL poly-Si TFT with a channel thickness of 10 nm, a gate oxide thickness of 8.5 nm, and a channel length of 0.4 μm.

II. Device Fabrication

In this letter, the JL devices were fabricated on Si wafers capped with a 200-nm-thick thermal oxide. To reduce the parasitic S/D resistance, 100-nm-thick n^+ poly-Si was first deposited and patterned to form the S/D pads, followed by the sequential deposition of a 10-nm n^+ poly-Si layer as the channel, an 8.5-nm oxide as the gate dielectric, and a 150-nm n^+ poly-Si layer as the gate electrode. All these films were deposited by low-pressure chemical vapor deposition. Fig. 2 shows the TEM image of a fabricated device showing the uniform thickness of the channel. These n^+ poly-Si layers were *in situ* doped. Hall measurements performed on blanket n^+ poly-Si of 200 nm indicate that the carrier concentration and Hall mobility are 7×10^{19} cm^{-3} and 43 cm^2/V $\cdot$ s, respectively. More efforts are in progress to extract the practical carrier concentration in the ultrathin channel of the JL device. The value should be reduced owing to the occurrence of dopant segregation [7]. Nonetheless, it is expected to be larger than 10^{19} cm^{-3}. For comparison, control devices, which were fabricated with the same process as that of the JL split except that the 10-nm-thick poly-Si channel is undoped, were also characterized.

III. Results and Discussion

Typical transfer and output I–V characteristics of the fabricated devices are shown in Figs. 3 and 4, respectively. In Fig. 3, an on/off current ratio larger than 10^7 is achievable for both splits. The control device exhibits a very low subthreshold swing (SS) of 125 mV/dec, owing to the use of an ultrathin channel. For the JL TFT, the SS is 240 mV/dec, which is higher than that of the control one but acceptable [4], [8]. The larger SS is attributed to an increase in the equivalent oxide thickness of the JL devices because of the contribution from the depleted channel region as the device is turned off. Owing to the high doping concentration in the channel, the JL TFT is normally on with a threshold voltage $(V_{\rm th})$ of -0.3 V, which is defined as the gate voltage (V_G) at drain current (I_D) equal to $10^{-9} \times W/L$ (in amperes), where W and L are the channel width and length, respectively. The value can be increased if a gate electrode of high work function, such as TiN [9], is employed.

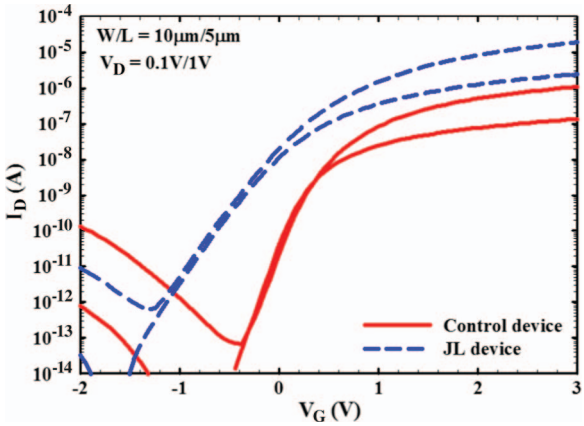

Fig. 3. Transfer characteristics of the JL and control devices measured at V_D of 0.1 and 1 V.

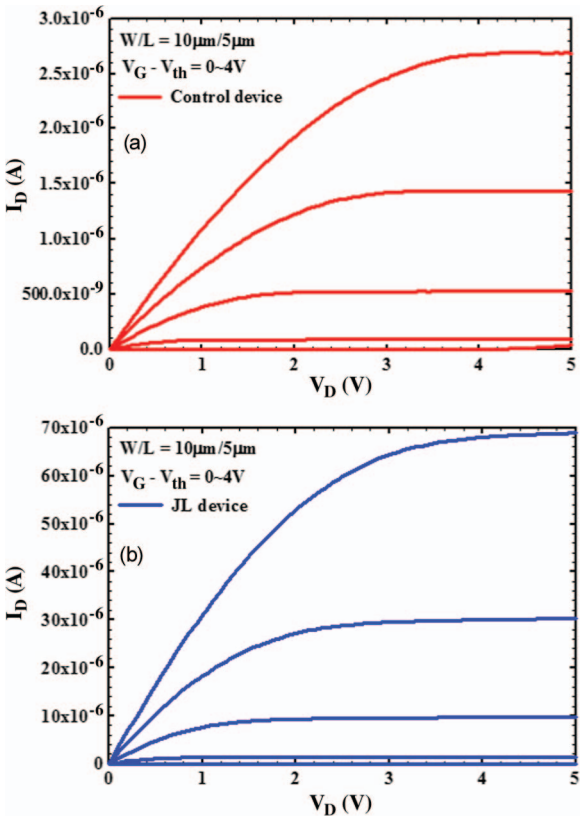

Fig. 4. Output characteristics of the (a) control and (b) JL devices at $(V_G - V_{\rm th})$ of 1–4 V.

On the other hand, a dramatic increase in ON-state I_D is unambiguously demonstrated. This is illustrated by comparing the output characteristics of the control and JL devices shown in Fig. 4(a) and (b), respectively. In the figures, I_D is expressed as a function of gate overdrive. For $(V_G - V_{\rm th})$ of 4 V, the I_D of the JL device is about 23 times higher than that of the control

device. Such an astonishing improvement is obviously related to the abundant carriers contained in the channel and confirms the potential of the JL scheme for practical applications. It is well known that the carrier mobility in poly-Si TFTs is limited by the potential barriers presenting at the grain boundaries. However, as the carrier concentration is sufficiently high, the barrier height decreases with increasing concentration and becomes negligible as the concentration is larger than 10^{19} cm^{-3} [10]. This might be another factor that needs to be taken into account for the high current drive of the JL devices.

IV. Conclusion

In summary, we have fabricated and characterized JL poly-Si TFTs with an ultrathin and heavily doped channel. Unlike traditional TFTs which need a high gate voltage to induce inversion carriers for boosting the drive current, the heavily doped channel of the JL devices inherently provides abundant carriers to conduct the current. Considering the simplification in device fabrication by skipping the implant step as well as the excellent device performance achieved in this letter, JL poly-Si TFTs represent a feasible alternative to conventional poly-Si TFT technology for 3-D-IC and flat-panel manufacturing.

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