High-Performance Light-Erasable Memory and Real-Time Ultraviolet Detector Based on Unannealed Indium–Gallium–Zinc–Oxide Thin-Film Transistor

Wei-Tsung Chen and Hsiao-Wen Zan

***Abstract*—A light-erasable memory and a real-time ultraviolet (UV) detector were developed from an amorphous indium–gallium–zinc–oxide (IGZO) thin-film transistor fabricated at room temperature without post-annealing. The natural defects within the IGZO or at the dielectric interface serve as electron traps to support a writing operation (switching down the channel conductance). A negative gate bias accompanied by UV illumination performs an erasing operation (switching up the channel conductance). After the writing/erasing of the proposed memory, an on/off ratio greater than 10^4 was maintained for a testing duration of 10 000 s. A real-time UV detector was also developed, and a light/dark ratio of roughly 10^4 was demonstrated.**

***Index Terms*—Indium–gallium–zinc–oxide (IGZO), memory, photodetector and room temperature.**

I. Introduction

AMORPHOUS metal–oxide thin-film transistors such as amorphous indium–gallium–zinc–oxide thin-film transistors (a-IGZO TFTs) are promising devices for uses in active-matrix displays, owing to their advantages such as high mobility [1] and low-temperature fabrication [2]. An a-IGZO TFT fabricated at low temperature exhibits an unstable threshold voltage under operation [3], [4]. Generally, efforts such as post-annealing and passivation are necessary to stabilize the a-IGZO TFT [4], [5]. The unstable behavior, however, can be advantageous when devices are used as detectors or memory. The threshold voltage (V_{TH}) is easily shifted by a bias stress, thus satisfying the requirement of a memory.

In this letter, based on the unstable characteristics of the a-IGZO TFT without post-annealing, we propose two promising applications: a light-erasable memory and a photodetector. In previous reports, a-IGZO TFTs with an additional carrier-trapping structure such as a floating gate [6], [7], a ferrodielectric [8], or a charge storage medium [9] have demonstrated good memory characteristics. In this letter, a conventional a-IGZO TFT without an additional carrier-trapping structure or post-annealing is proposed to serve as the memory device. The intrinsic acceptorlike states facilitate a significant positive shift in V_{TH}, which supports the writing operation by providing the low channel conductance (low state) of a memory or photodetector. Generally, these defects are intentionally suppressed by post-thermal annealing [4]; however, for a memory or photodetector, these defects become usable trapping centers that are obtained without effort.

A metal–oxide material exhibits an intense ultraviolet (UV) photoresponse that partially depends on the oxygen in the surrounding environment [10]. The optical bandgap of a-IGZO is around 3.2 eV [11], which indicates that UV light with a wavelength shorter than 400 nm can be strongly absorbed by an IGZO film. In this letter, a negative gate bias (V_G) accompanied by UV illumination facilitates a significant negative shift in V_{TH} for the a-IGZO TFTs, through either hole trapping at the dielectric surface [12] or oxygen reemission from the exposed surface [10], which supports the erasing operation by providing the high channel conductance (high state) of a memory. Furthermore, although the writing operation is promptly disabled when the UV illumination commences, the writing mechanism also instantaneously recovers when the UV illumination ceases, and this facilitates its application in a real-time UV detector. The light-erasable memory is applicable in optical touch panels, while the sensitive UV detector based on the wide-bandgap IGZO is applicable, where blindness to visible light is required [10].

II. Experimental Procedure

A 100-nm-thick layer of thermal silicon nitride (SiN_x) was grown on heavily doped Si wafers to serve as the gate dielectric. A 35-nm-thick layer of a-IGZO was deposited on the SiN_x at room temperature by radio-frequency (RF) sputtering through a shadow mask to form the active layer. The RF power and the pressure were 70 W and 7 mtorr, respectively. The gas introduced during the sputtering was argon. Some devices were subjected to an annealing process at 350 °C in a nitrogen furnace for 1 h. Finally, as shown in Fig. 1(a), each bottom-gate top-contact a-IGZO TFT was completed with a 50-nm-thick layer of aluminum (Al) that was deposited through a shadow mask to form the source and drain contacts. The channel length

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The authors are with the Department of Photonics, Institute of Electro-Optical Engineering, and Display Institute, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: hsiaowen@mail.nctu.edu.tw).

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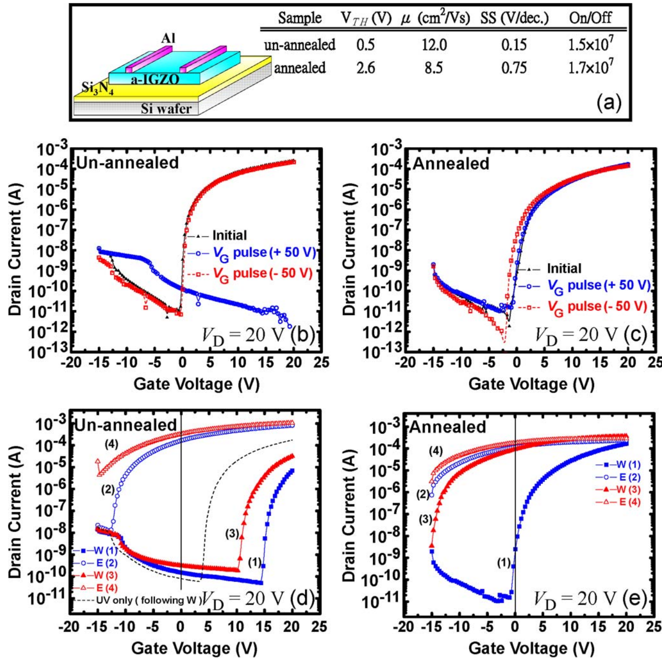

Fig. 1. (a) Schematic cross section of a-IGZO TFTs. (b) and (c) Transfer characteristics of unannealed and annealed a-IGZO TFTs as measured shortly after fabrication in response to positive V_G pulse (50 V, 20 s) and negative V_G pulse (-50 V, 20 s). (d) and (e) Transfer characteristics of unannealed and annealed a-IGZO TFTs as measured after several cycles of writing by positive V_G pulse (50 V, 20 s) and erasing by negative V_G pulse (-50 V, 20 s) accompanied by UV illumination. The curves in blue and red are for the first and second write/erase cycles, respectively. The numbers (1)–(4) in the figure denote the operation sequence.

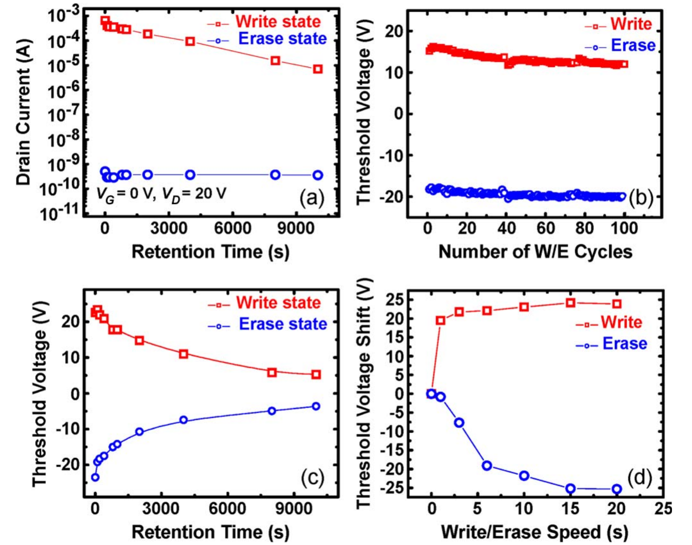

Fig. 2. (a) Monitored I_D of a-IGZO TFT after writing/erasing. (b), (c), and (d) Endurance characteristics, data-retention characteristics, and write/erase speeds of the proposed memory.

(L) and channel width (W) of the device were fixed at 400 and 1000 μm, respectively. A low-pressure mercury lamp, whose main emission line had a wavelength of 254 nm, served as the UV light source. The power density on the surface of the sample was around 0.1 mW/cm^2.

III. Results and Discussion

Fig. 1(b) and (c) shows the transfer characteristics of the a-IGZO TFTs as fabricated (unannealed) and when annealed, respectively. After annealing, the shallow acceptor states (tail states) are reduced. The degraded subthreshold slope (SS) after annealing may relate to the increase in deep states, but the mechanism requires further investigation. Both of the devices were subjected to measurements using a positive V_G pulse (50 V, 20 s) and a negative V_G pulse (-50 V, 20 s). The unannealed device exhibited great endurance under the negative V_G stress but high sensitivity to the positive V_G stress, which shifted the V_{TH} beyond the scope of measurement. By contrast, the annealed device exhibited adequate stability under the positive V_G stress but a slightly degraded stability under the negative V_G stress.

A post-annealing treatment can noticeably improve the stability of IGZO TFTs by reducing the electron trap defects [4]. For the proposed light-erasable memory, the writing (increasing V_{TH}) and erasing (decreasing V_{TH}) were performed using, respectively, a positive V_G pulse (50 V, 20 s) unaccompanied and a negative V_G pulse (-50 V, 20 s) accompanied by UV illumination. Fig. 1(d) and (e) shows, respectively, the transfer characteristics of the unannealed and annealed devices after several writing/erasing cycles. For the unannealed device, the V_{TH} position can be controlled as required by either writing or erasing. As shown in Fig. 1(d), the unannealed device was: 1) placed in the low state by writing, 2) transferred to the high state by erasing, and 3) transferred back to the low state by writing. The difference in V_{TH} between the low and high states (the V_{TH} window) of the light-erasable memory was around 30 V. As shown in Fig. 1(e), the electron trap defects were decreased by thermal annealing, so the writing operation was invalid for the annealed device. That is, the annealed device can only be erased, not written, and therefore cannot serve as a memory. Furthermore, the dotted curve in Fig. 1(d) was obtained by applying UV illumination following a writing operation and shows that UV illumination alone can reduce the trapping of electrons. This property would be useful for application of the device in a photodetector.

Fig. 2(a) shows the duration characteristics of the light-erasable memory after writing (50 V, 20 s) and erasing (UV on, -50 V, 20 s). The drain current was monitored continuously for 10 000 s with $V_G = 0$ and $V_D = 20$ V. The channel conductance produced by either writing or erasing could be well maintained for at least 10 000 s. An on/off ratio greater than 10^4 was recorded. Fig. 2(b) and (d) shows the endurance characteristics, data-retention characteristics, and write/erase speeds of the proposed memory, respectively. Before measuring the endurance characteristics, the UV intensity was tuned slightly to balance the responses of the writing and erasing operations. With a conventional a-IGZO TFT structure, the proposed memory device possesses a V_{TH} window of around 10 V when the retention time is 10 000 s. The writing action is due not to the release of trapped holes but to the generation of additional trapped electrons. For annealed devices, the difficulty to generate trapped electrons makes the device unwritable.

Because UV illumination of a-IGZO TFTs can suppress the effect of writing, a UV detector can be realized by operating

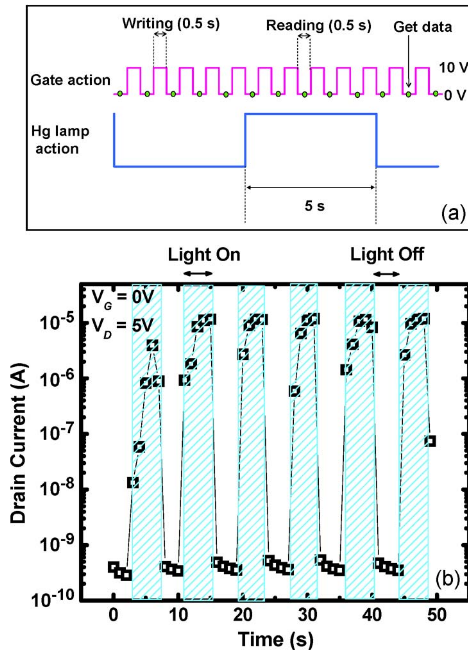

Fig. 3. (a) Action scenarios of V_G and UV lamp. (b) Temporal evolution of I_D for a-IGZO under flashing UV illumination.

an a-IGZO TFT in a cycle that alternates between writing and reading. Writing is used to keep the conductance low during the period without the UV, which can promptly switch off the photocurrent. Fig. 3(a) shows the action scenarios of the V_G and the UV lamp. The V_G of the IGZO TFT was periodically switched to alternate between reading ($V_G = 0$ V, 0.5 s) and writing ($V_G = 10$ V, 0.5 s). Meanwhile, the UV lamp was flashed with a light period of about 5 s. Fig. 3(b) shows the temporal evolution of I_D for the IGZO TFT under the flashing UV illumination, where I_D was recorded at the reading stage for a V_D of 5 V. The proposed UV detector responded promptly to each illumination change, with a light/dark ratio of 10^4. There have been many previous studies of UV detectors based on zinc oxide (ZnO). However, phototransistors generally exhibit lower real-time light/dark ratios [13], so high-performance devices (with light/dark ratios from 10 to 3×10^3) are realized only when complicated ZnO nanowires are used [14], [15].

A positive V_G is applied to produce electron trapping [4] at the dielectric surface, resulting in a positive $\Delta V_{\rm TH}$. Abundant electron trap defects, which can serve as electron storage centers, are intrinsically present in the as-deposited IGZO TFT. Furthermore, the trapped electrons can be untrapped by UV illumination. A negative V_G accompanied by UV illumination is applied to produce hole trapping [12] at the dielectric surface, resulting in a negative $\Delta V_{\rm TH}$. However, most trapped holes cannot be untrapped by a subsequent writing operation, which indicates that trapped holes and electrons may possibly coexist in the dielectric.

IV. Conclusion

This letter has proposed two potential applications for the a-IGZO TFT: a light-erasable memory and a real-time UV detector. An a-IGZO TFT can be fabricated at room temperature without the burden of post-annealing, because the intrinsic defects serve as electron traps. A negative V_G pulse accompanied by UV illumination can be regarded as the erasing operation. A light-erasable memory was demonstrated that offered a $V_{\rm TH}$ window of 30 V and exhibited an on/off ratio of 10^5. UV not only enhanced the effect of negative V_G stress but also suppressed the effect of positive V_G stress. A real-time UV detector was also demonstrated that operated in a mode of alternate writing and reading states and exhibited a light/dark ratio of 10^4.

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