Solid-Duty-Control Technique for Alleviating the Right-Half-Plane Zero Effect in Continuous Conduction Mode Boost Converters

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***Abstract*—This paper proposes a solid-duty-control (SDC) technique for application in boost converters to maintain a constant duty value and reduce dip voltage during load transient periods. Fast transient response was also achieved because of the variable transient enhancement controller. The proposed SDC technique can provide a stable and regulated output for edge-lit light-emitting diode backlight systems. This converter was used in a 0.25-μm CMOS process. Experimental results show that compared with a conventional design without a fast transient technique, the proposed approach yields about 30% and 80% improvement in undershoot voltage and recovery time, respectively, as load current changes from 50 to 250 mA.**

***Index Terms*—Adaptive off-time., alleviating skill, boost converter, dc–dc converter, light-emitting diode (LED), right-half-plane (RHP), solid duty control, valley current control.**

I. Introduction

THE CURRENT trend in the development of current liquid crystal display (LCD) panels is geared toward weightlessness and thinness. In this regard, edge-lit light-emitting diode (LED) backlight configuration has become a popular technique applied to medium- and small-size LCDs [1]–[3]. Fig. 1(a) illustrates a conventional block diagram of an LCD TV with edge-lit LED backlight units containing three LED colors. To obtain perfect image quality, light guides in the edge-lit LED backlight are designed to prevent total internal reflection and uniformly distribute light emitted from the LED sources across the light-guide surface [4]–[7]. Furthermore, the LED backlight driver, which is composed of boost converters, must be able to handle the requirements of fast transience, high stability, power efficiency, and space minimization to handle large instant load variations without sacrificing image quality and increasing motion blur effects [8]–[10]. The conventional current-mode boost converter contains one dominant pole and two zeros, the right-half-plane (RHP) and left-half-plane (LHP) zero. However, the RHP zero results in a tradeoff between fast transient response and system stability in the boost converters, which operate in (CCM) [11], [12].

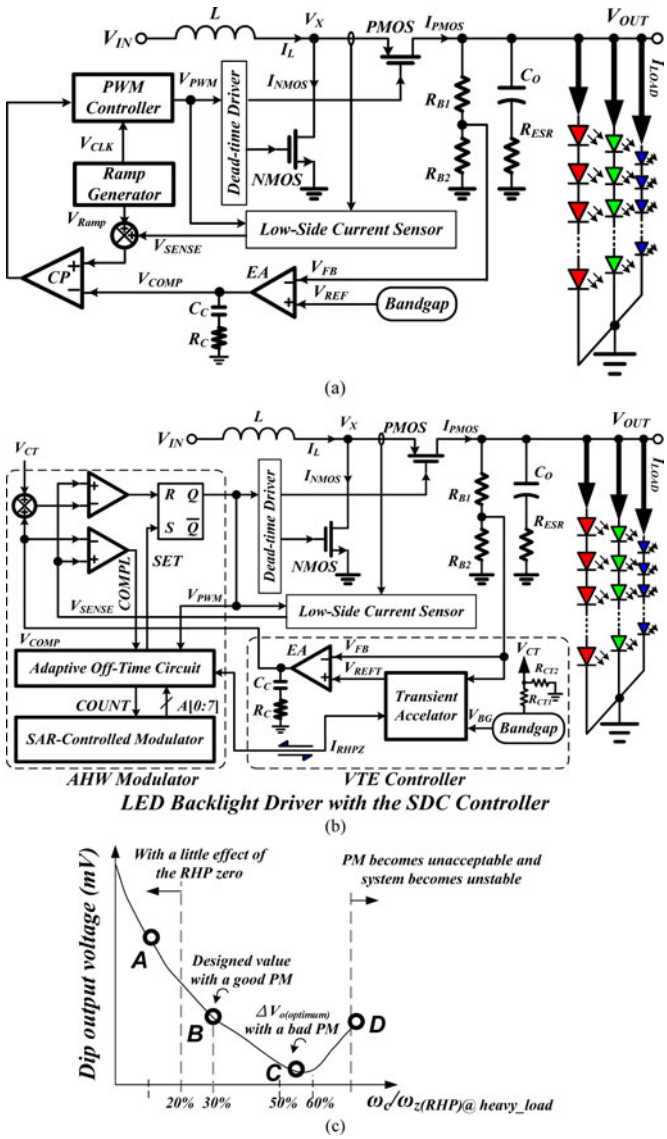

Fig. 1. (a) Conventional current-mode boost converter. (b) Proposed boost converter with SDC controller containing the AHW and VTE controllers. (c) Selection of the RHP zero can simultaneously ensure transient response and system stability.

A number of previous studies have mentioned the existence of the RHP zero that limits the system bandwidth because of system stability considerations [13]–[16]. In conventional design, the

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relationship between the crossover frequency and the RHP zero enables the tradeoff between transient response and the system stability [see Fig. 1(c)]. The crossover frequency is generally designed to be smaller than 10–20% of the ω_{RHPZ} at heavy loads. Point A shown in Fig. 1(c) is slightly influenced by the RHP zero on the phase margin, but the transient response time considerably slows down. As a result, the output voltage of the system has a large dip voltage when load current variations occur because of the limited system bandwidth. If the crossover frequency is designed as point B in Fig. 1(c), the RHP zero imposes a serious effect on the drop of the output voltage when load transient occurs. However, the higher crossover frequency can ensure that the dip voltage is smaller than that at point A. The designed value is usually located at point B.

Conversely, the discontinuous conduction mode in conventional boost converter design is widely used in obtaining simple compensation because the RHP zero appears at high frequencies [17], [18]. However, the slow response cannot satisfy the requirements of LED backlight systems.

This paper presents a solid-duty-control (SDC) technique for application in a boost converter with CCM operation [see Fig. 1(b)] to alleviate the effects of the RHP zero and improve transient response time. As a result, high bandwidth and fast transient response can be achieved simultaneously. The rest of the paper is arranged as follows. The methodology of SDC control is introduced in Section II. Section III presents the operation of the proposed SDC boost converter. The implementation of the proposed variable transient enhancement (VTE) circuit and adaptive hysteresis window (AHW) modulator is illustrated in Section IV. Experimental results shown in Section V demonstrate the advantages of the SDC control technique. Finally, the conclusions drawn are presented in Section VI.

II. Design of the SDC Technique

The duty ratio that changes during the load transient period results in a larger output voltage drop because the RHP zero moves toward the origin. Therefore, the SDC method is proposed to decrease the output voltage drop by keeping the duty ratio constant. That is, the SDC method can reduce the RHP effect because of the extension of the on-time and off-time periods during the load transient period.

A. Analysis in the Time Domain

As illustrated in Fig. 2(a), the voltage variation on the output capacitor during the on-time and off-time periods can be expressed as (1) and (2), respectively [19]. Fig. 2(b) shows the timing diagrams of the voltage and currents related to Fig. 2(a):

$$V_{C_O\_\mathrm{ontime}} = \frac{I_{\mathrm{Load}}}{C_O} D T_S \tag{1}$$

$$V_{C_O\_\mathrm{offtime}} = \frac{(I_L - I_{\mathrm{Load}})}{C_O} D' T_S. \tag{2}$$

Here, I_L is the inductor average current during the off-time period. Therefore, the total voltage drop on in the output capacitor C_O during one switching period T_S can be expressed as

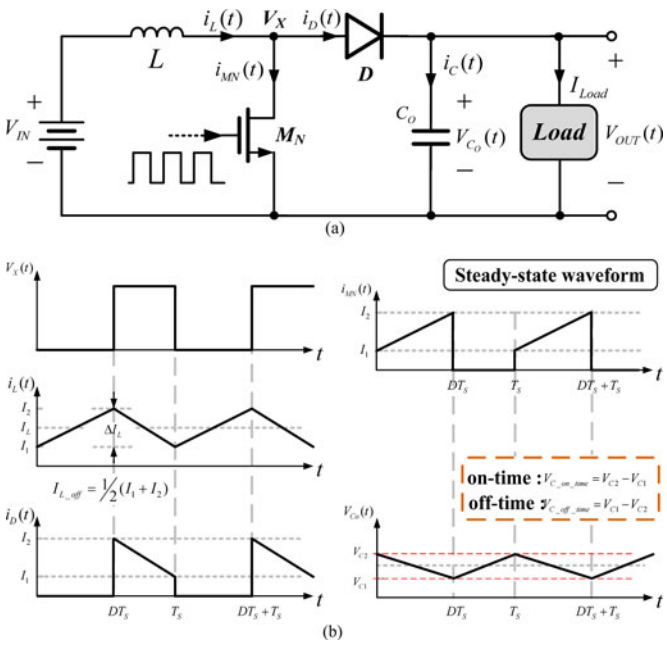

Fig. 2. (a) Boost converter scheme. (b) Timing diagram of some important waveforms.

$$\begin{aligned}\Delta V_{C_O} &= -V_{\mathrm{drop}} = V_{C_O\_\mathrm{offtime}} - V_{C_O\_\mathrm{ontime}} \\ &= \frac{T_S}{C_O}\left(D' I_L - I_{\mathrm{Load}}\right). \end{aligned} \tag{3}$$

The proposed SDC method extends the on-time and off-time periods by the same ratio during transient response to ensure that the duty ratio is kept constant (see Fig. 3). Assume that the switching period is changed from T_s to mT_{sI}, where "m" is the extended time ratio for on-time and off-time values for simplicity. The voltage drop on the output capacitor can then be expressed as

$$\begin{aligned}\Delta V_{C_O\_\mathrm{tran}_n} &= -\Delta V_{\mathrm{drop\_SDC}_n} \\ &= \frac{T_{S_n}}{C_O} \cdot \left[I_{L\_\mathrm{offtime}_n} D'_n - I_{\mathrm{Load}_n}\right] \end{aligned} \tag{4}$$

where

$$\begin{aligned} I_{L\_\mathrm{offtime}_n} &= \frac{1}{2}(I_2 + I_3) = I_L - \frac{\Delta I_L}{2} + \frac{1}{2}\frac{V_{\mathrm{IN}} D_n T_{S_n}}{L} \\ &\quad + \frac{\Delta V_{\mathrm{out}_n}}{L} D'_n T_{S_n} \end{aligned}$$

and

$$\Delta V_{\mathrm{out}_n} = \frac{I_L D'_{n-1}}{C_O}\left[D_n k T_{S_n} - D_{n-1} T_{S_{n-1}}\right].$$

Hence, the voltage drop on the output capacitor C_O with the SDC method can be rewritten as (5), where k is the change ratio

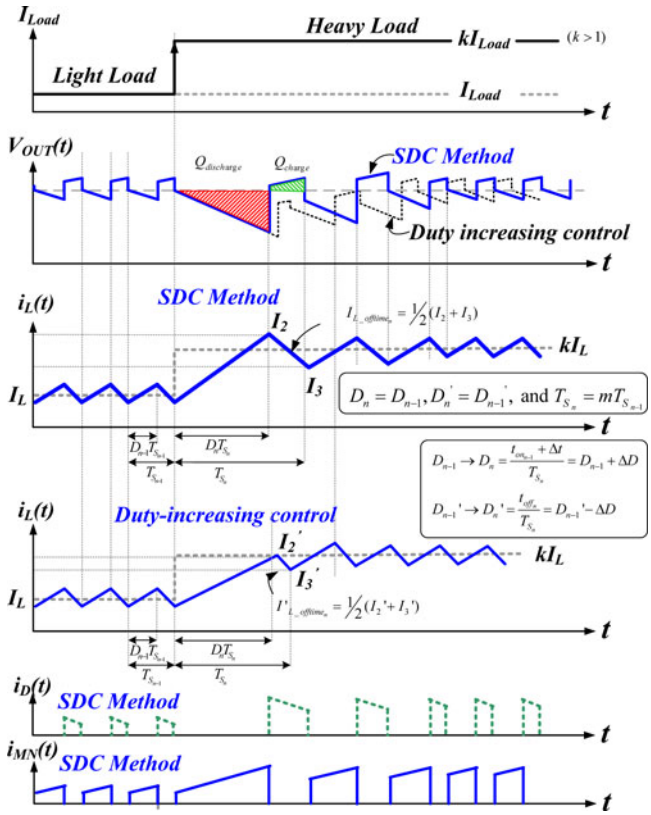

Fig. 3. Waveforms of inductor current, diode current, power MOSFET current, and output voltage in the SDC control method and inductor current of the duty-ratio increasing control.

of the load current.

$$\Delta V_{C_O\_\mathrm{tran}_n} = -\Delta V_{\mathrm{drop\_SDC}_n} = \frac{mT_{S_{n-1}} D'_{n-1}}{C_O} \times \left[\frac{V_{IN} D_{n-1} T_{S_{n-1}}}{2L} (m-1) - I_L (k-1) + \frac{mI_L D_{n-1} \left(D'_{n-1} T_{S_{n-1}}\right)^2}{2LC_O} (mk-1) \right]. \quad (5)$$

Compared with the control with an increasing duty ratio from D to $D + \Delta D$ in the transient period, the switching period simultaneously increases and results in the voltage drop that can be expressed as

$$\Delta V_{C_O\_\mathrm{tran}_n} = -\Delta V_{\mathrm{drop\_}D\text{-increasing}_n} = \frac{T_{S_n}}{C_O} \times \left[I'_{L\_\mathrm{offtime}_n} D'_n - I_{\mathrm{Load}_n} \right] \quad (6)$$

where

$$I'_{L\_\mathrm{offtime}_n} = I_L + \frac{V_{\mathrm{IN}}}{2L} \cdot \left[D_n T_{S_n} - D_{n-1} T_{S_{n-1}} \right] + \frac{\Delta V_{\mathrm{out}_n} D'_n T_{S_n}}{2L}$$

$$\Delta V_{\mathrm{out}_n} = \frac{I_L D'_{n-1}}{C} \cdot \left[D_n k T_{S_n} - D_{n-1} T_{S_{n-1}} \right].$$

Thus, the voltage drop across the output capacitor C_O with the duty-ratio increasing control can be rewritten as

$$\Delta V_{C_O\_\mathrm{tran}_n} = -\Delta V_{\mathrm{drop\_}D\text{-increasing}_n} = \frac{mT_{S_{n-1}}}{C_O} \left\{ \frac{V_{IN} T_{S_{n-1}}}{2L} \left[D_{n-1}(m-1) + m\Delta D \right] \cdot \left(D'_{n-1} - \Delta D \right) + I_L \left[(1-k) D'_{n-1} - \Delta D \right] + \frac{\left(D'_{n-1} - \Delta D \right) mT_{S_{n-1}}}{2L} \cdot \frac{I_L D'_{n-1} T_{S_{n-1}}}{C_O} \times \left[km(D'_{n-1} + \Delta D) - D_{n-1} \right] \right\}. \quad (7)$$

To identify a range of "m" so that the voltage drop value in the SDC method is less than that in the duty-ratio increasing control in transient period. That is, the difference between (5) and (7) must be larger than or equal to zero. Therefore

$$\Delta V_{\mathrm{drop\_}D\text{-increasing}_n} - \Delta V_{\mathrm{drop\_SDC}} \geq 0. \quad (8)$$

Substituting (5) and (7) into (8), the lower bound of the extension ratio of the on-time or off-time period can be derived as

$$m \geq \frac{D_{n-1} - (2LI_L / V_{\mathrm{IN}} T_{S_{n-1}})}{2D_{n-1} + \Delta D - 1}. \quad (9)$$

To minimize the settling time in the SDC method, the charge on the output capacitor during the on-time period is equal to the off-time period in case of transient period ($Q_{\mathrm{discharge}} = Q_{\mathrm{charge}}$). Hence, (5) must be set to zero. The upper bound of "m" can be derived as

$$m \leq 1 + \frac{2I_L L (k-1)}{V_{\mathrm{IN}} D_{n-1} T_{S_{n-1}}}. \quad (10)$$

Finally, the summary of the range for "m" can be expressed as

$$\frac{D_{n-1} - (2LI_L / V_{\mathrm{IN}} T_{S_{n-1}})}{2D_{n-1} + \Delta D - 1} \leq m \leq 1 + \frac{2I_L L(k-1)}{V_{\mathrm{IN}} D_{n-1} T_{S_{n-1}}}. \quad (11)$$

Therefore, the following implementation is based on the design value to satisfy the requirements defined by (11). Moreover, assume that factor "m" is at least larger than one, and that the design value of the switching frequency must be at least larger than the expression shown in

$$F_{S_{n-1}} \geq \frac{V_{\mathrm{IN}} \cdot [1 - (D_{n-1} + \Delta D)]}{2LI_L}. \quad (12)$$

B. Analysis in the Frequency Domain

The small-signal model of the conventional current-mode boost converter is illustrated in Fig. 4 and the control-to-output transfer function is shown in (13) [19]. R is the output resistance, R_f denotes the current sensing gain, and R_{ESR} represents the

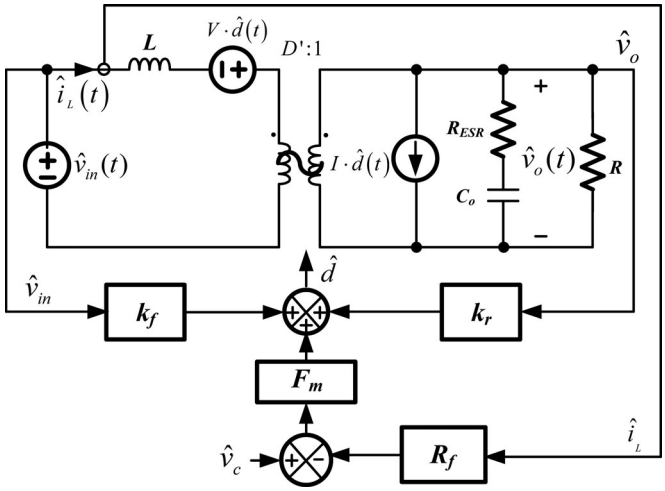

Fig. 4. Small-signal model of the conventional current-mode boost converter.

equivalent series resistance of output capacitor C_O:

$$G_{vc} = \frac{\hat{v}_o}{\hat{v}_c} = \frac{1}{R_f}\frac{G_{vd}}{G_{id}} = G_{vc0}\frac{\left(1-(s/\omega_{z(\mathrm{RHP})})\right)\left(1+(s/\omega_{z(\mathrm{ESR})})\right)}{(1+(s/\omega_{p1}))} \quad (13)$$

where

$$G_{vd} = \left.\frac{\hat{v}_o}{\hat{d}}\right|_{\hat{v}_{\mathrm{in}}=0} = \frac{V_o}{D'}\cdot\frac{\left(1-s(L/D'^2R)\right)(1+sR_{\mathrm{ESR}}C_o)}{1+s(L/RD'^2)+s^2(LC_o/D'^2)},$$

$$G_{id} = \left.\frac{\hat{i}_L}{\hat{d}}\right|_{\hat{v}_{in}=0} = \frac{2\cdot V_o}{D'^2R}\cdot\frac{(1+s(RC_o/2))}{1+s(L/RD'^2)+s^2(LC_o/D'^2)}$$

$$G_{vc0} = \frac{D'R}{2R_f}, \quad \omega_{p1} = \frac{2}{RC_o}, \quad \omega_{z(\mathrm{RHP})} = \frac{D'^2R}{L},$$

$$\text{and} \quad \omega_{z(\mathrm{ESR})} = \frac{1}{R_{\mathrm{ESR}}C_o}. \quad (14)$$

The control-to-output transfer function contains one dominant pole ω_{p1} and two zeros, which include one RHP zero $\omega_{z(RHP)}$ and one LHP zero $\omega_{z(ESR)}$. Moreover, the decrease in the value *D'* caused by the load transient response pushes the RHP zero toward the origin. This push results in a large dip voltage, which is the reason for keeping the duty ratio constant to cancel the effects of the RHP zero. Thus, the SDC method can improve the performance of the boost converter compared with the conventional design.

The proportional-integral (PI) compensation with a transfer function as shown in (15) is typically used to compensate for the system, with G_{c0} being the low-frequency gain of the PI compensator [20], [21]. Compensation zero ω_{zc1} is used to cancel the effect of ω_{p1}, while compensation pole ω_{pc1} forms the new dominant pole to determine the system bandwidth. The role of ω_{pc2} is used to decrease the high-frequency gain affected by the existence of $\omega_{z(\mathrm{RHP})}$. Through the constant duty ratio and high-frequency compensation pole, the effect of the RHP zero can be effectively canceled:

$$G_c = G_{c0}\frac{(1+(s/\omega_{zc1}))}{(1+(s/\omega_{pc1}))(1+(s/\omega_{pc2}))}. \quad (15)$$

III. Proposed SDC Controller

To cancel the RHP zero effect and achieve faster transient response for reliable system stability, the proposed boost converter utilizes the SDC technique, which contains an AHW modulator and a VTE controller [see Fig. 1(b)].

The hysteresis window is formed by the value of V_{CT}, which is generated by the voltage divider from the bandgap circuit and limits the output ripple within the hysteresis window [22]. Under heavy load conditions, the on-time period suddenly increases, whereas the off-time period decreases. The energy delivered to the output decreases in the beginning, causing the output to undergo a considerably large voltage drop. After the inductor current increases to a higher value, the output voltage can be restored to its regulated value. In other words, the RHP zero effect induces a large dip in the voltage and long transient response. Thus, the SDC controller includes the VTE controller to decrease the drop voltage and transient response time.

As shown in Fig. 5(a), the increasing on-time results in the off-time and the energy delivered to the output initially decreases in the conventional design when load current changes from light to heavy. Output voltage $V_{\mathrm{OUT(conv.)}}$ exhibits a large voltage drop because the RHP zero causes the output to initially lean toward the wrong direction during the transient period. The AHW modulator keeps the duty ratio constant during the load transient period because the increasing on-time accompanies the increasing off-time. Therefore, output voltage $V_{\mathrm{OUT(proposed)}}$ exhibits a smaller dip voltage compared with those in conventional designs. That is, the AHW technique reduces the RHP zero effect. However, the transient response time does not change because of the identical bandwidths. The proposed VTE controller instantly increases the slope of the hysteresis window to further increase the speed of the transient response. As depicted in Fig. 5(b), the inductor current can be raised to the rated value to reduce transient response time.

IV. Circuit Implementation

In the proposed SDC controller, the basic submodules contain the AHW modulator and VTE controller to keep a nearly constant duty ratio and a fast transient response, respectively.

A. AHW Modulator

Fig. 6(a) illustrates the AHW modulator. According to the successive approximation register conversion, the adaptive off-time is controlled by capacitor array C_{off} to decide off-time t_{off} [23]. The controller bits [see Fig. 6(b)] can decide a suitable value for the charging capacitor to determine value t_{off}. In the steady state, t_{off} is kept constant. In the design of a conventional boost converter, once the load current changes, the value of t_{off} decreases because of the effect of the RHP zero. As a result, a large voltage drop occurs because the output obtains less energy

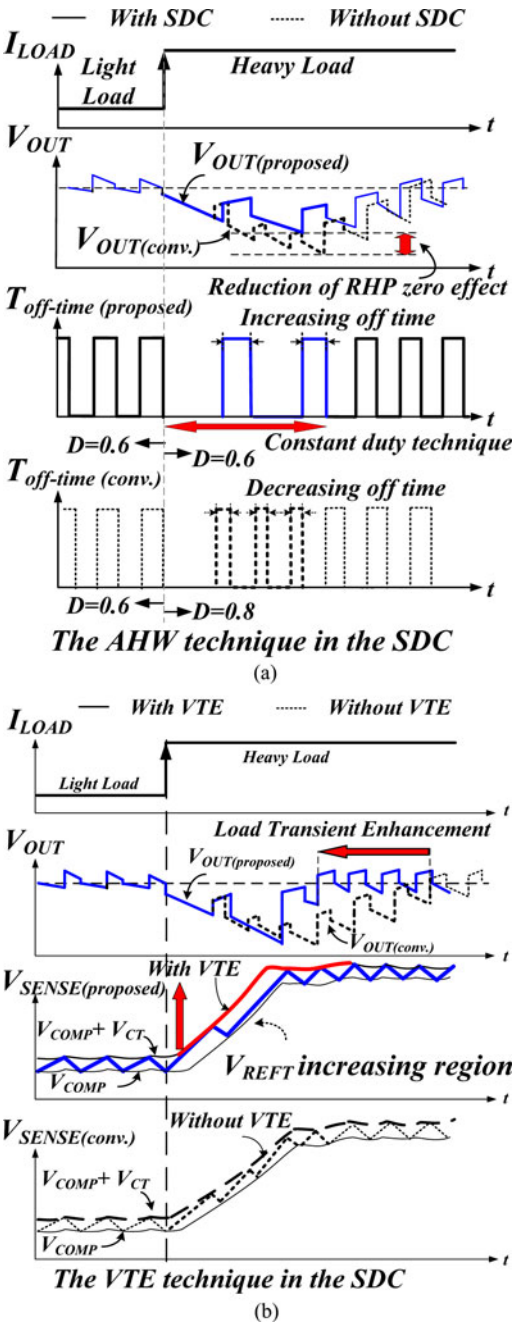

Fig. 5. Reduction in voltage drop and transient response are achieved using the AHW modulator and VTE controller, respectively.

from the input voltage source towing to the decrease in the off-time period.

Therefore, the AHW modulator prolongs $t_{\rm off}$ through decreasing charging current "$I_{\rm CONST} - I_{\rm RHPZ}$," and increases V_R because of the injection of $I_{\rm RHPZ}$. $t_{\rm off}$ is controlled by RHP zero control current $I_{\rm RHPZ}$ that stems from the VTE controller [see Fig. 7(a)]. As a result, the AHW modulator can ensure that the duty ratio cycle is kept constant even during the load transient period. The RHP zero effect can be effectively alleviated to guarantee low dip voltage during the load transient period. Furthermore, the duty ratio is kept nearly constant using the

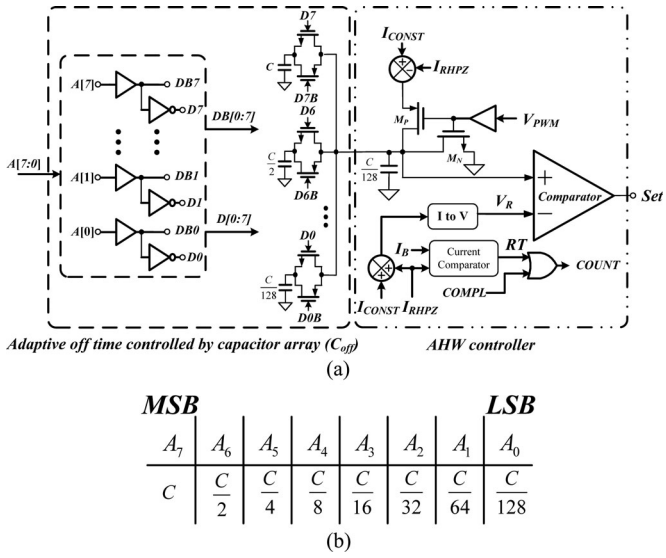

Fig. 6. (a) Schematic of the AHW modulator with adaptive off-time controller. (b) Controlling bits for determining the value of the charging capacitor.

AHW modulator. However, the switching frequency decreases, causing a slow transient response time. Thus, accelerating the transient response using the VTE controller is necessary for enhancing the performance of the SDC controller.

B. VTE Controller

To implement the RHP zero control current, the VTE controller is proposed to keep the duty ratio constant during the load transient period. Here, the G_m amplifier [see Fig. 7(b)] converts the voltage difference between $V_{\rm REF}$ and $V_{\rm FB}$ to three current signals, $I_{\rm OUT1}$, $I_{\rm OUT2}$, and $I_{\rm RHPZ}$ [21], [24]. $I_{\rm OUT1}$ flows through resistor R_1 to form two threshold voltages, V_H and V_L. Current signal $I_{\rm OUT2}$ is compared with a predefined constant current I_B to decide the starting time of the transient period. During the transient period, reference voltage $V_{\rm REF}$ changes from V_L, which is designed equal to $V_{\rm BG}$ here, to V_H. This change causes the reference voltage (which is connected to the noninverting terminal of the error amplifier) to increase, thereby effectively enhancing the performance of the transient response. This is particularly true for the high-speed current comparator, which is accelerated because of the shunt–shunt feedback resistor formed by transistor M_{N4}. In turn, this allows transistor M_{N4} to rapidly decide on the beginning condition of the transient response and further alleviate the effect of the RHP zero. Fig. 7(c) shows the waveforms with and without the VTE controller. The figure shows that the transient performance of the load transient response can be effectively improved.

V. Experimental Results

The proposed SDC controller for edge-lit LED backlight systems was fabricated via the TSMC 0.25μm BCD process. Fig. 8 shows the chip micrograph with a silicon area of 2.16 mm^2. The LED driver provides a 12-V regulated output voltage with a maximum loading current of 250 mA.

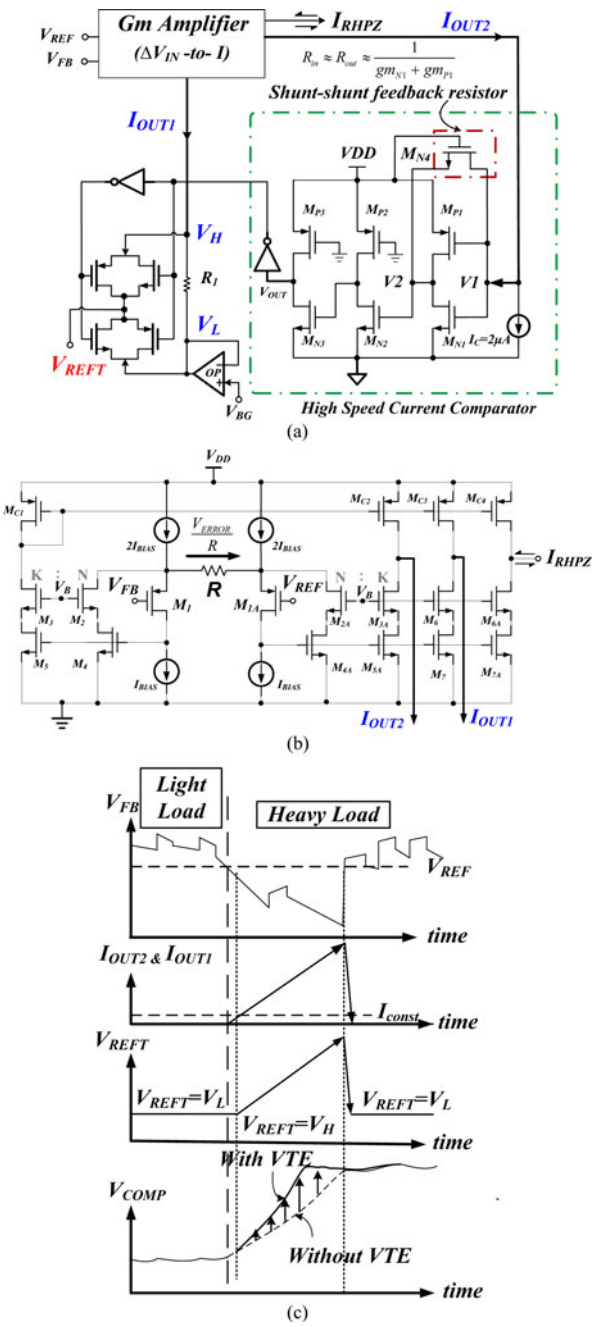

Fig. 7. (a) Structure of the VTE controller. (b) Schematic of the G_m amplifier. (c) Improved performance during load transient response caused by the VTE controller.

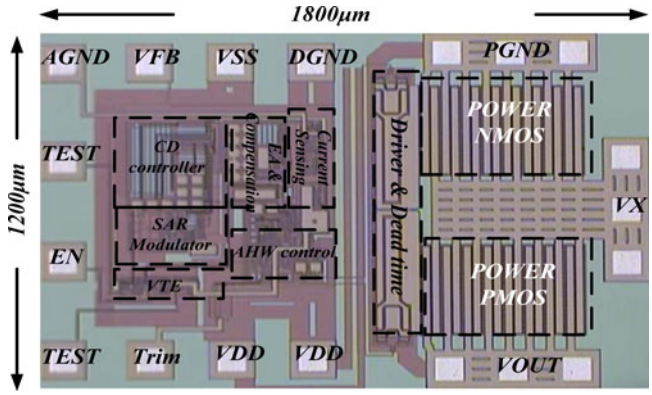

Fig. 8. Chip micrograph.

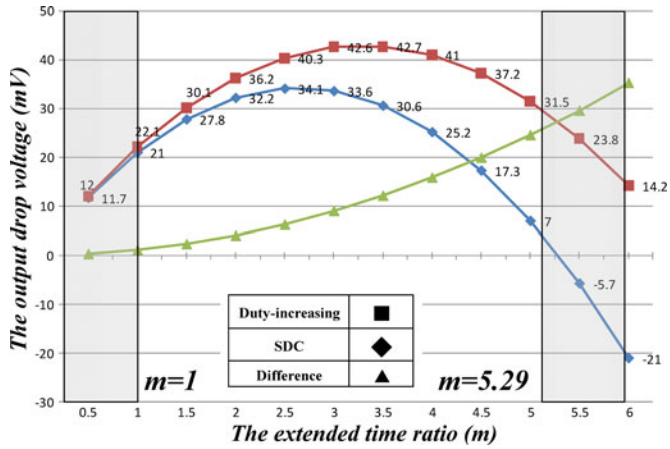

Fig. 9. Simulation and calculation results during the first load transient period.

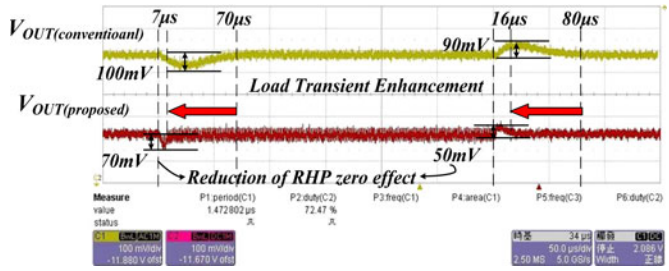

Fig. 10. Load transient response under a 200-mA load current variation in the conventional and proposed techniques.

To realize effect "m" in decreasing the $V_{\rm OUT}$ drop, the boost converter is tested with $V_{\rm IN} = 4$ V, $V_{\rm OUT} = 12$ V; thus, D is 2/3. Inductor L is 6.8 μH and output capacitor C_O is 6.8 μF. The operation switching frequency is 1.4 MHz. Here, the load current changes from 50 to 250 mA and vice versa. That is, the value of k is 5. According to the derived equations, the range of factor "m" ranges from 1 to 5.29. The simulation and calculation results during the first period are shown in Fig. 9. The larger the ratio factor "m" chosen, the lesser is the switching frequency occurring during the load transient period. A reasonable limitation on crossover frequency ω_c should be below 1/10 of the switching frequency to reduce the switching output ripples. Thus, the value of "m" cannot be increased to a large value because this can impose a serious effect on system stability. On the other hand, as the switching frequency decreases, more issues related to switching noise arise. In other words, the value of "m" should be decreased to enhance system stability.

Fig. 10 shows the experimental results that include the output voltage of the proposed technique compared with the conventional pulsewidth modulation boost converter when load changes from 50 to 250 mA and vice versa. The undershoot voltages of the conventional and proposed techniques are 100 and 70 mV, respectively. The overshoot voltages of the conventional and proposed techniques are 90 and 50 mV,

TABLE I
SUMMARY OF COMPARISON

	Ref. [10]	Ref. [24]	Ref. [25]*	Ref. [26]	Ref. [27]	This Work
Input voltage	8–13.5 V	3.05–5.5 V	5 V	0.8–2.4 V	0.9–1.2 V	2.7–4.3 V
Output voltage	16–30 V	5.6–25 V	1.5V	1.8–3.3 V	2.5 V	12 V
Switching frequency	1.5 MHz	0.9/1.2/1.8 MHz	300 kHz	300–700 kHz	667 kHz	1.4 MHz
Output capacitor	4.7 μF	4.7 μF	200 μF	NA	4.7 μF	6.8 μF
Load transient response (light to heavy)/(heavy to light)	20 μs/NA @$\triangle I_o$ = 80 mA	25/50 μs @$\triangle I_o$ = 120mA	150/200 μs @$\triangle I_o$ = 10A	50/50 μs @$\triangle I_o$ = 100mA	10/7 μs @$\triangle I_o$ = 100mA	7/16 μs @$\triangle I_o$ = 200mA
Output voltage drop/loading variation	30 mV/80 mA	2 V/120 mA	200 mV/10 A	38 mV/100 mA	50 mV/100 mA	70 mV/200 mA
Load regulation	0.5 mV/mA @V_{in} = 12 V, V_{out} = 21 V	11 mV/mA @ V_{in} = 3.6 V, V_{out} = 25 V	0.02 mV/mA @ V_{in} = 5 V V_{out} = 1.5 V	0.38 mV/mA @ V_{out} = 3.3 V	0.046 mV/mA @ V_{in} = 0.9 V	0.1 mV/mA @ V_{in} = 3 V, V_{out} = 12 V
Chip area with pads	6.178 mm^2	0.34 mm^2	NA	2.09 mm^2	3 mm^2	2.16 mm^2

*Reference [25] is a buck converter.

TABLE II
SUMMARY OF MEASUREMENT RESULTS

Process		TSMC 0.25 um 1P4M
Input voltage		2.7–4.3 V
Inductor/output capacitor		6.8 μH/6.8 μF
Switching frequency		1.4 MHz
Chip size		2.16 mm^2
Output		12 V
Proposed SDC technique	Recovery time (50 mA->250 mA)	7 μS **(10× fast)**
	Undershoot voltage $V_{undershoot}$	70 mV (0.7×)
	Recovery time (250 mA->50 mA)	16 μS **(5× fast)**
	Overshoot voltage $V_{overshoot}$	50 mV (0.56×)
Conventional method	Recovery time (50 mA->250 mA)	70 μS
	Undershoot voltage $V_{undershoot}$	100 mV
	Recovery time (250 mA->50 mA)	80 μS
	Overshoot voltage $V_{overshoot}$	90 mV

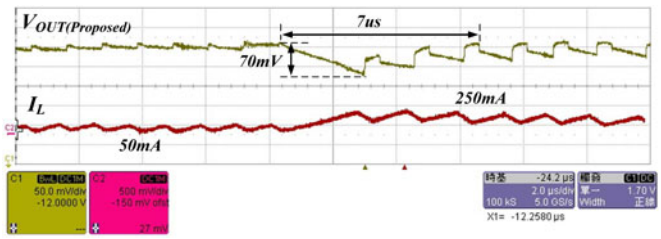

Fig. 11. Enlarged load transient waveforms can demonstrate the correct operation of the proposed technique.

respectively.The SDC controller can effectively reduce the transient dip voltage because of the constant duty ratio. Furthermore, the transient response time decreases from 70 to 7 μs when load current changes from 50 to 250 mA. Conversely, the recovery time decreases from 80 to 16 μs when load current changes from 250 to 50 mA. Table I shows that the SDC and VTE methods are more efficient than the previous approaches presented in [10], [24], and [25]–[27]. Fig. 11 enlarges the transient waveforms to demonstrate the correct operation of the proposed SDC controller. Table II shows the summary of the proposed SDC technique.

VI. CONCLUSION

In this paper, we proposed a solid-duty ratio-control technique for application in the boost converter that maintains the duty ratio at a constant level to reduce dip voltage during the load transient period. Fast transient response can also be achieved because of the VTE controller. For edge-lit LED backlight systems, stable and regulated output driving can be provided by the proposed SDC technique. Experimental results show that compared with the conventional design without a fast transient

technique, the proposed technique yields an enhancement of 30% and 80% for the undershoot voltage and recovery time, respectively.

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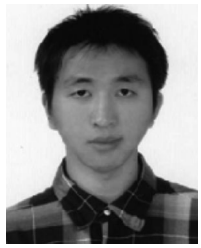

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