2.4-GHz Low-Noise Direct-Conversion Receiver With Deep N-Well Vertical-NPN BJT Operating Near Cutoff Frequency

Jin-Siang Syu, *Student Member, IEEE*, Chinchun Meng, *Member, IEEE*, and Chia-Ling Wang

***Abstract*—A 2.4-GHz low-power low-noise direct-conversion receiver is demonstrated using parasitic vertical-NPN bipolar junction transistors (BJTs) in a standard 0.18-μm CMOS process. The current switching operation of a Gilbert mixer with finite transistor cutoff frequency (f_T) is thoroughly analyzed and discussed in this paper. When the mixer operates near or higher than the transistor f_T, the loss of the polyphase filter due to the capacitive loading of the mixer is a main issue. Thus, BJT devices with smaller base resistance and an inductive peaking technique with symmetric 3-D realization are employed in this paper to reduce local oscillator power by 4.5 dB. At 2.4 GHz, the demonstrated receiver has conversion gain of 51 dB and noise figure of 3.2 dB with 70-kHz $1/f$ noise corner, while the current consumption is 4.5 mA at a 1.8-V supply.**

***Index Terms*—Direct-conversion receiver (DCR), polyphase filter (PPF), symmetric 3-D inductor, vertical-NPN (V-NPN).**

I. Introduction

BIPOLAR junction transistors (BJTs) have ultra-low $1/f$ noise, better device-to-device matching, and also larger transconductance (g_m) than MOS devices. Therefore, many RF transceiver chips have been fabricated using BiCMOS processes where the high-performance SiGe HBT is used for the RF circuit and CMOS for the logic circuits [1], [2]. However, the cost is high and access to the foundry process is quite limited. Continuous advances in CMOS technology provide both good RF circuits and digital very large scale integration (VLSI) at very low cost. For wireless communication applications, a direct-conversion receiver (DCR) has the highest integration level. However, a CMOS DCR has inherently serious problems of noise and dc offset because the MOS device has a very high $1/f$ noise corner and large mismatch. Conventionally, a passive mixer is widely chosen for a DCR due to its low $1/f$ noise property because no dc current flows through the switching core [3]–[10]. However, the conversion loss of the passive mixer core results in an urgent need of higher gain (i.e., higher power consumption) at the preceding low-noise amplifier (LNA) to compensate for the mixer loss to achieve a low noise figure (NF) for the receiver. In the previous literature [4], [5], a preceding g_m cell was placed between the LNA and passive mixer to compensate for the passive mixer loss, while the $1/f$ noise corner is kept low. Further, if an advanced technology is available [3], [4], e.g., 90- or 65-nm CMOS process, excellent noise performance can be easier to be achieved at a higher cost. Although a CMOS active mixer has sufficient gain due to the additional RF g_m stage, the several-megahertz $1/f$ noise corner is a critical weakness for a DCR, especially in a narrow IF band application. A longer gate length is chosen to guarantee sufficiently low $1/f$ noise, which is inversely proportional to the gate area $W \times L$ [11]. The flicker noise leaks to the IF port at the local oscillator (LO) zero-crossing intervals from the LO switching device. Thus, the dynamic current injection method [12] alleviates the direct mechanism of the $1/f$ noise contribution [11] by drawing out the biasing current of the LO switching devices at the zero-crossing. A CMOS current-reuse g_m stage can also be employed as a current bleeding topology with additional transconductor gain [13]. Further, the parallel inductors placed at the push–push nodes of the mixer switching core tune out the parasitic capacitance, and thus reduce the indirect mechanism of the $1/f$ noise contribution to mixer outputs [14].

A vertical-NPN (V-NPN) BJT can be obtained in a deep n-well CMOS process without an extra mask [15], [16] and its low $1/f$ noise performance is especially suitable for a DCR. As a result, V-NPN BJTs are used in this paper to directly eliminate the device $1/f$ noise source. However, the V-NPN BJT has a relatively low cutoff frequency (f_T). Thus, the current switching operation of a Gilbert mixer is fully analyzed, especially when the operating frequency is near or even higher than the transistor f_T. Besides, the LO polyphase filter (PPF) loss due to the capacitive load of the following mixer is also addressed. Finally, a pair of the fully symmetric 3-D inductors are used to improve both the mixer conversion gain (CG) and reduce the PPF loss.

The dc and RF performance of the parasitic V-NPN BJT in a standard low-cost 0.18-μm CMOS process are described in Section II. Circuit design of a low-power low-noise DCR using V-NPN BJTs is described in Section III, while Section IV reports the measurement results. Finally, conclusions are presented in Section V.

II. V-NPN BJT in Deep N-Well CMOS

Today, most of the state-of-the-art CMOS foundries provide deep n-well technology, which can provide excellent

Manuscript received April 02, 2011; revised August 28, 2011; accepted September 12, 2011. Date of publication October 24, 2011; date of current version December 14, 2011. This work was supported by the National Science Council of Taiwan, R.O.C., under Contract NSC 98-2221-E-009-033-MY3, Contract 99-2221-E-009-049-MY3, and Contract NSC 98-2218-E-009-008-MY3, and by the Ministry of Education (MoE) Aim for the Top University (ATU) Program under Contract 95W803.

The authors are with the Department of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: jssyu.cm95g@nctu.edu.tw; ccmeng@mail.nctu.edu.tw; hownfun.cm97g@nctu.edu.tw).

Digital Object Identifier 10.1109/TMTT.2011.2169421

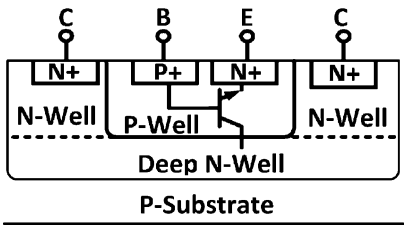


Fig. 1. Cross-section view of the V-NPN BJT in deep n-well 0.18-μm COMS process.

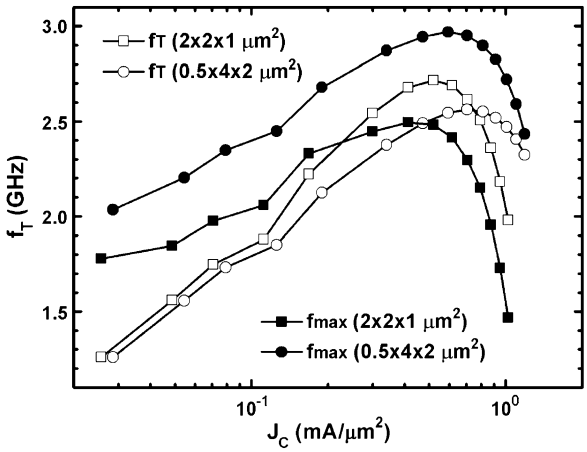


Fig. 2. Current cutoff frequency (f_T) and maximum oscillation frequency $(f_{\max})$ of the V-NPN BJT with two shapes, but the same emitter area of 4 μm^2.

isolation against the substrate coupling noise among and between digital baseband logic circuits and RF circuits. Besides, the V-NPN BJT can be obtained without extra cost from this deep n-well CMOS technology. The V-NPN BJT is composed of the source–drain diffusion as the emitter, the p-well diffusion as the base, and the deep n-well as the collector, as shown in Fig. 1. A deep-n-well V-NPN BJT provides not only lower collector resistance, but also thinner p-base thickness, both of which can lead to good BJT performance. The f_T and maximum oscillation frequency $(f_{\max})$ obtained from S-parameter measurements are drawn in Fig. 2. Two devices [(i) $W_E \times L_E \times n = 2 \times 2 \times 1$ μm^2, (ii) $W_E \times L_E \times n = 0.5 \times 4 \times 2$ μm^2 with identical emitter areas of 4 μm^2] are implemented and measured, where W_E, L_E, and n represent the emitter stripe width, emitter length, and number of emitter fingers, respectively. Fig. 2 indicates that the four devices with different layout shapes have similar f_T because of the same base thickness. On the other hand, $f_{\max} \approx \sqrt{f_T/(8\pi R_B C_C)}$, where $R_B = r_0 W_E/L_E$, $C_C = C_0 W_E L_E$, r_0, and C_0 are the intrinsic base resistance and collector capacitance per unit area. Thus, $f_{\max}$ can be rewritten as

$$f_{\max} \approx \frac{1}{2W_E}\sqrt{\frac{f_T}{2\pi r_0 C_0}} \tag{1}$$

which indicates the importance of emitter stripe width on $f_{\max}$ [17]. Thus, a V-NPN BJT with a rectangular emitter shape has a higher $f_{\max}$ than a V-NPN BJT with a square emitter, as shown in Fig. 2. Here, R_B (or $f_{\max}$) is noted in this paper because it affects the LO power loss, which will be described in Section III-C.

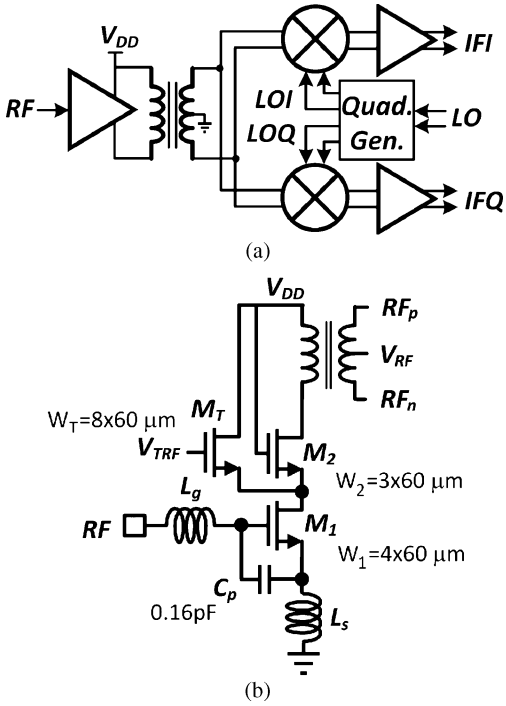


Fig. 3. (a) Block diagram of the DCR including LNA, I/Q mixers, I/Q VGAs, and an LO quadrature generator. (b) Schematic of the single-ended-input LNA with tuning transistor M_T and a single-to-differential transformer.

III. Circuit Design

Fig. 3(a) shows the block diagram of the DCR consisting of a single-in-differential-out LNA, in-phase/quadrature (I/Q) Gilbert mixers with the V-NPN BJT switching core, I/Q variable-gain amplifiers (VGAs), and an LO quadrature generator.

A. RF LNA and IF VGA

Many low-frequency (<2 GHz) LNAs have outstanding NF performance because the bond wires with high quality factor (Q) are used for off-chip matching [18], [19]. However, the wire-bonding has significant percentage error and it is difficult to mass produce. On the other hand, a receiver with fully integrated inductors can avoid the time-consuming off-chip tuning for every chip. However, the effect of the series resistance in low-Q inductors should be considered for NF optimization [20]. A parallel C_p, as shown in Fig. 3(b), can be placed to somewhat reduce the inductance of L_g at the cost of voltage gain [19]. A tuning transistor (M_T) is used to achieve gain reduction and avoid signal compression when a large RF signal is applied. The transistor M_T acts as a current switch that reduces the output signal by shunting the RF current away from the inductive load, as shown in Fig. 3(b). Note that the gain tuning approach using tunable M_T and fixed-biased M_2 is a prototype. The cascode device can be broken into more branches with weighted sizes (not only M_2 and M_T), and a more gentle slope of the tuning curve can be achieved by digitally switching on/off the bias of each branch [21]. In addition, a transformer is employed at the load of the cascode LNA to transform the single-ended input current to differential output voltage. The gate dc voltage of the g_m stage in I/Q mixers is fed from the center tap of the secondary coil in the transformer. Instead of a stacked transformer,

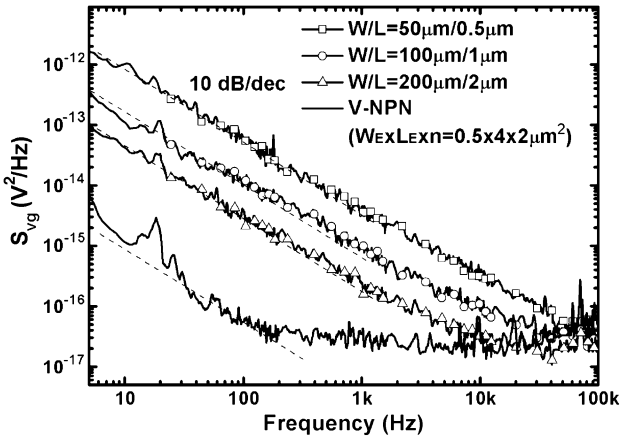


Fig. 4. Output noise current spectral density of V-NPN BJT and MOS devices. The dc current is 250 μA for the devices.

an interleave transformer is selected using both ultra-thick metal (UTM) layers with 2.34-μm thickness for low passive loss and a high Q. Thus, the turn ratio should be $n : n \pm 1$. After optimization for gain and NF, a 5:4 transformer is utilized with linewidth, line spacing, and outer diameter of 9, 2, and 290 μm, respectively.

On the other hand, an IF VGA with 20-dB linear-in-decibel tuning range is implemented using an $R-r$ attenuation method [22], [23]. In addition, the V-NPN BJTs are used at the input transconductance stage for excellent noise performance (including $1/f$ noise) and also a larger transconductance under the same dc current consumption when compared with nMOS transistors.

B. Gilbert Mixer Using V-NPN BJT in Switching Core

Fig. 4 shows the device input-referred noise voltage spectral density, measured by an Agilent 35670A dynamic signal analyzer, for pMOS devices [(i) $W/L = 50$ μm/0.5 μm, (ii) 100 μm/1 μm, (iii) 200 μm/2 μm] and V-NPN BJT with $W_E \times L_E \times n = 0.5 \times 4 \times 2$ μm^2. The $1/f$ noise corner ranges from 10 to 100 kHz for (i)/(ii)/(iii) devices and a wider gatewidth leads to a lower $1/f$ noise corner. By contrast, the V-NPN BJT has only around 200-Hz $1/f$ noise corner, while the advanced 0.18-μm nMOS device has around several-megahertz corner frequency under the same dc current of 250 μA. Thus, V-NPN BJTs are used in the LO switching core to guarantee a low $1/f$ noise corner, as shown in Fig. 5(a). Instead of a pure resistive load (without $1/f$ noise contribution), pMOS devices with a 2-μm gate length is applied for a more constant dc bias against process variation and still allowable $1/f$ noise performance. On the contrary, the high-performance, but high $1/f$ noise corner nMOS device can be used in the RF LNA and the RF g_m stage of the mixers because the low-frequency noise at the RF stage will be upconverted to the odd harmonics of the LO signals, not baseband, after the switching operation. Note that if there is dc offset in the mixer core, the $1/f$ noise of the g_m stage will still appear at the output [11]. However, in fact, the BJT core has good device matching and low dc offset [15]; thus, this phenomenon is not serious.

Although the V-NPN BJT in the mixer core has a 200-Hz $1/f$ noise corner, it has a relatively low f_T. Here, we stress

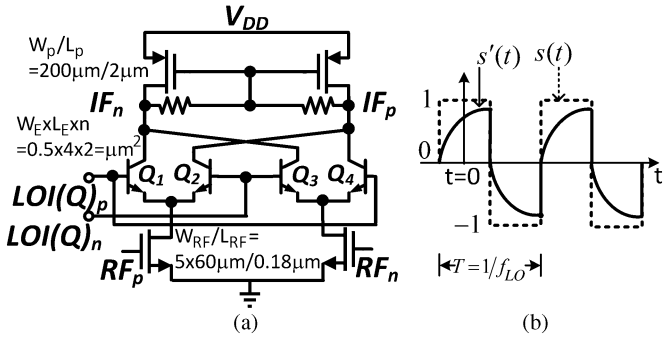


Fig. 5. (a) Schematic of the Gilbert mixer with V-NPN BJT in LO switching core. (b) LO switching function with infinite/finite f_T in large LO region.

the effect of the transistor f_T on the switching function. The BJT-based Gilbert cell has an exact mathematical expression of current switching function [24]

$$s(t) = \frac{i_{\text{out}}}{i_{\text{RF}}} = \tanh(u) \tag{2}$$

where $u = (V_{\text{LO}}/2V_T)\cos\omega_{\text{LO}}t$.

The small-signal CG of the current switching function can be computed as the mean dc output current when the input signal is $i_{\text{RF}} = \hat{i}_{\text{RF}} \cdot \cos(\omega_{\text{LO}}t)$

$$\text{CG} = \frac{\overline{i_{\text{out}}}}{\hat{i}_{\text{RF}}} = \frac{1}{T}\int_0^T s(t)\cos(\omega_{\text{LO}}t)dt. \tag{3}$$

The current switching function can be simplified for two extreme cases as follows:

$$s(t) = \begin{cases} \text{sgn}(u), & |u| \gg 1(\text{large LO}) \\ u, & |u| \ll 1(\text{small LO}). \end{cases} \tag{4}$$

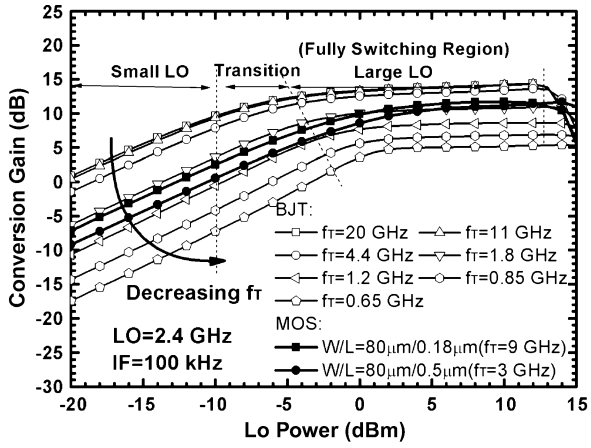
That is, the switching function of the mixing core in the large-LO (fully switching) region can be approximated as a square wave, drawn by the dotted line in Fig. 5(b). Therefore, the CG of the switching function $s(t)$ in the large-LO region is $2/\pi$ [25]. On the other hand, when the LO power is small, the CG can be calculated as

$$\text{CG} = \frac{1}{T}\int_0^T \left(\frac{V_{\text{LO}}\cos(\omega_{\text{LO}}t)}{2V_T}\right)\cdot\cos(\omega_{\text{LO}}t)\cdot dt = \frac{V_{\text{LO}}}{4V_T}. \tag{5}$$

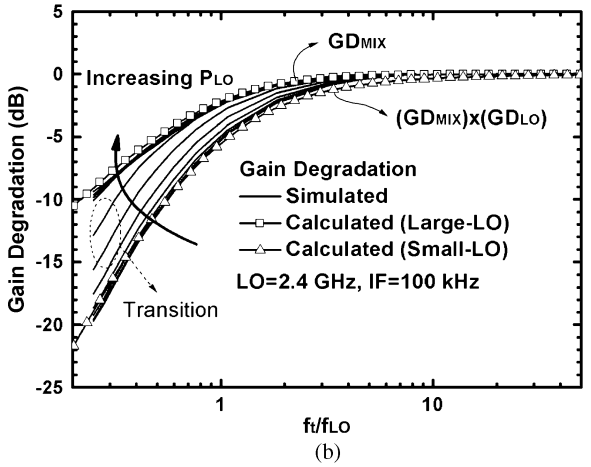
That is, the CG is proportional to the LO voltage swing (V_{LO}).

The simulated CG of a Gilbert mixer [see Fig. 5(a)] is shown in Fig. 6(a) with different f_T of the BJT switching core, while a two-stage PPF is applied as an LO generator. The f_T of the simulated BJT is changed by modifying the model parameter TF (forward base transit time). Fig. 6(a) clearly shows that the CG increases as the LO power increases when the LO power is small. Gradually, the CG reaches a wide flat-gain response (i.e., in the large-LO region). The wide LO power range with a flat-gain response covers typically more than 5 dB.

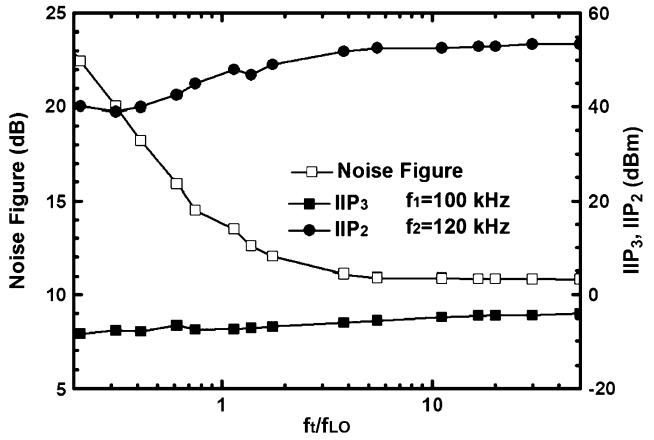
In the large-LO region, the switching function $s'(t)$ replaces $s(t)$, as indicated via a solid line in Fig. 5(b), when a finite f_T



(a)



(b)



(c)

Fig. 6. (a) CG with respect to LO power at different for different f_T. (b) CG degradation as a function of relative cutoff frequency ($f'_T = f_T/f_{\rm LO}$). (c) NF, $\rm IIP_3$, and $\rm IIP_2$ as a function of f'_T.

is considered and can be expressed as

$$s'(t) = \begin{cases} 1 - e^{-\omega_T(t-nT+T/4)}, \\ \quad nT - T/4 < t < nT + T/4 \\ \left[1 - e^{-\omega_T(t-nT-T/4)}\right], \\ \quad nT + T/4 < t < nT + 3T/4. \end{cases} \tag{6}$$

That is, the whole current charges the capacitance (C_π) of Q_1/Q_4 in the positive LO period while $C_{\pi 2}$ and $C_{\pi 3}$ are charged in the negative LO period. Thus, after the detailed derivations summarized in Appendix A, the CG of $s'(t)$ is

$$\rm CG = \frac{2}{\pi}\left[1 - \frac{1}{2}\frac{1+e^{-\pi f'_T}}{1+(f'_T)^2}\right] \tag{7}$$

where $f'_T = f_T/f_{\rm LO}$ represents the relative cutoff frequency. It is evident that a lower f_T results in a lower CG, as shown in Fig. 6(a).

As a result, the gain degradation of the mixer ($\rm GD_{MIX}$) due to the finite transistor f_T can be represented as

$$\rm GD_{MIX} = \frac{CG}{CG_{max}} = 1 - \frac{1}{2}\frac{1+e^{-\pi f'_T}}{1+(f'_T)^2} \tag{8}$$

where $\rm CG_{max}$ is defined as the CG when f_T is infinite.

In fact, the low f_T of the switching transistors also results in an LO voltage loss because of the loading effect of the LO PPF [26]. The flat gain region corresponding to the fully switching function becomes smaller for a lower f_T, as shown in Fig. 6(a). Thus, the LO voltage loss is tolerable in the large-LO region.

On the other hand, the CG degrades much more seriously in the small-LO region than in the large-LO region, as shown in Fig. 6(a). Since the CG is proportional to $V_{\rm LO}$ when the Gilbert mixer operates in the small-LO region, the degradation of the LO voltage directly leads to CG degradation. As a result, the GD due to LO loss ($\rm GD_{LO}$) should be included and the overall GD can be approximated as

$$\rm GD_{total} = GD_{MIX} \times GD_{LO}. \tag{9}$$

$\rm GD_{LO}$ can be expressed as follows:

$$\rm GD_{LO} = \sqrt{\frac{2}{1+\left[1+2g_mR_n/f'_T\right]^2}} \tag{10}$$

where g_m is the transconductance of the switching device and R_n is the resistance at the $n_{\rm th}$ stage (last stage) of the PPF. The complete derivation is also summarized in Appendix A.

For a more clear observation of the GD, Fig. 6(b) shows the GD with respect to the relative cutoff frequency (f'_T) at different LO power levels and the data is directly taken from Fig. 6(a). The line with the square symbol represents the calculated GD in the large-LO region (i.e., $\rm GD_{MIX}$) while the GD with small LO input is indicated by triangular symbols (i.e., $\rm GD_{MIX} \times GD_{LO}$). Two lines successfully represent the upper and lower bounds of the GD at different LO power levels while the solid lines represent the simulated GD at different LO power and are thoroughly located within the two calculated boundaries.

It is noteworthy that this phenomenon is also suitable for an MOS switching core. However, a larger LO power is required to commute the tail current from one side to the other because a MOS differential pair requires a $\sqrt{2}V_{ov}$ LO voltage swing while only around $4V_T(\sim 0.1\ \rm V)$ is required for a BJT core. As a result, the fully switching region of the LO power range is relatively narrow and even disappears if a low-supply voltage is applied. For a clear comparison between MOS and BJT mixers, two MOS mixers are also simulated and indicated in Fig. 6(a) with the core device sizes (W/L) of 80 μm/0.18 μm and 80 μm/0.5 μm, respectively, while the RF g_m stage and

IF load stage are the same as those in the BJT mixer. As a result, the LO power requirement for the flat-gain response of both devices are around 2–5 dBm while the LO power requirement of the BJT mixer is below 0 dB even at the low-f_T operation. More importantly, the $1/f$ noise corner is 2 MHz/600 kHz for the MOS mixer with gate length of 0.18/0.5 μm, respectively, while the $1/f$ noise corner of the BJT mixer is much lower than 100 kHz.

Besides, the NF and linearity degradation are also simulated as shown in Fig. 6(c). Straightforwardly, the NF increases as the CG degrades. On the other hand, as the f_T' decreases, the IIP_2 performance is degraded due to the node capacitance at the switching core [27], while the IIP_3 performance has only a slight change.

C. PPF With Inductive Peaking Technique

Instead of a divide-by-2 divider and/or LO buffers with extra dc power consumption, the pure passive PPF can be directly used because the BJT mixer inherently has low LO power requirement even at a low-f_T operation when compared with MOS active/passive mixers. The multistage PPF is widely used in single-sideband upconverters, image-rejection downconverters, and I/Q downconverters [26], [28] since the quadrature phase error of the n-stage PPF can be expressed as $\phi = 2\tan^{-1}[(\omega-\omega_0)/(\omega+\omega_0)]^n$ where ω_0 is the designed center frequency. In other words, for a given tolerable phase error ϕ_0, the ratio bandwidth becomes $[(1+\varepsilon_n)/(1-\varepsilon_n)]^2$ where $\varepsilon_n = \tan^{1/n}(\phi_0/2)$. That is, more stages of the PPF result in less phase error within the target bandwidth or a wider tolerable bandwidth for a given phase error. In addition, the phase accuracy is independent of loading, but the loadings affect the overall voltage loss, as mentioned in [26]. The PPF has a certain voltage loss due to both the inter-stages and the last loading stage. The loss between every stage at the center frequency was fully discussed in [26] and can be directly calculated using the voltage division $R_n/(R_n+R_{n+1})$, while R_n is the n_{th}-stage resistance of the PPF. However, in this study, we especially emphasize the loss due to capacitive loading (i.e., the mixers) at the last stage because it is the sole term related to the mixer transistor f_T.

As proposed in [26], the voltage division (VD) at the output node can be expressed as

$$VD(\omega_0) = \frac{Z_L}{Z_L + R_n||(1/j\omega_0 C_n)} \tag{11}$$

where $\omega_0 = 1/(R_nC_n)$.

Conventionally, Z_L is typically a capacitive load (C_L) due to an active/passive mixer. Thus,

$$|VD(\omega_0)| = \frac{2}{\sqrt{1+(1+C_L/C_n)^2}}. \tag{12}$$

A large loading capacitance results in an incredible loss. In this study, parallel inductors are employed to optimize the LO voltage loss, as shown in Fig. 7(a). A simple model of a real inductor consists of a series resistor (R_S) and an inductor (L_S) with a quality factor (Q) defined as $\omega_0 L_S/R_S$. Generally, the

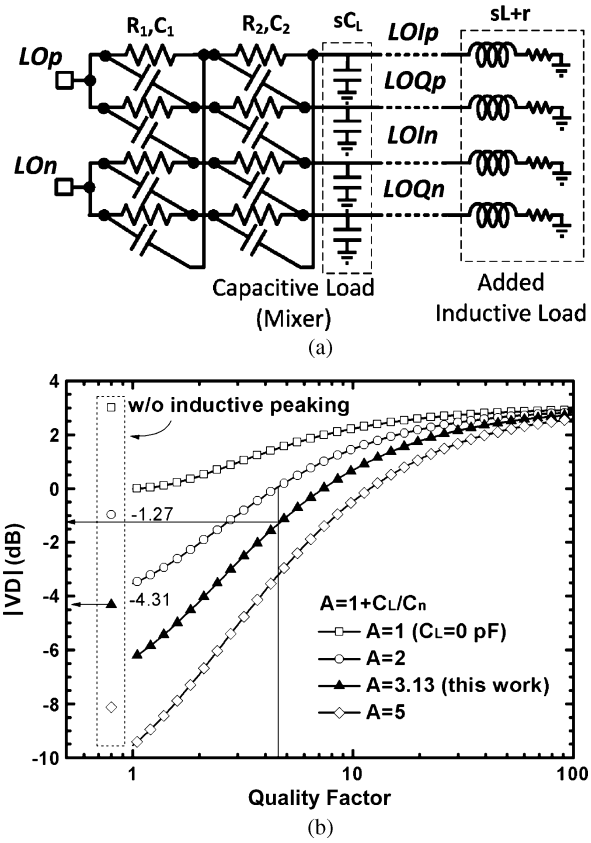


Fig. 7. (a) Schematic of the two-stage PPF with original capacitive load and additional inductive load. (b) Calculated optimal voltage division (VD) as a function of inductor quality factor (Q) for different capacitive loadings.

R_S is proportional to the geometric length, and thus also proportional to L_S. In fact, the parasitic capacitance C_{par} should be included for each inductor, which can be merged to C_L for simplicity.

After detailed derivations summarized in Appendix B, the maximum $|VD(\omega_0)|$ and its corresponding L_{opt} are

$$\begin{cases} |VD(\omega_0)|_{\mathrm{opt}} = \dfrac{\sqrt{2(1+Q^2)}}{A+Q} \\ L_{\mathrm{opt}} = \dfrac{1}{\omega_0^2 C_n(A-1/Q)} = \dfrac{1}{\omega_0^2\left[C_n(1-1/Q)+C_L\right]} \end{cases} \tag{13}$$

where $A = 1 + C_L/C_n$.

Fig. 7(b) shows the $|VD|$ as a function of Q with different $A(= 1 + C_L/C_n)$. The $|VD|$ without peaking inductors is also indicated in the same figure. It reveals that when the loading capacitance is small, an inductive peaking technique has no improvement. Further, when Q reaches infinity, $|VD|_{\mathrm{opt}} = +3$ dB, which is the same as the result in an open-load situation. However, in practice, $|VD|_{\mathrm{opt}}$ degrades due to a finite Q.

For the double-balanced structure of a Gilbert mixer, the peaking inductor parallel between the PPF and mixer core should be symmetric to maintain a fully differential performance. Besides, the differential inductor can provide size reduction and a better Q than separate inductors [29]. In this study, a 3-D symmetric inductor realization is employed for further area saving. Fig. 8(a) shows the multilayer structure

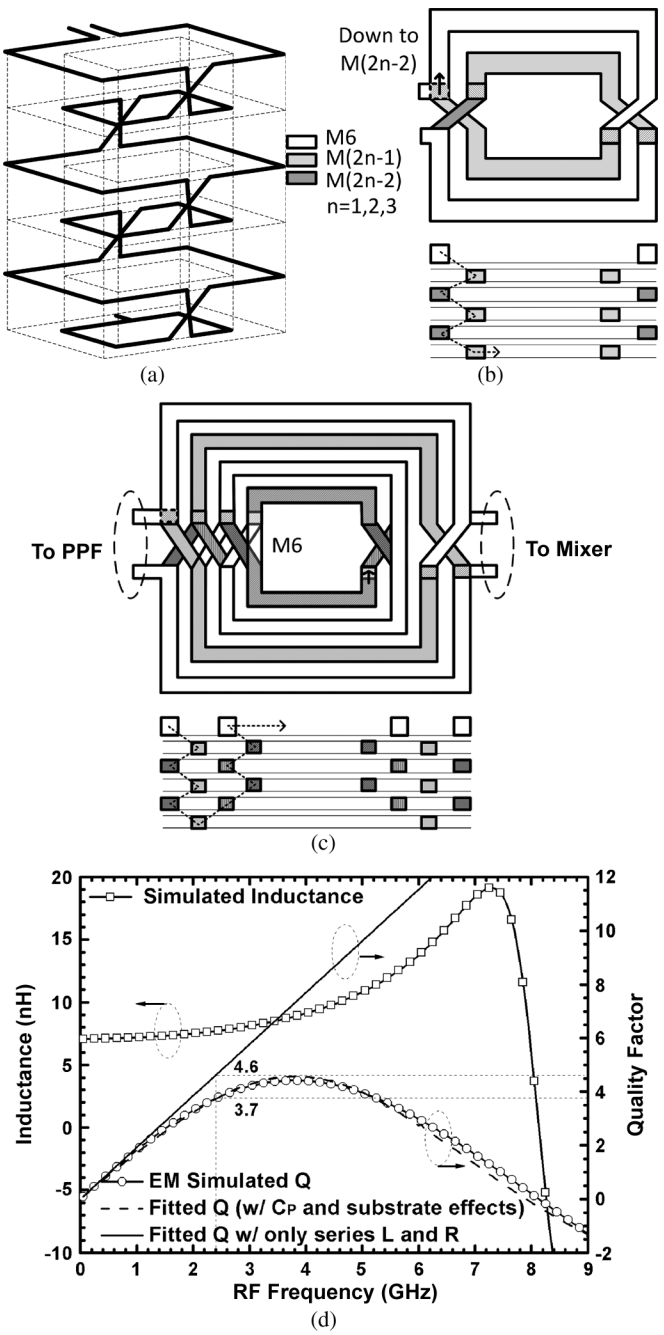


Fig. 8. (a) 3-D view and (b) top view of the pseudo-two-turn layout of the fully symmetric stacked inductor. (c) Top view and (d) simulated inductance and quality factor of the proposed pseudo-four-turn (equivalent 11 turns) fully symmetric stacked inductor.

of a pseudo-two-turn symmetric 3-D inductor proposed in [30]. The top view and cross-section view of this 3-D inductor are shown in Fig. 8(b). A pseudo-two-turn layout can provide, at most, six turns of an inductor in a 1P6M 0.18-μm CMOS process. However, the inductance is not enough. Using the basic idea of interleaving the inner and outer turns, this structure can be extended to a pseudo-four-turn formation, as illustrated in Fig. 8(c). As a result, a 3-D inductor with 11 turns is achieved with 8-μm linewidth, 2-μm line spacing, and an outer diameter of only 100 μm. The electromagnetic (EM)

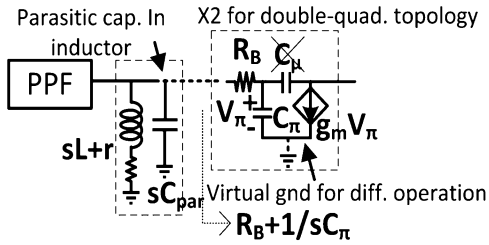


Fig. 9. Schematic PPF loadings including 3-D inductor and mixer with parasitic R_B.

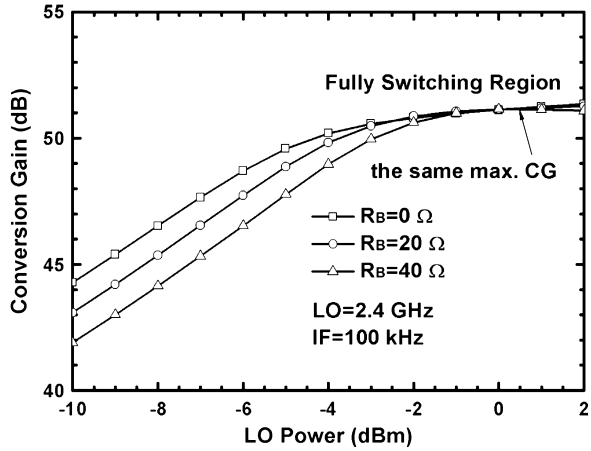


Fig. 10. Simulated CG as a function of LO power with different transistor R_B.

simulated differential inductance and quality factor are 7.2 nH and $Q_{\max} = 4.5$ with $f_{Q\max}/f_{\rm res}$ of 3.6/8.2 GHz, as shown in Fig. 8(d). Here, we emphasize that the Q of the inductor degrades by the parasitic capacitance, but this is not included in the Q used in (13). In fact, after extraction, the 3-D inductor has a differential inductance of 7.2 nH and a series resistance of 23.6 Ω. That is $Q = \omega_0 L/R = 4.6$, not 3.7, as indicated in Fig. 8(d). Moreover, additional parasitic capacitance should be added to C_L when calculating (13).

In this study, $C_n = 0.444\,\text{pF}\,(R_n = 150\,\Omega)$, $C_L = 0.945\,\text{pF}$, and $Q_{\rm ind} = 4.6$. As a result, the loss due to the pure capacitive load C_L (i.e., without inductive peaking) is around 4.31 dB. Around 3-dB improvement is obtained when using the inductive peaking technique, as shown in Fig. 7(b).

Further, all the above discussions are concerned about the pure capacitive mixer load. However, it is noteworthy that the series R_B of the V-NPN BJT is important for the LO power loss, especially for the parasitic devices, even though the current switching mechanism is dominated by the transistor f_T. As indicated in Fig. 9, R_B not only decreases the load impedance (at resonance) of the PPF (i.e., increases the PPF loss due to the loadings), but also reduces the voltage delivered to V_π by a factor of $1/(1+sR_BC_\pi)$. The simulated CG with respect to LO power for different R_B is shown in Fig. 10. Thus, a small R_B results in a lower LO power requirement, but the maximum CG are almost the same with different R_B. As discussed in Section II, $f_{\max}$ is a criterion for the parasitic resistance R_B; thus the device of $W_E \times L_E \times n = 0.5 \times 4 \times 2\ \mu\text{m}^2$ is chosen for its lowest required LO power to reach the peak CG of the Gilbert mixer.

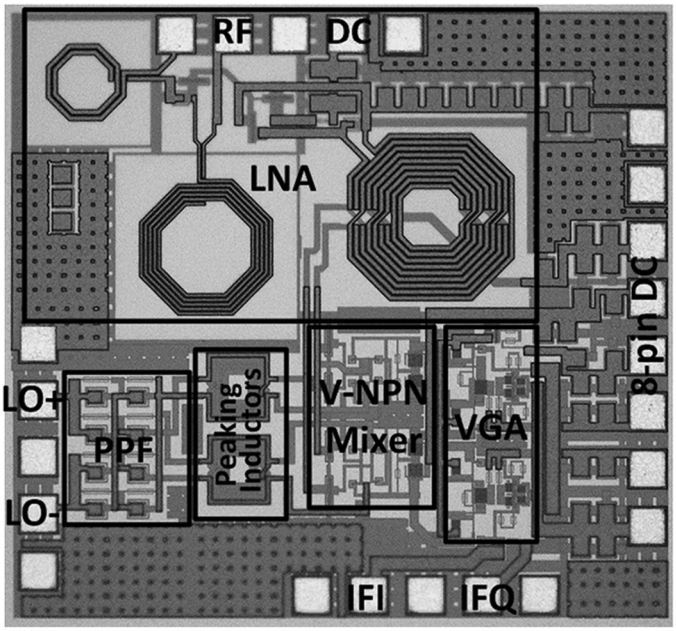


Fig. 11. Die photograph of a DCR using V-NPN BJT in a standard 0.18-μm CMOS process.

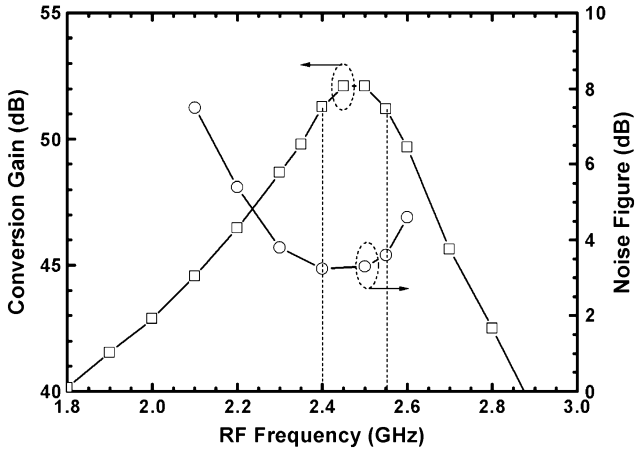


Fig. 12. CG and NF with respect to RF frequency of a DCR using V-NPN BJT in a standard 0.18-μm CMOS process.

IV. Measurement Results

The die photograph of the 2.4-GHz low-power low-noise DCR is shown in Fig. 11 and the die size is 1.15×1.05 mm^2. On-wafer measurement facilitates the RF performance. The current consumption of the LNA is 2.5 mA, while the I/Q mixers and VGAs consume 1.4 and 0.6 mA, respectively. Fig. 12 shows the CG and NF as a function of the RF frequency. The peak CG is 52 dB at 2.45 GHz with a 1-dB gain-flatness bandwidth ranging from 2.4 to 2.55 GHz. The minimum NF is 3.2 dB at 2.4 GHz and less than 4 dB within 2.3–2.6 GHz. Fig. 13 shows the CG with respect to the LO power at LO $=$ 2.4 GHz of three designs. The first design (the main design) uses two parallel inductors and the BJT size is $W_E \times L_E \times n = 0.5 \times 4 \times 2$ μm^2. Compared to the first design, the second and third designs have the BJT size of $W_E \times L_E \times n = 2 \times 2 \times 1$ μm^2 (with lower $f_{\max}$) and the former has parallel inductors, but the latter does not. As a result,

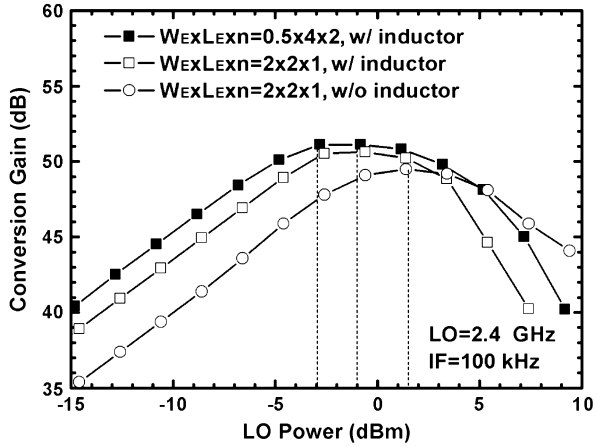


Fig. 13. CG as a function of LO power of a DCR using V-NPN BJT in a standard 0.18-μm CMOS process.

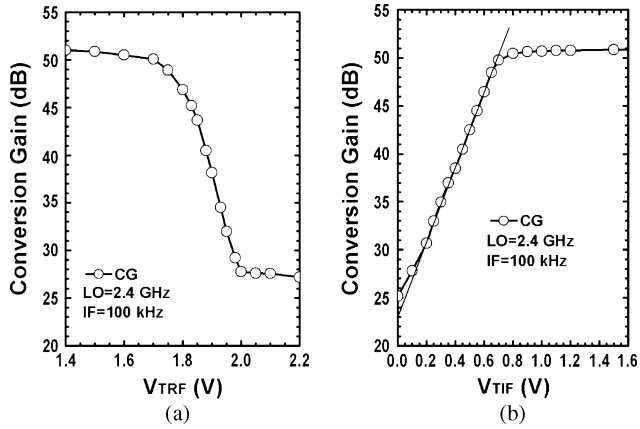


Fig. 14. CG with respect to: (a) RF tuning voltage and (b) IF tuning voltage of a DCR using V-NPN BJT in a standard 0.18-μm CMOS process.

only -3-dBm LO power is used to reach the maximum CG of 51 dB at 2.4 GHz for the main design. As shown in Fig. 13, using a higher $f_{\max}$ transistor results in around 2-dB less LO power requirement while the peak gain is similar, as predicted. On the other hand, the mixer without resonance inductors (the third design) requires around 2.5-dB larger LO power to reach the peak gain than that with inductors (i.e., the second design). As a result, using both a better device selection and an inductive peaking technique, the overall LO power is reduced by around 4.5 dB. Note that when the LO voltage swing increases, the dc voltage of the push–push point in the BJT switching core also increases. Thus, the BJT devices are gradually forced to operate in a saturation region and then the CG degrades. Due to the $1/f$ noise corner requirement, 2-μm gate length of the pMOS loads is chosen. Thus, the resulting high pMOS drain–source voltage drop makes the flat-gain region of the mixer core narrower. Fig. 14(a) shows the CG as a function of the LNA RF tuning voltage (V_{TRF}), while Fig. 14(b) indicates the CG with respect to the VGA IF tuning voltage (V_{TIF}). An over 20-dB tuning range is achieved by both RF and IF tuning schemes. Fig. 15 shows the NF when LO $=$ 2.4 GHz at different LNA gain. The NF is around 3.2/6/10 dB when CG $=$ 51/46/41 dB, respectively, while the $1/f$ noise corner is around 70 kHz.

TABLE I
PERFORMANCE COMPARISONS

Reference	[5]	[6]	[7]	[8]	[9]	[23]	[31]	[32]	[33]	[13]	[34]	This Work
Mixer Topology (A: Active; P: Passive)	**P**	**P**	**P**	**P**	**P**	**A**	**A**	**A**	**A** w/ PMOS core	**A** w/ current bleeding	**A** w/ BJT core	**A** w/ BJT core
RF Frequency (GHz)	2	2	2.4	2	2	2.5	2.4	1.6	2.4	1.9	2	2.4
Single-Ended Input	Yes	No	Yes	Yes	No	No	No	Yes	Yes	No	Yes	Yes
Conversion Gain (dB)	30	29	30 (5kΩ)	92(max)	22.5-25	43	52	36	21	21-47	33	51 (1MΩ) (10@ low-gain mode)
Noise Figure (dB)	3.1[a]	3.9	7.3[a]	>3[a]	<9.5[b]	5	24.5[a]	4.8	6	5.6	4.3[a]	3.2
1/f noise corner (kHz)	40	70	70	N/R	50	N/R	N/R	~1000	300	350	10	70
LO Power (dBm)	N/R	N/R	0	N/R[c]	N/R	-10[c]	-10[c]	N/R	0[d]	0.5V swing[e]	-10	-3 (w/o PPF: -8 dBm)
IIP_3 (dBm)	-12	-1	-8 (50Ω)	-17	>7	-37	-21	-19	-18	-10	-14.5	-32 (1MΩ) (-14@ low-gain mode)
IIP_2 (dBm)	39	35	40 (50Ω)	32	>50	N/R	18	N/R	N/R	44.8	34	22(1MΩ) (30@ low-gain mode)
Supply Voltage (V)	1.5	1.8	1.8	1.8	1.8	1.2	1.2	1.2	1.8	1.8	1.8	1.8
Power Dissipation (mW)	12[f]	15	6.3	81	10[b]	1.4[g]	3.4[g]	5.4[g]	1.6	37.8[g]	22.5	8.1
Technology	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.13μm CMOS	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	0.35μm BiCMOS	0.18μm CMOS

[a]Off-chip input matching [b]No LNA [c]With LO buffer
[d]Differential LO; no LO quadrature generator [e]Integrated PLL/VCO/divider
[f]Excluding off-chip baseband circuits [g]Including the LO generator

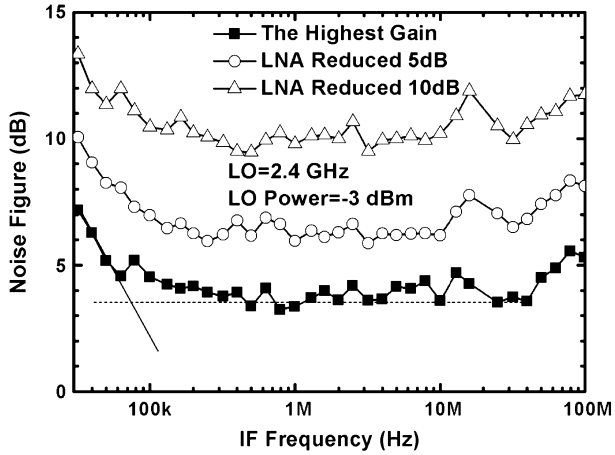


Fig. 15. NF with respect to IF frequency of a DCR using V-NPN BJT in a standard 0.18-μm CMOS process.

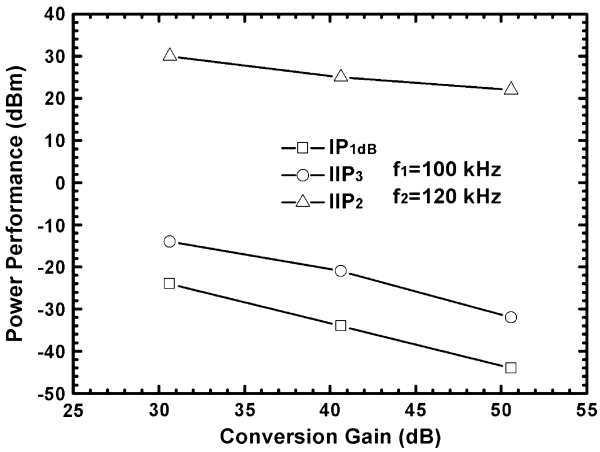


Fig. 16. Power performance, including $IP_{1\,dB}$, IIP_3, and IIP_2 of a DCR using V-NPN BJT in a standard 0.18-μm CMOS process.

Besides, the NF is kept below 4 dB when the IF VGA gain is reduced by over 20 dB while the LNA is on the maximum gain condition.

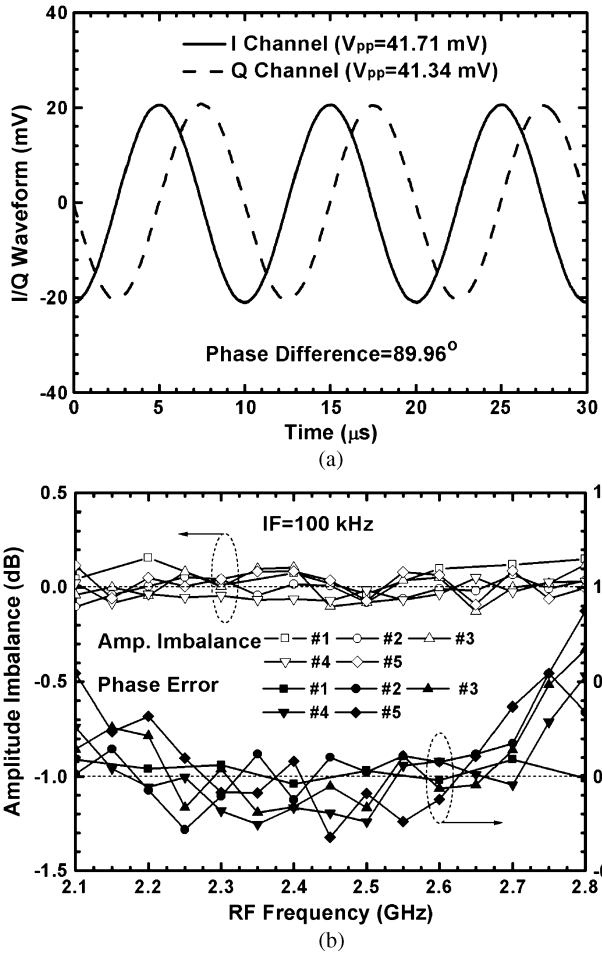


Fig. 17. (a) I/Q waveforms at $RF = 2.4$ GHz. (b) I/Q amplitude imbalance and phase error of a DCR using V-NPN BJT in a standard 0.18-μm CMOS process.

Fig. 16 shows the power performance, including $IP_{1\,dB}$, IIP_3, IIP_2, at different gain conditions. The I/Q output waveforms are shown in Fig. 17(a) with 0.077-dB gain difference and 0.04° phase error when $RF = 2.4001$ GHz and $LO = 2.4$ GHz. Since the *RC*

values of the PPF are random due to process variation, the amplitude/phase mismatch of five random-selected chips are measured to verify the balanced I/Q outputs, as shown in Fig. 17(b). Thus, the amplitude imbalance is below ± 0.15 dB and phase error is below $\pm 0.3^{\circ}$ covering 2.2–2.7 GHz. The input return loss is greater than 10 dB covering 2.2–2.6 GHz. The circuit performance is summarized and compared with state-of-the-art DCRs in Table I. The IIP_3 in this study at the high-gain mode ($\sim$50-dB gain) is relatively low; however, at similar gain condition ($\sim$30 dB) by tuning the VGA, the IIP_3 of this study is still compatible to that of other studie. The passive mixer realizations typically have worse noise performance, but the off-chip input matching inductors and off-chip baseband circuits results in a very low NF and also a very low $1/f$ noise corner [5], [8]. On the other hand, active mixer realizations [23], [31], [32] suffer from a serious $1/f$ noise problem (i.e., $1/f$ noise corner is typically higher than 1 MHz). However, both the pMOS mixer core [33] and the current bleeding technique [13] can reduce the $1/f$ noise corner. In [34], a low-noise high-gain receiver was proposed using BiCMOS technology to directly avoid the $1/f$ noise problem at a higher cost. As a result, the proposed receiver has excellent RF performance using low-cost 0.18-μm CMOS process.

V. Conclusion

Parasitic V-NPN BJTs in a standard CMOS process are used in the LO switching core of the Gilbert mixer because of their ultra-low $1/f$ noise corner. Both the current switching operation and PPF loss due to finite f_T of the following mixers are fully analyzed. Thus, an inductive peaking technique is proposed to enhance the overall performance. Further, a new fully symmetric 3-D layout realization is proposed in this paper for die size reduction. As a result, the demonstrated 2.4-GHz DCR has a CG of 51 dB and an NF of 3.2 dB with $1/f$ noise corner of around 70 kHz, while the current consumption is 4.5 mA at a 1.8-V supply.

Appendix A
Derivation of CG With Finite Cutoff Frequency and Gain Degradation Due to LO Loss

The Fourier series coefficient at ω of the switching function $s'(t)$ can be calculated by

$$\begin{aligned}\mathrm{CG} &= \frac{1}{T}\int_0^T s'(t)\cos\omega t dt \\ &= \frac{2}{T}\int_{-T/4}^{T/4}\left(1-e^{-\omega_T(t+T/4)}\right)\cos\omega t dt \\ &= \frac{2}{T}\int_0^{T/2}(1-e^{-\omega_T t})\sin\omega t dt \\ &= \frac{2}{\pi}\left[1-\frac{1}{2}\frac{1+e^{-\omega_T T/2}}{1+\left(\frac{\omega_T}{\omega_{\mathrm{LO}}}\right)^2}\right] \\ &= \frac{2}{\pi}\left[1-\frac{1}{2}\frac{1+e^{-\pi f_T'}}{1+(f_T')^2}\right] \end{aligned} \tag{A1}$$

where $T = 2\pi/\omega$ and $f_T' = f_T/f_{\mathrm{LO}}$.

As proposed in [24], the voltage division (VD) due to capacitive loading $(C_L \approx 2C_\pi)$ can be expressed as

$$VD_{\mathrm{LO}} = \frac{2}{\sqrt{1+(1+2C_\pi/C_n)^2}} \approx \frac{2}{\sqrt{1+[1+2g_mR_n/f_T']^2}} \tag{A2}$$

where $\omega_T \approx g_m/C_\pi$ and $\omega_{\mathrm{LO}} = 1/(R_nC_n)$.

As a result, the maximum VD_{LO} is $\sqrt{2}$ (i.e., +3-dB gain) when f_T reaches infinity. Thus, the gain degradation due to LO loss $(\mathrm{GD}_{\mathrm{LO}})$ is defined as

$$\mathrm{GD}_{\mathrm{LO}} = \frac{VD}{VD_{\max}} = \sqrt{\frac{2}{1+[1+2g_mR_n/(f_t/f_{\mathrm{LO}})]^2}}. \tag{A3}$$

Appendix B
Derivation of Optimal Inductance for an Inductive Peaking Between LO PPF and Mixer Core

The load impedance of series $L-R$ with parallel C_L can be expressed as

$$Z_L = \frac{1}{sC_L + \frac{1}{(s+\omega_0/Q)L}} = \frac{(j\omega+\omega_0/Q)L}{1-\omega^2C_LL + j\frac{\omega_0}{Q}\omega LC_L} \tag{B1}$$

where $R = \omega_0 L/Q$.

As a result, VD at the output node of the LO PPF is

$$\begin{aligned} VD(\omega_0) &\equiv \frac{Z_L}{Z_L+R_n\|(1/j\omega_0C_n)} \\ &= \frac{\omega_0L(1+j)(1+jQ)}{\omega_0L(1+j)(1+jQ)+R_n\left[Q+j\omega_0^2C_LL(1+jQ)\right]} \\ &= \frac{(1+j)(1+jQ)}{(1-AQ)+R_n\frac{Q}{\omega_0L}+j(A+Q)} \end{aligned} \tag{B2}$$

where $\omega_0 = 1/(R_nC_n)$ and $A = 1 + C_L/C_n$.

Taking the absolute value,

$$|VD(\omega_0)| = \frac{\sqrt{2(1+Q^2)}}{\sqrt{K-2\frac{M}{L}+\frac{N}{L^2}}} \tag{B3}$$

where

$$\begin{cases} M = \dfrac{QR_n}{\omega_0}[QA-1] \\ N = \dfrac{Q^2R^2}{\omega_0^2} \\ K = (1+A^2)(1+Q^2). \end{cases}$$

By setting the first-order differential equation to zero, $L_{\rm opt}$ is obtained as follows:

$$L_{\rm opt} = \frac{N}{M} = \frac{R_n}{\omega_0(A - 1/Q)} = \frac{1}{\omega_0^2 C_n(A - 1/Q)}. \quad \text{(B4)}$$

Substituting (B4) back into (B3),

$$|VD_O(\omega_0)|_{\rm opt} = \frac{\sqrt{2(1+Q^2)}}{\sqrt{(1+A^2)(1+Q^2) - (QA-1)^2}} = \frac{\sqrt{2(1+Q^2)}}{A+Q}. \quad \text{(B5)}$$

If L reaches infinity (i.e., without an inductor), VD becomes

$$|VD(\omega_0)| = \frac{2}{\sqrt{1+A^2}} = \frac{2}{\sqrt{1+(1+C_L/C_n)^2}} \quad \text{(B6)}$$

which is the same as the case of the pure capacitive loads proposed in [26].

REFERENCES

[1] D. A. Rich, M. S. Carroll, M. R. Frei, T. G. Ivanov, M. Mastrapasqua, S. Moinian, A. S. Chen, C. A. King, E. Harris, J. D. Blauwe, H.-H. Vuong, V. Archer, and K. Ng, "BiCMOS technology for mixed-digital, analog, and RF applications," *IEEE Microw. Mag.*, vol. 3, no. 2, pp. 44–55, Jun. 2002.

[2] L. E. Larson, "Integrated circuit technology options for RFICs—Present status and future directions," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 387–399, Mar. 1998.

[3] F. Beffa, T. Y. Sin, A. Tanzil, D. Ivory, B. Tenbroek, J. Strange, and W. Ali-Ahmad, "A receiver for WCDMA/EDGE mobile phones with inductorless front-end in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2011, pp. 370–371.

[4] C.-H. Wu, W.-C. Tsai, C.-G. Tan, C.-N. Chen, K.-I. Li, J.-L. Hsu, C.-L. Lo, H.-H. Chen, S.-Y. Su, K.-T. Chen, M. Chen, O. Shana'a, S.-H. Chou, and G. Chien, "A GPS/Galileo SoC with adaptive in-band blocker cancellation in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2011, pp. 462–463.

[5] Y. Feng, G. Takemura, S. Kawaguchi, and P. Kinget, "Design of a high performance 2-GHz direct-conversion front-end with a single-ended RF input in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1380–1390, May 2009.

[6] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, "A 15 mW, 70 kHz $1/f$ corner direct conversion CMOS receiver," in *Proc. CICC*, Sep. 2003, pp. 459–462.

[7] T.-K. Nguyen, V. Krizhanovskii, J. Lee, S.-K. Han, S.-G. Lee, N.-S. Kim, and C.-S. Pyo, "A low-power RF direct-conversion receiver/transmitter for 2.4-GHz-band IEEE 802.15.4 standard in 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4062–4071, Dec. 2006.

[8] H. Moon, J. Han, S.-I. Choi, D. Keum, and B.-H. Park, "An area-efficient 0.13-μm CMOS multiband WCDMA/HSDPA receiver," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 5, pp. 1447–1455, May 2010.

[9] N. Kim, V. Aparin, and L. E. Larson, "A resistively degenerated wideband passive mixer with low noise figure and high $\rm IIP_2$," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 4, pp. 820–830, Apr. 2010.

[10] H. Khatri, P. S. Gudem, and L. E. Larson, "Distortion in current commutating passive CMOS downconversion mixers," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 11, pp. 2671–2681, Nov. 2009.

[11] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, Jan. 2000.

[12] H. Darabi, "A noise cancellation technique in active RF-CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2628–2632, Dec. 2005.

[13] F. Gatta, D. Manstretta, P. Rossi, and F. Svelto, "A fully integrated 0.18-μm CMOS direct conversion receiver front-end with on-chip LO for UMTS," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 15–23, Jan. 2004.

[14] J. Park, C.-H. Lee, B.-S. Kim, and J. Laskar, "Design and analysis of low flicker-noise CMOS mixers for direct-conversion receivers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4372–4380, Dec. 2006.

[15] I. Nam, Y. J. Kim, and K. Lee, "Low $1/f$ noise and DC offset RF mixer for direct conversion receiver using parasitic vertical NPN bipolar transistor in deep N-well CMOS technology," in *VLSI Circuits Symp. Dig.*, Kyoto, Japan, Jun. 2003, pp. 223–226.

[16] I. Nam and K. Lee, "High-performance RF mixer and operational amplifier BiCMOS circuits using parasitic vertical bipolar transistor in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 392–405, Feb. 2005.

[17] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1985, pp. 162–165.

[18] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz, CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[19] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1433–1442, May 2004.

[20] K.-J. Sun, Z.-M. Tsai, K.-Y. Lin, and H. Wang, "A noise optimization formulation for CMOS low-noise amplifiers with on-chip low-Q inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 4, pp. 1554–1560, Apr. 2006.

[21] M. Zargari, M. Terrovitis, S. H.-M. Jen, B. J. Kaczynski, M. Lee, M. P. Mack, S. S. Mehta, S. Mendis, K. Onodera, H. Samavati, W. W. Si, K. Singh, A. Tabatabaei, D. Weber, D. K. Su, and B. A. Wooley, "A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g wireless LAN," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2239–2249, Dec. 2004.

[22] Y.-S. Youn, J.-H. Choi, M.-H. Cho, S.-H. Han, and M.-Y. Park, "A CMOS IF transceiver with 90 dB linear control VGA for IMT-2000 application," in *VLSI Circuits Symp. Tech. Dig.*, Jun. 2003, pp. 131–134.

[23] B. G. Perumana, R. Mukhopadhyay, S. Chakraborty, C.-H. Lee, and J. Laskar, "A low-power fully monolithic subthreshold CMOS receiver with integrated LO generation for 2.4 GHz wireless PAN applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2229–2238, Oct. 2008.

[24] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001, pp. 708–712.

[25] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998, pp. 188–189.

[26] J.-S. Syu, C. C. Meng, Y.-H. Teng, and H.-Y. Liao, "Large improvement in image rejection of double-quadrature dual-conversion low-IF architectures," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 7, pp. 1703–1712, Jul. 2010.

[27] M. Brandolini, P. Rossi, D. Sanzogni, and F. Svelto, "A +78 dBm $\rm IIP_2$ CMOS direct downconversion mixer for fully integrated UMTS receivers," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 552–559, Mar. 2006.

[28] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, Jun. 2001.

[29] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–382, Sep. 2000.

[30] W.-Z. Chen and W.-H. Chen, "Symmetric 3-D passive components for RF ICs application," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, pp. 599–602.

[31] J. A. M. Järvinen, J. Kaukovuori, J. Ryynänen, J. Jussila, K. Kivekäs, M. Honkanen, and K. A. I. Halonen, "2.4 GHz receiver for sensor applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1426–1433, Jul. 2005.

[32] A. Liscidini, A. Mazzanti, R. Tonietto, L. Vandi, P. Andreani, and R. Castello, "Single-stage low-power quadrature RF receiver front-end—The LMV cell," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2832–2841, Dec. 2006.

[33] V. H. Le, S.-K. Han, J.-S. Lee, and S.-G. Lee, "Current-reused ultra low power, low noise LNA+mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 11, pp. 755–757, Nov. 2009.

[34] J. Ryynanen, K. Kivekas, J. Jussila, A. Parssinen, and K. Halonen, "A dual-band RF front-end for WCDMA and GSM applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1198–1204, Aug. 2001.

Jin-Siang Syu (S'09) was born in Taoyuan, Taiwan, in 1984. He received the B.S. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2006, and is currently working toward the Ph.D. degree in electrical engineering at National Chiao Tung University.

His current research interests are in the areas of RF integrated circuits (RFICs).

Mr. Syu is a member of Phi Tau Phi.

Chinchun Meng (M'02) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1985, and the Ph.D. degree in electrical engineering from the University of California at Los Angeles (UCLA), in 1992.

He is currently a Full Professor with the Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan. His current research interests are in the areas of RF integrated circuits (RFICs) and microwave and millimeter-wave integrated circuits (ICs).

Chia-Ling Wang was born in Tainan, Taiwan, in 1986. She received the B.S. and M.S. degrees in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2008 and 2010, respectively. Her M.S. research concerned low-power low-noise receivers and low-cost V-band Schottky diodes in a standard CMOS process.