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Review Article

Wafer-level three-dimensional integrated circuits (3D IC): Schemes and key technologies

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Schemes and key technologies of wafer-level three-dimensional integrated circuits (3D IC) are reviewed and introduced in this paper. Direction of wafer stacking, methods of wafer bonding, fabrication of through-silicon via (TSV), and classification of wafer type are options for 3D IC schemes. Key technologies, such as alignment, Cu bonding, and TSV fabrication, are described as well. Better performance, lower cost, and more functionality of future electronic products become feasible with 3D IC concept application.

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1. Introduction

In recent decades, with the development of microelectronic technologies, high performance, small form factor and low cost of electronic products have become basic requirements for surviving in the market. Traditional integrated circuits are fabricated on one flat silicon wafer which the development is restricted by two-dimensional version. In order to follow Moore's law [1], chip makers are trying to integrate many transistors into the chip with better performance. However, when the gate length and oxide thickness of transistors both approach to the physical limit, the two-dimensional scaling will eventually face the end of the road.

Even though the dimensional scaling improves device performance in terms of gate switching speed, it has a reverse effect on global interconnect latency [2]. In addition, the global interconnect may dominate the operation frequency in some cases. Three-dimensional integration is one of the candidates to keep up with Moore's law and solve the issues above. The basic concept of three-dimensional integration is to integrate doubled or more transistors into the same "area". Besides, three-dimensional integration scheme can integrate different ICs from their own optimum processes together without using compromised fabrications which lower the efficiency and the yield [3–5].

From the packaging point of view, multi-chips package is the trend of semiconductor industries. Three-dimensional packaging offers a smaller area solution with lower power consumption. Although three-dimensional integration has many advantages, challenges such as reliability, heat dissipation, and testing methodology are current topics to be solved. This paper reviews and summaries wafer-level three-dimensional integrated circuits (3D IC). The content will focus on different 3D IC schemes and introduce key technologies. The information provides guidelines and references for researchers who are interested in this field.

2. Classification of wafer level 3D integration technology

The concept of 3D IC is based on the new position of ICs: Z direction. This means the position of ICs does not limit on X–Y plan anymore. Therefore we can stack the ICs to shorten the interconnection and also reduce the visible surface which increases the application range due to the small chip size and better efficiency.

3D integration includes three options: chip-to-chip, chip-to-wafer, and wafer-to-wafer. Wafer-level 3D integration is different from 3D package technology in terms of the stacking size. Generally speaking, 3D package technology focuses on final IC chip/die stacking. On the other hand, key technologies and schemes of wafer-level 3D integration are completed in wafer level, including bonding technology and through silicon via (TSV).

Because the fundamental concepts of wafer-level 3D integration technologies are the same as those of 3D packaging, this paper will only focus on wafer-level 3D integration. In general, wafer-level 3D integration can be classified into different categories based on the technologies applied.

2.1. Direction of wafer stacking

Based on the stacking direction of two device wafers, there are two different kinds of wafer stacking: face-to-face and face-to-

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back. The effects of wafer stacking direction are very enormous, including the circuit symmetry, fabrication difficulties, capacitance of interconnection and alignment consideration. Both of the stacking methods have been applied in 3D integration applications. Even mutual usage of each stacking method is also possible [6].

2.1.1. Face-to-face

For face-to-face version wafers, two wafers align and bond face to face together with the circuits, as shown in Fig. 1. From the fabrication technology point of view, this kind of integration is easy to be applied and does not need an additional handle wafer. However, the wafer to wafer symmetric issue needs to be taken into consideration. This means while designing the top wafers, since circuits on these wafers will be faced down during bonding, the action of mirroring circuits is required. At the same time, the symmetry and placement of alignment marks of both wafers should be considered as well.

2.1.2. Face-to-back

For face-to-back version wafers, the wafer upward (upper wafer or top wafer) should be thinned from the substrate with the top side attaching to an additional handle wafer. Comparing to the face-to-face version, this approach increases the complexity of process. However, the wafer to wafer symmetric issues can be eliminated. While the handle wafer is transparent and thinned wafer is thinned enough, the alignment process becomes transparent and much easier, as shown in Fig. 2.

2.2. Methods of wafer bonding

Bonding (stacking) technology is the key technology in 3D integration, both in wafer-level and chip-level. This process can make two or more layers stacking in Z-direction. Based on the bonding medium, the wafer bonding can be categorized into three options.

2.2.1. Metal-to-metal

Metal-to-metal bonding technique provides good adhesion and thermal conducting due to the characteristics of metal compounds. The use of metal diffusion bonding (thermo-compression bonding) in 3D applications allows the mechanical and electrical connections to be made between two wafers in one step process. For example, copper, tin and gold are usually the materials of metal bonding. The bonding parameters include 150–400 °C bonding temperature, high bond pressure up to 40 kN, high vacuum or nitrogen ambient [7–12]. Copper is one of the popular choices for 3D IC bonding since it is the interconnecting material of the standard CMOS process [7–10]. However, the bonding temperature for metal-to-metal bonding process needs to follow the thermal budget of existing devices and circuits.

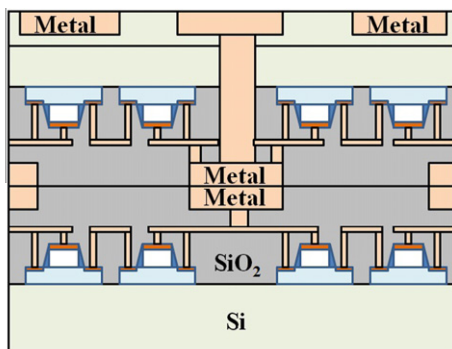

Fig. 1. Face-to-face wafer stacking.

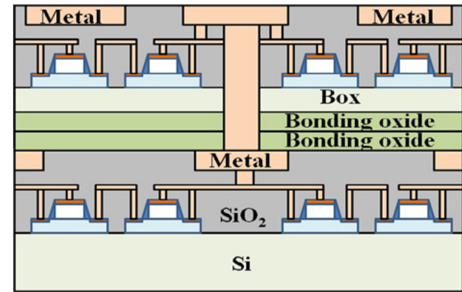

Fig. 2. Face-to-back wafer stacking.

2.2.2. Oxide-to-oxide

Since silicon oxide is the standard dielectric material of semiconductor processing, this material naturally becomes the candidate of bonding medium among two wafers [13–17]. The advantage of silicon oxide adhesion is CMOS process compatible and also gets high stacking density when top wafer is an SOI wafer. However, the oxide surfaces of both wafers should be extremely cleaned and flattened; usually an extra process is required. In bonding process, two-step technique is performed with room temperature contact followed by a high temperature anneal, up to 1000 °C, to let the bonding interface form strong covalent bonds (Si–O–Si) [17].

2.2.3. Polymer-to-polymer

Polymer-to-polymer bonding technique is similar to oxide-to-oxide bonding technique; both of the techniques can have high stacking density with the use of an SOI wafer. Furthermore, polymer-to-polymer bonding technique has better adhesive strength because the polymer material is more compliant than silicon oxide. [18–24]. This advantage is significant for wafer-level bonding. Nowadays SU-8 and BCB (benzocyclobu-tene) are the most common material used for wafer level adhesive bonding in 3D integration and applications [24]. However, the fusion point or glass transition temperature (Tg) of polymer is usually lower than 400 °C, which restricts the following process and even may pollute wafers or instruments due to the decomposition of polymer.

2.3. Fabrication of through-Si-via (TSV)

The order of TSV fabrication is much correlation with the wafer stacking, TSV filling materials, and device fabrications. Generally, the definition of TSV fabrication is based on the order with metal connection fabrication (so called BEOL process). The fabrications of TSV before and after BEOL fabrication are defined via-first and via-last, respectively.

2.3.1. Via-first

Via-first process means the TSVs are fabricated before BEOL process [25–27]. In this scheme, the materials to be filled in TSVs cannot be metals, such as Cu. In addition, because metal levels are not fabricated in this stage yet, the aspect ratio of via-first TSVs is smaller than those of via-last ones. Fig. 3 shows the process of via-first.

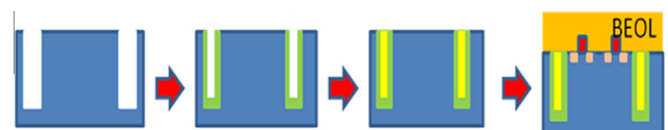

Fig. 3. Via-first process flow.

2.3.2. Via-last

When the through-silicon-vias are fabricated after the BEOL process [28,29], it is called via-last technique. The via-last technique, including drilling and filling processes, should be formed in the temperature lower than the thermal budget in order not to damage the existing devices and circuits. Fig. 4 shows the process of via-last.

2.4. Classification of wafer type

2.4.1. Bulk Si

The general wafer type, bulk Si is used most in the wafer level 3D IC integration. Not only the cost, but also the maturity of the process is the reason of population. Even when other species of wafers is used as a top wafer, the bottom wafer is usually still bulk Si wafer.

2.4.2. Silicon-on insulator (SOI)

SOI wafer, with a buried oxide layer, can be thinned uniformly because the buried oxide layer acts as an etch stop layer [6]. The etching process can be mechanical grinding, wet etching, dry etching or any combination. Most important, because the final thickness can be uniformly thin, using SOI can potentially achieve a high density 3D IC. The SOI structure also offers good latch-up immunity [30]. However, the ESD capability might be lowered in the stacked structure and the dense device layers have potential heat dissipation concern.

2.4.3. Glass

The role of a glass wafer in 3D integration is usually used to carry the top wafer. Therefore, the glass wafer for this purpose is called handle wafer. After the glass attaches the top wafer temporarily, the substrate of the top wafer can be thinned. Finally, the glass wafer will be removed after the thin top wafer bonds to the bottom wafer. Using glass wafers also offer good alignment results because of the transparent characteristic of glasses.

For all kinds of wafer stacking, we should notice that the wafer might be induced charge if any charged body touch or even close to the wafer. In the stacking step of two wafers, as long as one wafer is charged, the electrostatic discharge event might happen.

3. Key technology of wafer-level 3D IC integration

The wafer-level 3D IC integration is a novel concept to increase the circuit density and reduce the form factor with many enabling techniques. In this section, the most important three key technologies are introduced.

3.1. Alignment

The bad alignment leads to circuit malfunction or bad reliability. Therefore, the alignment tolerance dominates the contact area and the yield of 3D IC stacking. The accuracy of alignment correlates to the design of aligner and alignment marks. It is also decided by the experience of the operator. Fig. 5 shows an example of IR image showing typical misalignment results [31].

Fig. 4. Via-last process flow.

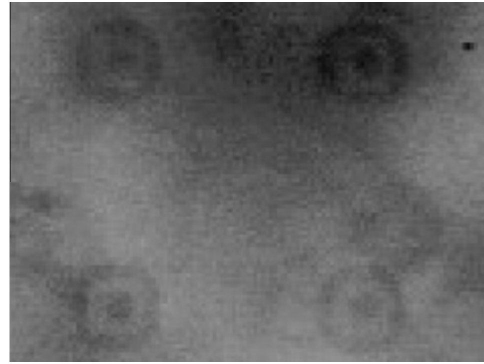

Fig. 5. An example of IR image showing typical misalignment results [23].

3.2. Copper wafer bonding

Copper is widely used as interconnects and metal wires in standard CMOS fabrication. Therefore, copper is the best candidate to connect two device layers or wafers of 3D IC. The principal of copper wafer bonding is to let two wafers contact then thermally compressed. During bonding, the copper layers of two wafers can diffuse each other to complete the bonding process. The cleanness of the wafer surface and the assembling time are correlated to the quality of the interconnection.

Generally speaking, a bonding temperature at least 300–400 °C is required to complete the copper bonding. The bonding quality can be identified by its morphology of the interface. To get good Cu bonding results, wafer bonding conditions are 400 °C for 30 min followed by 400 °C nitrogen annealing for 30 or 60 min [31]. Although high temperature and pressure may improve the bonding quality, the corresponding cost and possibility to affect the characteristics of devices are major concerns. Therefore, the low temperature and pressure bonding method is a major goal to be achieved for 3D integration [7,8]. Fig. 6 shows an SEM image of Cu interconnect bonding to Cu pad [31].

3.3. TSV process

The whole TSV fabrication process includes two parts: the first part is the etching of via, and the second part is filling of via. The difficulty of etching TSV depends on thickness of the thinned wafer. When the target etching depth is too deep, the opening size of via needs to be enlarged accordingly, which leads to the increase of chip size consumption. Fig. 7 shows an image of high aspect ratio TSVs [32–37].

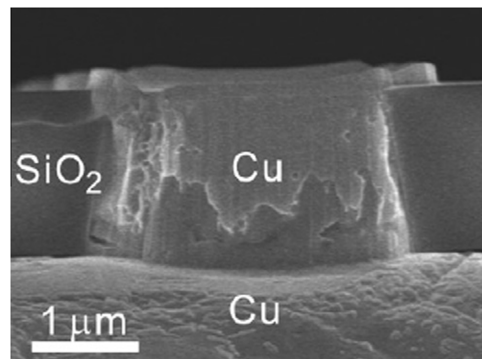

Fig. 6. An SEM image of Cu interconnect bonding to Cu pad [31].

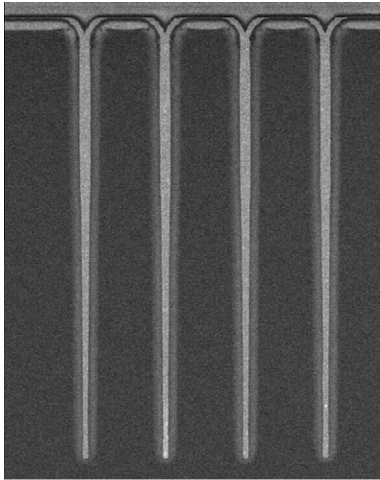

Fig. 7. An image of high aspect ratio TSVs [33].

The filling material is also another concern. Copper, tungsten, and polysilicon are typical options of TSV filling materials. Among these materials, copper and tungsten can be used only for via-last scheme, while polysilicon can be used both for via-first and via-last. Copper is the process compatible material with less residual stress and better electronic performance, but it is hard to fill into via holes with high aspect ratio. On the contrary, tungsten is easy to fill into via holes with high aspect ratio, but its high residual stress will be an issue. Polysilicon is the option for via-first TSVs but its resistance is higher than metals. With advantages and disadvantages of each material, the choice of filling TSV is significant in 3D integration, especially for wafer-level 3D IC.

4. Example of wafer-level 3D IC integration

The best way to understand the wafer-level 3D IC integration is to actually go through a real case of integration process. In this section, a 3D IC integration technology developed by MIT is introduced [38]. This novel process flow includes several key technologies and is very suitable to be an introductory study to understand wafer-level 3D IC integration technology.

The MIT three-dimensional integration is based on direct Cu–Cu wafer bonding at low temperature [38]. Device wafers, with Cu interconnects for electrical connectivity and Cu pads for structural support, are bonded each other in a face-to-back approach using Cu-to-Cu low temperature thermal compression.

The process flow for fabricating 3D IC is illustrated in Fig. 8. The significant steps shown in Fig. 8 are described as followed [38]:

(1) Fabrication of device layers on a SOI Si wafer.
(2) In order to stack the device layer on the top of another device layer, the substrate of SOI wafer has to be thinned by grinding and etching process. During the grinding process, for the mechanical support reason, a handle wafer is attached to the SOI wafer.
(3) The thin back process to remove the Si substrate of SOI wafer is a combination of mechanical grindback and chemical etching, which will stop on the buried oxide of SOI.
(4) Once the completion of the removal of SOI substrate, inter-vias are created by etching the oxide, SOI and ILD.
(5) The PECVD oxide sidewall passivation and via filling using damascene are performed.
(6) Cu interconnects are deposited on the top of vias for electrical connectivity. In this step, the device layer attached to the handle wafer is treated as the upper wafer for the next bonding process.

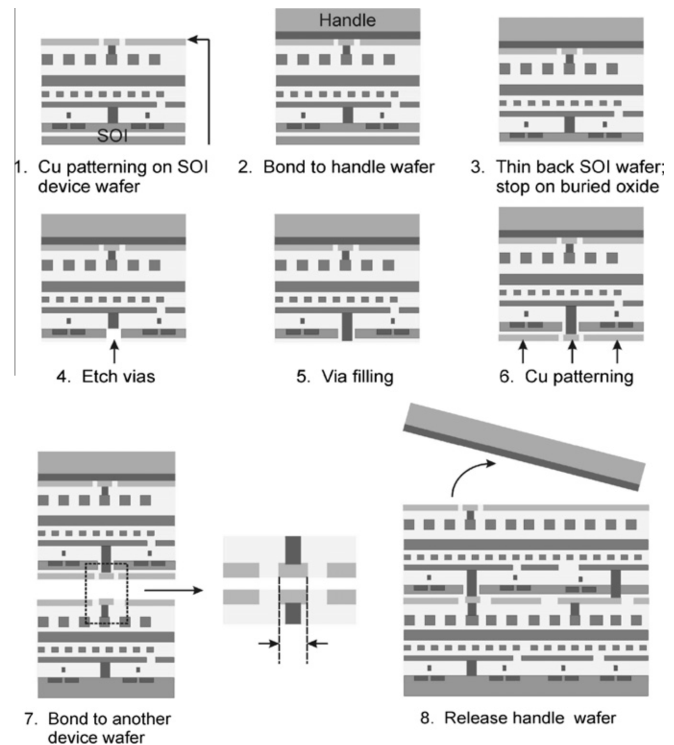

Fig. 8. MIT process flow for fabricating 3D IC [39].

(7) Fabrication of device layers, including the patterning of Cu interconnects and pads, on a bulk Si wafer. This bulk Si wafer with device layer is treat as the bottom wafer. Then the upper wafer and bottom wafer are aligned and bonded at the desired bonding condition.
(8) Handle wafer release is the final step of the 3D integration process. The handle wafer will be released from the bottom wafer. The device layer attached to the handle wafer will be remained bonding to the device layer of the bottom wafer.

5. Challenge of wafer level 3D ICs integration and outlook

Differs from conventional 2D package technology, wafer-level 3D integration gives more advantages, including: (a) higher interconnect density; (b) lower interconnect RC leads to lower power consumption and higher operation speed [39,40]; and (c) lower integration cost. However, challenges, such as reliability, alignment, new materials, 3D design CAD tool, and testing methodology, are still needed to be overcome.

6. Summary

As the approach of the physical limitation [41], industries can no more integrate many circuits into integrated circuits as easy as before. 3D IC technology offers a brand new version of concept to extend Moore's Law. In addition, 3D IC provides the solution to meet heterogeneous integration and small form factor requirements for today and future electronic products. With the efforts from academia and industries, wafer-level 3D IC integration with these advantages will eventually lead to mass production, high performance and low cost for the next generation ICs revolution.

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