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(54) **LIGHT EMISSION DIODE WITH FLIP-CHIP STRUCTURE AND MANUFACTURING METHOD THEREOF**

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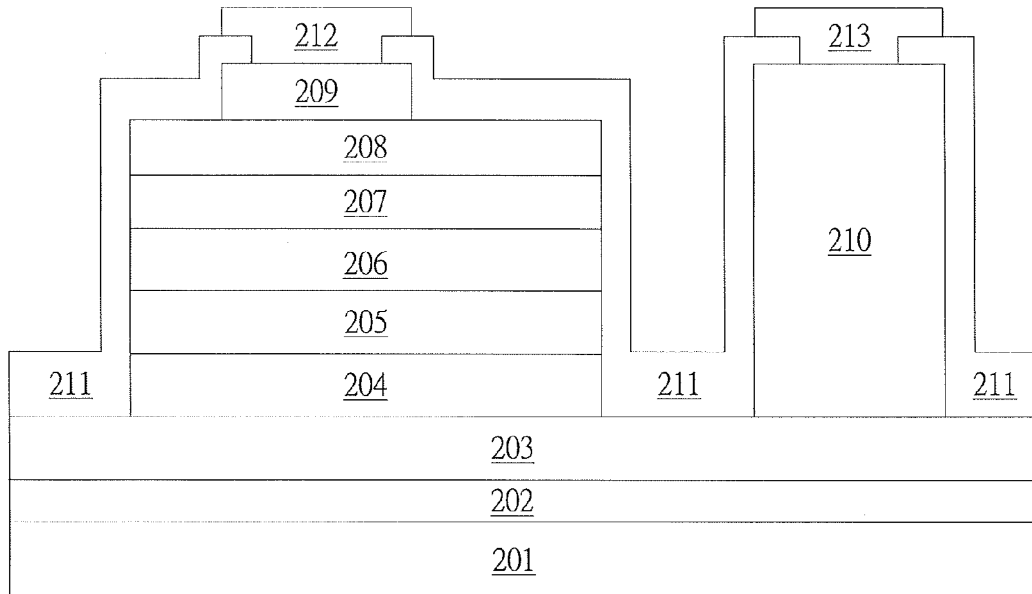
(57) **ABSTRACT**

A light emitting diode device with flip-chip structure includes a transparent protective substrate, a transparent conductor layer, a glue layer, a group III-V stack layer, a first conductivity metal electrode, a second conductivity metal electrode and an insulating layer. The transparent conductor layer is formed on the transparent protective substrate. The glue layer bonds the transparent protective substrate and the transparent conductor layer. The group III-V stack layer and the first conductivity metal electrode are respectively formed on a first portion and a second portion of the transparent conductor layer. The second conductivity metal electrode is formed on a portion of the group III-V stack layer. The insulating layer covers exposed portions of the transparent conductor layer and the group III-V stack layer, and the insulating layer further covers portions of the first and second conductivity metal electrodes, so as to expose the first and second conductivity metal electrodes.



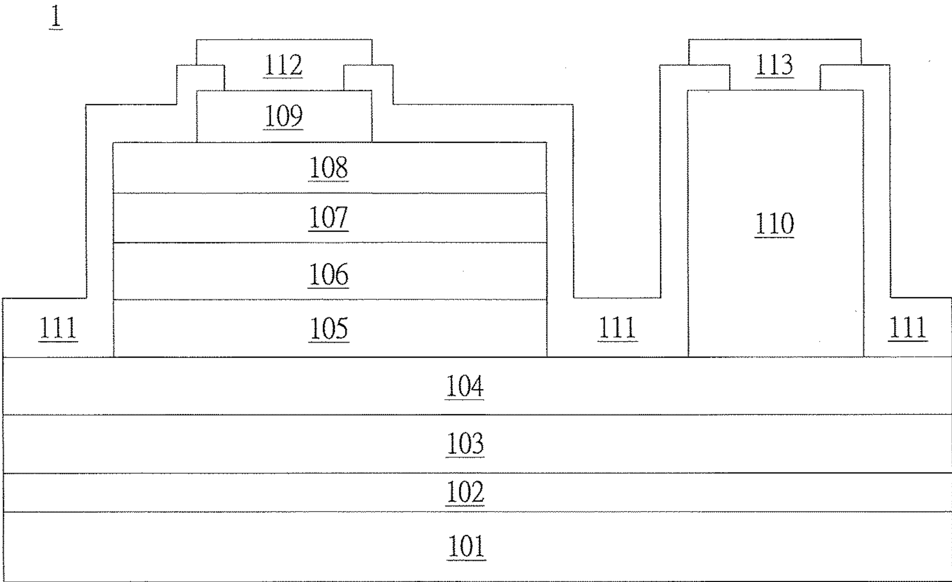


FIG. 1 (PRIOR ART)

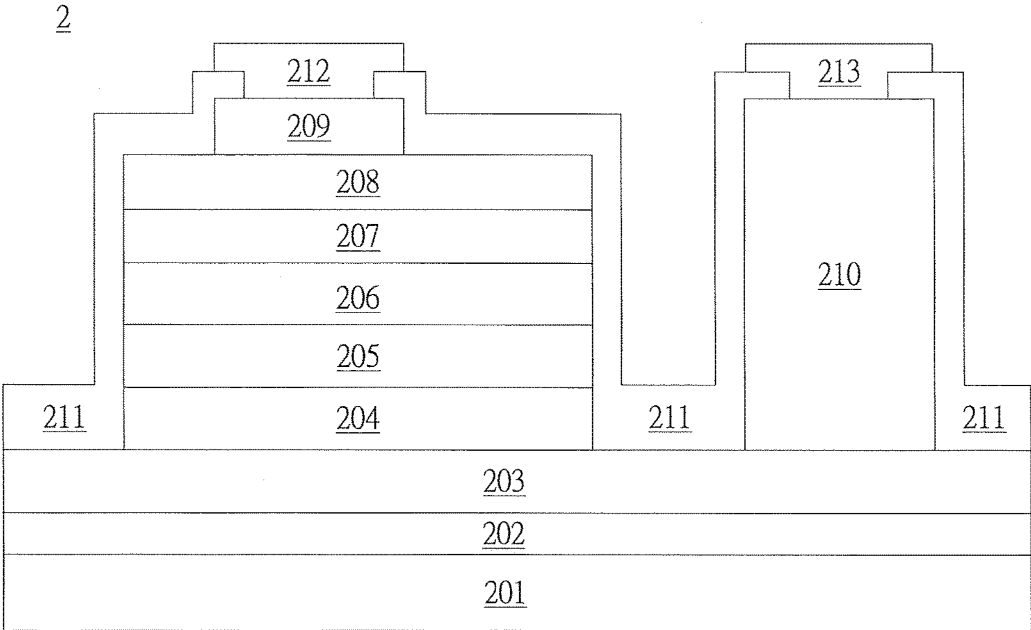


FIG. 2

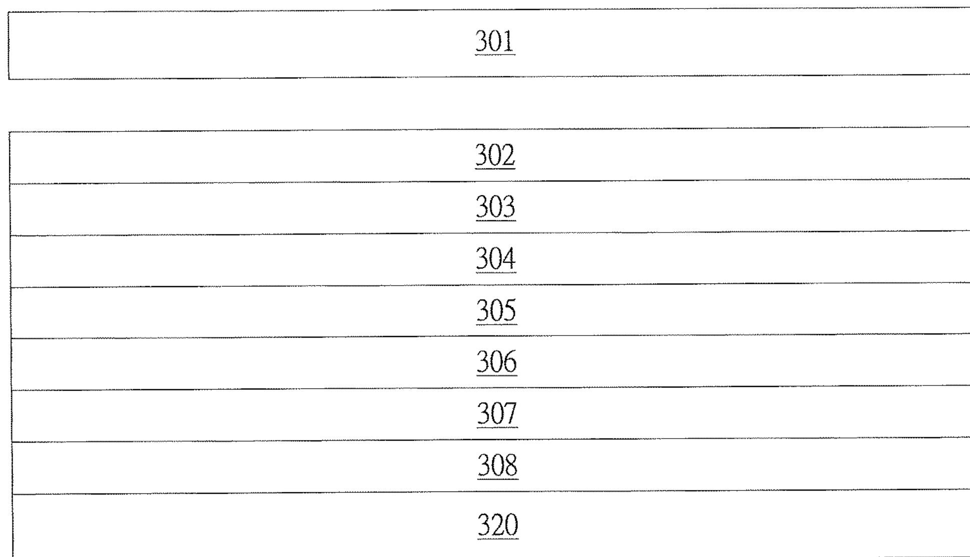


FIG. 3A

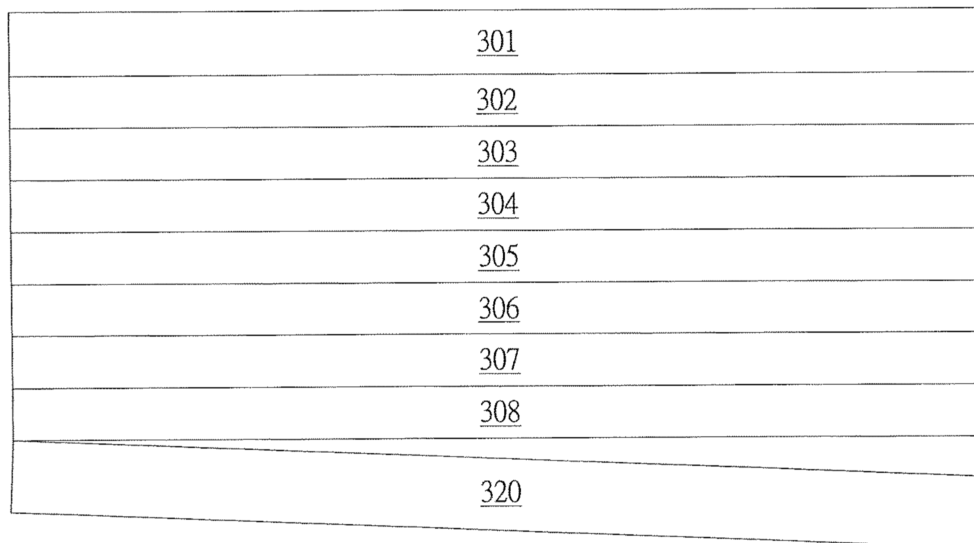


FIG. 3B

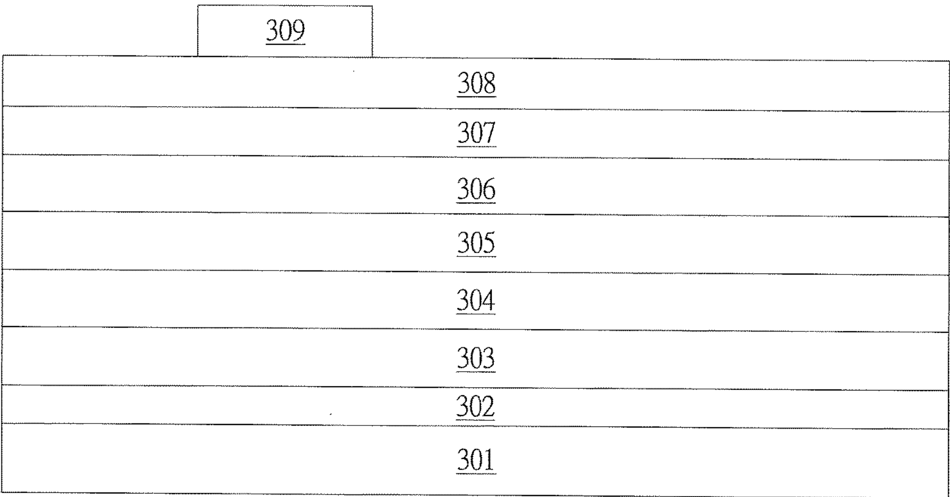


FIG. 3C

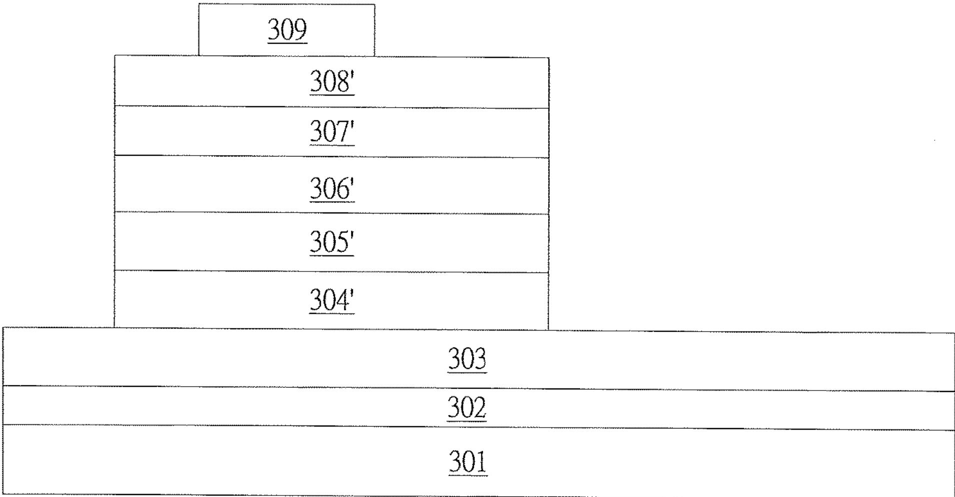


FIG. 3D

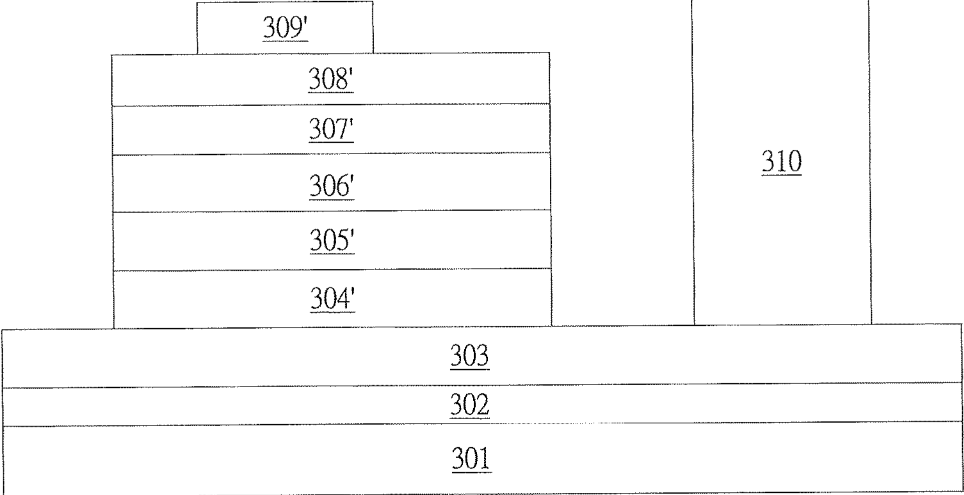


FIG. 3E

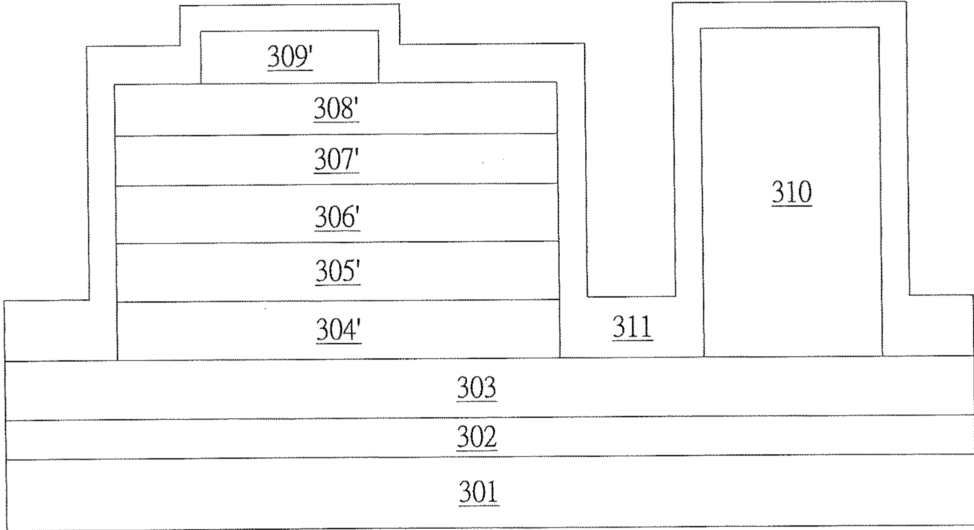


FIG. 3F

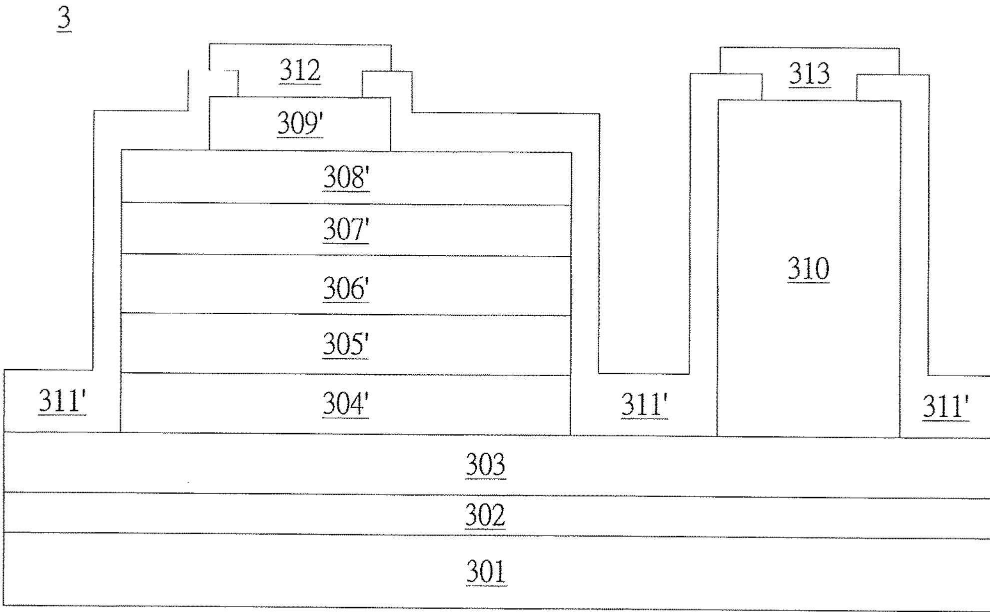


FIG. 3G

LIGHT EMISSION DIODE WITH FLIP-CHIP STRUCTURE AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from Taiwan Application No. 106126932, filed on Aug. 9, 2017, in the Taiwan Intellectual Property Office, the content of which is hereby incorporated by reference in their entirety for all purposes.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present disclosure relates to a structure of a lighting device, and in particular, to an LED device with flip-chip structure and manufacturing method thereof.

2. Description of the Related Art

[0003] Firstly, refer to FIG. **1**. FIG. **1** is a schematic diagram showing a sectional structure of a conventional LED device with flip-chip structure. The conventional flip-chip LED device **1** comprises a transparent protective substrate **101** (such as, a sapphire substrate), a glue layer **102** (such as, optical glue layer), a transparent conductor layer **103** (such as, an indium tin oxide layer), group III-V layer **104** (such as, a gallium phosphide layer or a gallium nitride layer), a first conductivity semiconductor layer **105** (such as, a P-type semiconductor layer), a quantum well and separation confining layer **106**, a second conductivity semiconductor layer **107** (such as, a N-type semiconductor layer), a group III-V contacting layer **108** (such as, a gallium arsenide contacting layer or a gallium nitride contacting layer), a second conductivity metal electrode **109** (such as, a N-type metal electrode), a first conductivity metal electrode **110** (such as, a P-type metal electrode), an insulating layer **111** (such as, a silicon dioxide layer), a first smooth electrode layer **113** and a second smooth electrode layer **112** (such as, titanium or gold layer).

[0004] The first conductivity semiconductor layer **105**, the quantum well and separation confining layer **106**, the second conductivity semiconductor layer **107**, the group III-V contacting layer **108** and the second conductivity metal electrode **109** are sequentially formed one portion of an upper surface of the group III-V layer **104**, and the first conductivity metal electrode **110** is formed on other one portion of the upper surface of the group III-V layer **104**, such that the first conductivity metal electrode **110** and each of the first conductivity semiconductor layer **105**, the quantum well and separation confining layer **106**, the second conductivity semiconductor layer **107**, the group III-V contacting layer **108** and the second conductivity metal electrode **109** has gap therebetween, and other portions of the upper surface of the group III-V layer **104** is exposed, wherein second conductivity metal electrode **109** is formed on merely one portion of an upper surface of the group III-V contacting layer **108**, and other portions of the upper surface of the group III-V contacting layer **108** is exposed.

[0005] The transparent conductor layer **103** is formed under a lower surface of the group III-V layer **104**, and the glue layer **102** contacts the lower surface group III-V layer **104** and an upper surface of the transparent protective substrate **101**, so as to glue the transparent protective substrate **101** with the transparent conductor layer **103**. The insulating layer **111** is formed on an exposed portion of the upper surface of the group III-V layer **104** and an exposed portion of the upper surface of the group III-V contacting layer **108**, the insulating layer **111** is further formed on a portion of an upper surface of the second conductivity metal electrode **109** and a portion of an upper surface of the first conductivity metal electrode **110**, and openings are formed on the upper surfaces of the second conductivity metal electrode **109** and the first conductivity metal electrode **110**. The second smooth electrode layer **112** and the first smooth electrode layer **113** are respectively formed on the openings on the upper surfaces of the second conductivity metal electrode **109** and the first conductivity metal electrode **110**, and further cover a portion of an upper surface of the insulating layer **111**.

[0006] During the manufacturing procedure of the conventional flip-chip LED device **1**, one etching process is performed to etch the first conductivity semiconductor layer **105**, the quantum well and separation confining layer **106**, the second conductivity semiconductor layer **107** and the group III-V contacting layer **108**, so as to expose the residual portions of the first conductivity semiconductor layer **105**, the quantum well and separation confining layer **106**, the second conductivity semiconductor layer **107** and the group III-V contacting layer **108**, wherein the above residual portions form the second conductivity plat illumination region. In short, the etching process merely etches to group III-V layer **104**.

[0007] The group III-V layer **104** functions as a cladding layer, and the cladding layer is coated with the first conductivity metal electrode **110**. During the manufacturing procedure of the conventional flip-chip LED device **1**, the first conductivity metal electrode **110** should be coated with the contacting metal and the thermal annealing process should be performed to form an Ohmic contact, and then the first conductivity metal electrode **110** is padded by and coated with the contacting metal. Since the first conductivity metal electrode **110** is formed on the cladding layer, the manufacturing procedure needs high temperature annealing, and it causes process uncertainty. In this case, the fabrication yield could be reduced.

[0008] In other one side, during the manufacturing procedure of the conventional flip-chip LED device **1**, a gluing process and a flipping process are required, but the high temperature annealing causes the damage for the glue of the glue layer **102**. Thus, merely the process of the non-substrate thin film flip-chip LED can be implemented, and it causes that the conventional flip-chip LED device **1** may be damaged easily during the manufacturing procedure.

SUMMARY OF THE INVENTION

[0009] Exemplary embodiments of the present disclosure provide a flip-chip LED device and manufacturing method thereof without high temperature annealing. A transparent conductor layer of the above flip-chip LED device is directly coated with a first conductivity metal electrode and the transparent conductor layer functions as a cladding layer which directly connects the first conductivity metal electrode. The flip-chip LED device does not need the usage of the Ohmic contacting electrode, and the high temperature

annealing process is not necessary, either, such that the manufacturing cost is decreased and the process yield is increased.

[0010] An exemplary embodiment of the present disclosure provides a flip-chip LED device a transparent protective substrate, a transparent conductor layer, a glue layer, a group III-V stack layer, a first conductivity metal electrode, a second conductivity metal electrode and an insulating layer. The transparent conductor layer is formed on the transparent protective substrate. The glue layer glues the transparent protective substrate and the transparent conductor layer. The group III-V stack layer and the first conductivity metal electrode are respectively formed on a first portion and a second portion of the transparent conductor layer. The second conductivity metal electrode is formed on a portion of the group III-V stack layer. The insulating layer covers exposed portions of the transparent conductor layer and the group III-V stack layer, and the insulating layer further covers portions of the first and second conductivity metal electrodes, so as to expose the first and second conductivity metal electrodes.

[0011] An exemplary embodiment of the present disclosure provides a manufacturing method of a flip-chip LED device comprises steps as follows. A group III-V substrate is provided, and a group III-V stack layer is formed on the group III-V substrate. A transparent conductor layer is formed on the group III-V stack layer. A glue layer is coated on the transparent conductor layer, and the transparent conductor layer is bonded with a transparent protective substrate. A separation process is performed, so as to remove the group III-V substrate from the group III-V stack layer. A stacking structure formed by the group III-V stack layer, the transparent conductor layer and the transparent protective substrate is flipped once. A second conductivity region is defined and a metal deposition is performed to define a second conductivity metal electrode on the second conductivity region, and then a reactive ion etching process is performed to etch the group III-V stack layer through the transparent conductor layer within a non-protective region. A first conductivity metal electrode region and a first conductivity metal electrode on the first conductivity metal electrode region are defined, and the first conductivity metal electrode region is coated with a first metal to form and pad the first conductivity metal electrode on the first conductivity metal electrode region. A second conductivity metal electrode region on the second conductivity region is defined, and the second conductivity metal electrode region is coated with a second metal. A physical deposition is used to coat the first conductivity metal electrode, the second conductivity metal electrode and the transparent conductor layer with an insulating layer, such that the insulating layer covers the first conductivity metal electrode, the second conductivity metal electrode and the transparent conductor layer. The first conductivity metal electrode and the second conductivity metal electrode are defined and an etching process is performed to expose the first conductivity metal electrode and the second conductivity metal electrode.

[0012] To sum up, in the flip-chip LED device and the manufacturing method thereof provided by exemplary embodiments of the present disclosure, the transparent conductor layer is directly coated with the first conductivity metal electrode, and the transparent conductor layer functions as the cladding layer which connects the first conductivity metal electrode. Thus, compared to the prior art, the present disclosure can have advantages as follows.

[0013] (1) The Ohmic contacting electrode is not required.

[0014] (2) The high temperature annealing is not required.

[0015] (3) The manufacturing cost is decreased.

[0016] (4) The process yielding rate is increased.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. **1** is a schematic diagram showing a sectional structure of a conventional flip-chip LED device.

[0018] FIG. **2** is a schematic diagram showing a sectional structure of a flip-chip LED device according to an exemplary embodiment of the present disclosure.

[0019] FIG. **3**A through FIG. **3**G are schematic diagrams depicting a manufacturing procedure of a flip-chip LED device according to an exemplary embodiment of the present disclosure.

DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0020] The present disclosure will be described in more detail below with reference to the accompanying drawings, in which exemplary embodiments of the present disclosure are shown. It will be understood by those skilled in the art that the described embodiments may be modified in various ways without departing from the spirit or scope of the present disclosure.

[0021] In order to clearly describe the present disclosure, portions not related to the present description are omitted, and like reference numerals refer to like elements throughout the specification. In addition, the dimensions and thicknesses of the individual structural members shown in the drawings are illustrative for convenience of illustration, and the present disclosure is not limited to the illustrated drawings.

[0022] Firstly, refer to FIG. **2**. FIG. **2** is a schematic diagram showing a sectional structure of a flip-chip LED device according to an exemplary embodiment of the present disclosure. The flip-chip LED device **2** can be micro OLED device for example, and the color of the illumination light is red. However, the type and illumination light color of the flip-chip LED device **2** are not used to limit the present disclosure.

[0023] The flip-chip LED device **2** comprises a transparent protective substrate **201**, a glue layer **202**, a transparent conductor layer **203**, a group III-V stack layer (**204** through **208**), a first conductivity metal electrode **210**, a second conductivity metal electrode **209**, an insulating layer **211**, a second smooth electrode layer **212** and a first smooth electrode layer **213**.

[0024] The glue layer **202** is used glue the transparent protective substrate **201** with the transparent conductor layer **203**, such that the transparent conductor layer **203** is formed on the transparent protective substrate **201**. In the exemplary embodiment of the present disclosure, the glue layer **202** can be a transparent optical glue layer, the transparent protective substrate **201** can be sapphire substrate or a glass substrate, the transparent conductor layer **203** can be a conductive metal oxide layer, such as an indium tin oxide layer, and the present disclosure does not limit the types of the transparent protective substrate **201**, the glue layer **202** and the transparent conductor layer **203**.

[0025] The group III-V stack layer (**204** through **208**) is formed on a first portion of the transparent conductor layer **203**, and the first conductivity metal electrode **210** is formed on a second portion of the transparent conductor layer **203**, and the second conductivity metal electrode **209** is formed on a portion of the group III-V stack layer (**204** through **208**), such that the first conductivity metal electrode **210** and the group III-V stack layer (**204** through **208**) has a gap therebetween.

[0026] In the exemplary embodiment of the present disclosure, the first conductivity metal electrode **210** and the second conductivity metal electrode **209** are respectively a P-type metal electrode and a N-type metal electrode, wherein the first conductivity metal electrode **210** is selected from a metal which is coated with "titanium and aluminum" or "chromium and gold", and the second conductivity metal electrode **209** is selected from at least one of gold and gold germanium alloy. However, the present disclosure does not limit the type and material of the first conductivity metal electrode **210** and the second conductivity metal electrode **209**.

[0027] The insulating layer **211** covers an exposed portion of the transparent conductor layer **203** (i.e. the portion outside the first and second portions of the transparent conductor layer **203**), an exposed portion of the group III-V stack layer (**204** through **208**) (i.e. the other portion of the group III-V stack layer not covered by the second conductivity metal electrode **209**), and the insulating layer **211** further covers a portion of the first conductivity metal electrode **210** and a portion of the second conductivity metal electrode **209**, so as to expose the first conductivity metal electrode **210** and the second conductivity metal electrode **209**. In the exemplary embodiment of the present disclosure, the insulating layer **211** can be a silicon dioxide layer, and the present disclosure does not limit the material of the insulating layer **211**.

[0028] The first smooth electrode layer **213** and the second smooth electrode layer **212** respectively covers an exposed portion of the first conductivity metal electrode **210** (i.e. the other portion of the first conductivity metal electrode **210** not covered by the insulating layer **211**) and an exposed portion of the second conductivity metal electrode **209** (i.e. the other portion of the second conductivity metal electrode **209** not covered by the insulating layer **211**), and further cover a portion of the insulating layer **211**. In the exemplary embodiment of the present disclosure, the first smooth electrode layer **213** and the second smooth electrode layer **212** can be selected from at least one of titanium and gold, and the material of the first smooth electrode layer **213** and the second smooth electrode layer **212** is not used to limit the present disclosure.

[0029] The group III-V stack layer (**204** through **208**) comprises a group III-V layer **204**, a first conductivity semiconductor layer **205**, a quantum well and separation confining layer **206**, a second conductivity semiconductor layer **207** and a group III-V contacting layer **208**. The group III-V layer **204** is formed on the first portion of the transparent conductor layer **203**. The first conductivity semiconductor layer **205** is formed on the group III-V layer **204**. The quantum well and separation confining layer **206** is formed on the first conductivity semiconductor layer **205**. The second conductivity semiconductor layer **207** is formed on the quantum well and separation confining layer **206**. The group III-V contacting layer **208** is formed on the second conductivity semiconductor layer **207**.

[0030] In the exemplary embodiment of the present disclosure, the group III-V layer **204** is a gallium phosphide (GaP) layer, a gallium nitride (GaN) layer or a gallium nitride aluminum indium layer. The first conductivity semiconductor layer **205** is a P-type semiconductor layer, the second conductivity semiconductor layer **207** a N-type semiconductor layer, and the group III-V contacting layer **208** functions as a group III-V semiconductor contacting layer for forming an Ohm contact, for example, a gallium arsenide (GaAs) contacting layer or a gallium nitride (GaN) contacting layer. However, the preset disclosure does not limit the types and materials of the group III-V layer **204**, the first conductivity semiconductor layer **205**, the second conductivity semiconductor layer **207** and the group III-V contacting layer **208**.

[0031] From the exemplary embodiment of FIG. **2**, it can be known that the transparent conductor layer **203** of the flip-chip LED device **2** functions as a cladding layer, such that the transparent conductor layer **203** is directly coated with the first conductivity metal electrode **210**. The flip-chip LED device **2** does not need the Ohm contacting electrode, and also does not needs the high temperature annealing, such that the manufacturing cost is decreased and the process yielding rate is increased.

[0032] Next, the manufacturing method of the flip-chip LED device in the present disclosure is illustrated. Refer FIG. **3**A through FIG. **3**G. FIG. **3**A through FIG. **3**G are schematic diagrams depicting a manufacturing procedure of a flip-chip LED device according to an exemplary embodiment of the present disclosure.

[0033] Firstly, in FIG. **3**A, the group III-V substrate **320** is provided, and a group III-V stack layer (**302** through **308**) is formed on the group III-V substrate **320**. Specifically, the manner for forming the group III-V stack layer (**302** through **308**) on the group III-V substrate **320** is to sequentially form the group III-V contacting layer **308**, the second conductivity semiconductor layer **307**, the quantum well and separation confining layer **306**, the second conductivity semiconductor layer **305** and the group III-V layer **304** on the group III-V substrate **320**. Next, the transparent conductor layer **303** is formed on the group III-V stack layer (**304** through **308**), for example the electron gun is used to coat the group III-V layer **304** with the transparent conductor layer **303**. Moreover, the transparent conductor layer **303** is directly formed on the group III-V layer **304**. Next, a glue layer **302** is smeared on the transparent conductor layer **303**, and the transparent conductor layer **303** is glued with the transparent protective substrate **301**.

[0034] In the exemplary embodiment of the present disclosure, the group III-V substrate **320** can be the gallium arsenide (GaAs) substrate, the transparent protective substrate **301** can be the sapphire substrate, the glue layer **302** can be the transparent optical glue layer, the transparent conductor layer **303** can be indium tin oxide layer, the group III-V layer **304** can be the gallium phosphide (GaP) layer, the first conductivity semiconductor layer **305** can be the P-type semiconductor layer, the second conductivity semiconductor layer **307** can be the N-type semiconductor layer, and the group III-V contacting layer **308** can be the gallium arsenide (GaAs) contacting layer. However, the present disclosure does not limit the types and materials of the group III-V substrate **320**, the transparent protective substrate **301**,

the glue layer **302**, the group III-V layer **304**, the first conductivity semiconductor layer **305**, the second conductivity semiconductor layer **307** and the group III-V contacting layer **308**.

[0035] Next, in FIG. **3**B, the separation process is performed by a wet etching process to remove group III-V stack layer (**304** through **308**) from the group III-V substrate **320**. For example, the prepared gallium arsenide etchant can etch to the gallium arsenide (GaAs) contacting layer, such that the gallium arsenide (GaAs) substrate can be removed. Next, the stack structure formed by the group III-V stack layer (**304** through **308**), the transparent conductor layer **303** and the transparent protective substrate **301** is flipped once.

[0036] Next, referring to FIG. **3**C, the photo resistor is used to define the second conductivity plat illumination region (the region of elements **304'** through **308'** in FIG. **3**D), and the metal deposition is performed to define the second conductivity metal electrode **309** on the second conductivity plat illumination region. Next, referring to FIG. **3**D, after the second conductivity plat illumination region is defined, the reactive ion etching process (for example, Inductively Coupled Plasma Reactive Ion Etching (ICP RIE) process) is performed, so as to etch the group III-V stack layer (**304** through **308**) to the transparent conductor layer **301** within the non-protective region (the region outside the elements **304'** through **308'**, and that is, the region outside the second conductivity plat illumination region). Next, the above used photo resistor is removed.

[0037] Next, referring to FIG. **3**E, the negative photo resistor is used to define the first conductivity metal electrode region (i.e. the region of the element **310**) and the first conductivity metal electrode **310** on the first conductivity metal electrode region, and the electron gun is used to coat the first conductivity metal electrode region with the first metal to form and pad the first conductivity metal electrode **310** of the first conductivity metal electrode region. Then, the negative photo resistor is used to define the second conductivity metal electrode region on the second conductivity plat illumination region. Next, the thermal evaporator is used to coat the second conductivity metal electrode region with the second metal, so as to from the second conductivity metal electrode **309'**. Then, the negative photo resistor is removed.

[0038] In the exemplary embodiment of the present disclosure, the first conductivity metal electrode **310** and the second conductivity metal electrode **309'** are respectively the P-type electrode and the N-type electrode, the second conductivity plat illumination region is the N-type plat illumination region, and the first conductivity metal electrode region and the second conductivity metal electrode region are respectively the P-type electrode region and the N-type electrode region. In addition, the first metal is the high conductance metal coated with the intermediate metal, wherein the intermediate metal can be titanium or chromium, and the high conductance metal can be aluminum or gold (i.e. the surface of the first metal can be coated with "titanium or chromium" and "aluminum or gold" sequentially). The second metal can be selected from at least one of gold and gold germanium alloy. However, the above limitations are used to implement an exemplary embodiment, and they are not limited in the present disclosure.

[0039] Next, referring to FIG. **3**F, the chemical vapor deposition (such as, PECVD) is used to coat first conductivity metal electrode **310**, the second conductivity metal electrode **309'** and the transparent conductor layer **303** with an insulating layer **311**, so as to finish the insulation process. In the exemplary embodiment of the present disclosure, the insulating layer **311** can be the silicon dioxide, and the present disclosure is not limited thereto.

[0040] Next, referring to FIG. **3**G, the negative photo resistor is used to define the first conductivity metal electrode **310** and the second conductivity metal electrode **309'**, and the etchant is used to etch the insulating layer **311** to locate the positions of the first conductivity metal electrode **310** and the second conductivity metal electrode **309'**, i.e. to expose the first conductivity metal electrode **310** and the second conductivity metal electrode **309'** (as shown in FIG. **3**G, the etched insulating layer **311'** has two openings corresponding to the first conductivity metal electrode **310** and the second conductivity metal electrode **309'**). Next, the negative photo resistor is removed, and the photo resistor is used to define the first conductivity metal electrode **310** and the second conductivity metal electrode **309'**. Then, the electron gun is used to coat the first conductivity metal electrode **310** and the second conductivity metal electrode **309'** with the third metal, and thus the first smooth electrode layer **312** and the second smooth electrode layer **313** are formed and the first conductivity metal electrode **310** and the second conductivity metal electrode **309'** are smoothed, so as to finish electrode smoothing process. Then, the photo resistor is removed. Next, the transparent protective substrate **301** is grinded and polished, and then the laser is used to perform the cutting process to form a plurality of chip dies of the flip-chip LED device **3**. In the exemplary embodiment of the present disclosure, the third metal is selected from at least one of titanium or gold, the transparent protective substrate **301** can be the sapphire substrate which is grinded and polished to have a thickness of 80 μm, and the present disclosure is not limited thereto.

[0041] From the exemplary embodiment of FIG. **3**A through FIG. **3**G, it can be known that during the manufacturing procedure of the flip-chip LED device **3**, the transparent conductor layer **303** functions as the cladding layer which is coated with the first conductivity metal electrode **310**. Thus, the flip-chip LED device **3** does not need the Ohm contacting electrode and high temperature annealing, resulting low manufacturing cost and high process yielding rate.

[0042] The above-mentioned descriptions represent merely the exemplary embodiment of the present disclosure, without any intention to limit the scope of the present disclosure thereto. Various equivalent changes, alternations or modifications based on the claims of present disclosure are all consequently viewed as being embraced by the scope of the present disclosure.

What is claimed is:

1. A flip-chip LED device, comprising:

a transparent protective substrate;

a transparent conductor layer, formed on the transparent protective substrate;

a glue layer, bonding the transparent protective substrate with the transparent conductor layer;

a group III-V stack layer, formed on a first portion of the transparent conductor layer;

a first conductivity metal electrode, formed on a second portion of the transparent conductor layer;

a second conductivity metal electrode, formed on a portion of the group III-V stack layer; and

an insulating layer, formed on an exposed portion of the transparent conductor layer and an exposed portion of the group III-V stack layer, and the insulating layer further covers a portion of the first conductivity metal electrode and a portion of the second conductivity metal electrode, so as to expose the first conductivity metal electrode and the second conductivity metal electrode.

2. The flip-chip LED device according to claim **1**, further comprising:

a first smooth electrode layer and a second smooth electrode layer, covering an exposed portion and the first conductivity metal electrode and an exposed portion of the second conductivity metal electrode, and further covering a portion of the insulating layer.

3. The flip-chip LED device according to claim **1**, wherein the group III-V stack layer comprises:

a group III-V layer, formed on the first portion of the transparent conductor layer;

a first conductivity semiconductor layer, formed on the group III-V layer;

a quantum well and separation confining layer, formed on the first conductivity semiconductor layer;

a second conductivity semiconductor layer, formed on the quantum well and separation confining layer; and

a group III-V contacting layer, formed on the second conductivity semiconductor layer.

4. The flip-chip LED device according to claim **3**, wherein the transparent conductor layer is a conductive metal oxide layer, the first conductivity metal electrode is a P-type metal electrode, and the second conductivity metal electrode is a N-type metal electrode.

5. The flip-chip LED device according to claim **4**, wherein the first conductivity semiconductor layer is a P-type semiconductor layer, and the second conductivity semiconductor layer is a N-type semiconductor layer, and the group III-V contacting layer functions as a group III-V semiconductor contacting layer for forming an Ohmic contact.

6. The flip-chip LED device according to claim **4**, wherein the first conductivity metal electrode is selected from aluminum or gold which is coated with titanium or chromium, the second conductivity metal electrode is selected from at least one of gold and gold germanium alloy, and each of the first smooth electrode layer and the second smooth electrode layer is selected from at least one of titanium and gold.

7. The flip-chip LED device according to claim **4**, wherein the insulating layer is a silicon dioxide layer and the transparent protective substrate is a glass substrate or a sapphire substrate.

8. The flip-chip LED device according to claim **2**, wherein the group III-V stack layer comprises:

a group III-V layer, formed on the first portion of the transparent conductor layer;

a first conductivity semiconductor layer, formed on the group III-V layer;

a quantum well and separation confining layer, formed on the first conductivity semiconductor layer;

a second conductivity semiconductor layer, formed on the quantum well and separation confining layer; and

a group III-V contacting layer, formed on the second conductivity semiconductor layer.

9. A manufacturing method of a flip-chip LED device, comprising:

providing a group III-V substrate, and forming a group III-V stack layer on the group III-V substrate;

forming a transparent conductor layer on the group III-V stack layer;

coating a glue layer on the transparent conductor layer, and bonding the transparent conductor layer with a transparent protective substrate;

performing a separation process, so as to remove the group III-V substrate from the group III-V stack layer;

flipping a stacking structure formed by the group III-V stack layer, the transparent conductor layer and the transparent protective substrate once;

defining a second conductivity plat illumination region and performing a metal deposition to define a second conductivity metal electrode on the second conductivity region, then performing a reactive ion etching process to etch the group **111**-V stack layer through the transparent conductor layer within a non-protective region;

defining a first conductivity metal electrode region and a first conductivity metal electrode on the first conductivity metal electrode region, and coating the first conductivity metal electrode region with a first metal to form and pad the first conductivity metal electrode on the first conductivity metal electrode region;

defining a second conductivity metal electrode region on the second conductivity region, and coating the second conductivity metal electrode region with a second metal;

using a physical deposition to coat the first conductivity metal electrode, the second conductivity metal electrode and the transparent conductor layer with an insulating layer, such that the insulating layer covers the first conductivity metal electrode, the second conductivity metal electrode and the transparent conductor layer; and

defining the first conductivity metal electrode and the second conductivity metal electrode and performing an etching process to expose the first conductivity metal electrode and the second conductivity metal electrode.

10. The manufacturing method of the flip-chip LED device according to claim **9**, further comprising:

defining the first conductivity metal electrode and the second conductivity metal electrode and coating the first conductivity metal electrode and the second conductivity metal electrode with a third metal to smooth the first conductivity metal electrode and the second conductivity metal electrode; and

grinding and polishing the transparent protective substrate, and performing a cutting process to form a plurality of chip dies.

11. The manufacturing method of the flip-chip LED device according to claim **9**, wherein a group III-V contacting layer, a second conductivity semiconductor layer, a quantum well and separation confining layer, a first conductivity semiconductor layer and a group III-V layer are sequentially formed on the group III-V substrate, so as to form the group III-V stack layer on the group III-V substrate.

12. The manufacturing method of the flip-chip LED device according to claim **11**, wherein first conductivity metal electrode and the second conductivity metal electrode are respectively a P-type metal electrode and a N-type metal electrode, the first conductivity semiconductor layer and the second conductivity semiconductor layer are respectively a

P-type semiconductor layer and a N-type semiconductor layer, the second conductivity plat illumination region is a N-type plat illumination region, and the first conductivity metal electrode region and the second conductivity metal electrode region are respectively a P-type electrode region and a N-type electrode region.

13. The manufacturing method of the flip-chip LED device according to claim **12**, the group III-V substrate is a gallium arsenide substrate, the group III-V contacting layer is a gallium arsenide contacting layer or a gallium nitride contacting layer, and the group III-V layer is a gallium phosphide layer, a gallium nitride layer or a gallium nitride aluminum indium layer.

14. The manufacturing method of the flip-chip LED device according to claim **12**, wherein the transparent protective substrate is a glass substrate or a sapphire substrate, the insulating layer is a silicon dioxide layer, and the transparent conductor layer is a conductive metal oxide layer.

15. The manufacturing method of the flip-chip LED device according to claim **14**, wherein the first metal is selected from a metal coated with "aluminum and titanium" or "gold and chromium", the second metal is selected from at least one of gold and gold germanium alloy, and the third metal layer is selected from at least one of titanium and gold.

16. The manufacturing method of the flip-chip LED device according to claim **10**, wherein the transparent protective substrate is grinded and polished to have a thickness of about 80 μm.

17. The manufacturing method of the flip-chip LED device according to claim **10**, wherein the cutting process is implemented by a laser.

18. The manufacturing method of the flip-chip LED device according to claim **10**, wherein a photo resistor is used to define the second conductivity region, and a negative photo resistor is used to define the first conductivity metal electrode region and the second conductivity metal electrode region on the second conductivity region.

19. The manufacturing method of the flip-chip LED device according to claim **10**, wherein an electron gun is used to coat the first conductivity metal electrode region with the first metal and to coat the first conductivity metal electrode and the second conductivity metal electrode with a third metal, and a thermal evaporator is used to coat the second conductivity metal electrode region with a second metal.

20. The manufacturing method of the flip-chip LED device according to claim **10**, wherein a group III-V contacting layer, a second conductivity semiconductor layer, a quantum well and separation confining layer, a first conductivity semiconductor layer and a group III-V layer are sequentially formed on the group III-V substrate, so as to form the group III-V stack layer on the group III-V substrate.

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