Investigation of Post-NBT Stress Current Instability Modes in HfSiON Gate Dielectric pMOSFETs by Measurement of Individual Trapped Charge Emissions

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Abstract

Bipolar charge detrapping induced current instability in HfSiON gate dielectric pMOSFETs after negative bias and temperature stress is studied by using a fast transient measurement technique. Both single electron and single hole emissions are observed, leading to post-stress current degradation and recovery, respectively. The NBT stress voltage and temperature effect on post-stress current evolution is explored. Clear evidence of electron and hole trapping in NBT stress is demonstrated. A bipolar charge trapping/detrapping model and charge detrapping paths based on measured charge emission times are proposed.

Introduction

Negative bias–temperature (NBT) instability has been recognized as a major reliability concern in ultra-thin gate dielectric pMOSFETs. Recent studies have shown electron trapping in NBTI in SiON and high-k gate dielectric pMOSFETs [1-4]. In this work, we are focused on post-stress current evolution in HfSiON gate dielectric pMOSFETs due to bipolar charge detrapping. Two post-stress current evolution modes, recovery mode and degradation mode, are observed, depending on a NBT stress condition. A physical model based on bipolar charge trapping/detrapping is proposed to explain the observed instability modes. A small area device is used to measure individual trapped electron and hole emissions directly. A fast transient measurement technique is employed to characterize charge emission times. The description of the measurement setup can be found in [5,6].

The devices used here are p-type MOSFETs with a poly-silicon electrode and a HfSiON-SiO_2 gate stack. The transistors have an effective oxide thickness (EOT) of 1.7nm, a gate length of 0.08~10μm, and a gate width of 0.16~100μm. NBT stress at V_g=-2.0V to -3.2V is performed. The linear drain current is measured at V_d=-0.2V and V_g=-0.7V to -1.2V. The voltage waveforms in NBT stress phase and in measurement (relaxation) phase are depicted in Fig. 1.

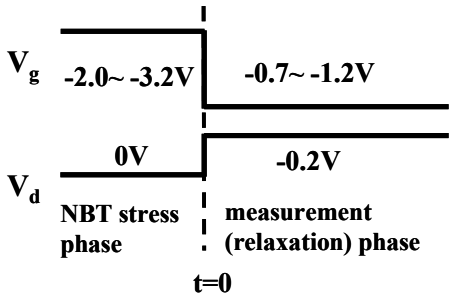


Fig. 1 Voltage waveforms applied to the gate and the drain during NBT stress and measurement (relaxation) phases. A high-speed electronic switch is used to minimize a delay between stress and measurement.

Results and Discussion

The drain current evolution after NBT stress at V_g =-3.0V is shown in Fig. 2. In a small area device (Fig. 2(a)), single-electron detrapping and single-hole detrapping are both observed, which are manifested by a step-like decrease and increase in the drain current. The pre-stress drain current is also plotted as a reference. In a large area device (Fig. 2(b)), the bipolar charge detrapping is exhibited by a turn-around characteristic of the post-stress current versus measurement time. Notably, trapped electron emission usually has shorter detrapping times and thus one may fail to observe it in a conventional NBT measurement setup using Agilent 4156 due to a switching delay. Our findings here are different from the result in a SiON pMOSFET in Ref.[3] that hole detrapping is faster than electron detrapping.

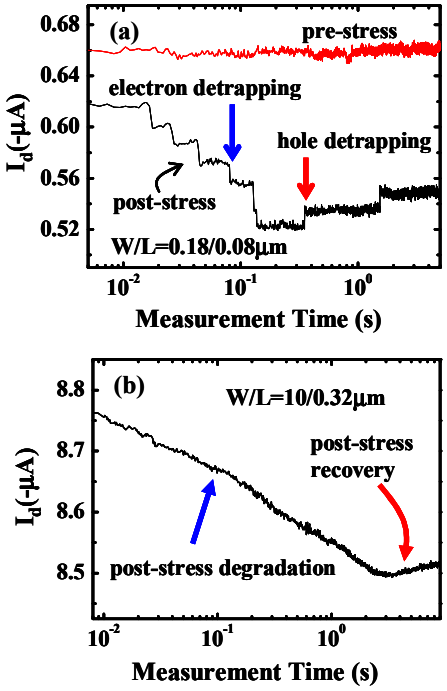


Fig. 2 Post-stress current evolution with measurement (relaxation) time in (a) a small area device (W/L=0.18/ 0.08μm) and (b) a large area device (W/L=10/0.32μm). The NBT stress voltage is -3.0V. The measurement voltages are V_g/V_d=-1.2V/-0.2V and temperature is 25°C. The pre-stress current is shown in (a) for comparison. Both current degradation and recovery are obtained in the measurement (relaxation) period.

(a) Stress V_g and temperature effect

Hole trapping is usually observed in NBT stress in pMOSFET's, but electron trapping is strongly affected by stress voltage and temperature. Fig. 3 shows the NBT

induced ΔI_d versus stress time at different stress V_g. The stress V_g ranges from –1.6V (result not shown here) to –2.8V. ΔI_d was taken immediately after stress. At a large stress V_g, ΔI_d initially increases with stress time and then decreases, featuring a turn-around characteristic in Fig. 3. The transition time for the ΔI_d changing from enhancement mode to degradation mode is mostly within seconds in the bias range of interest. This feature provides evidence of electron trapping in the stress. In contrast, at a smaller stress V_g (for example, -2V), ΔI_d decreases monotonically with stress time, indicating that holes are the dominant injected charges.

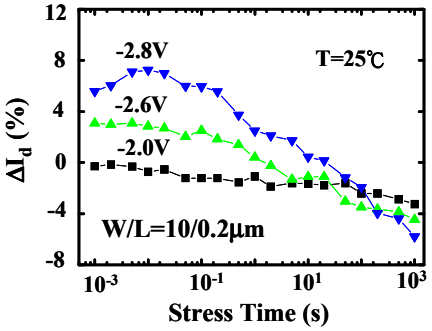


Fig. 3 Linear drain current change versus NBT stress time. ΔI_d is measured immediately after stress. Three stress voltages, V_g =-2.8V, -2.6V and -2.0V are applied. Electron trapping into pre-existing high-k traps is demonstrated by a positive ΔI_d at a high stress $|V_g|$.

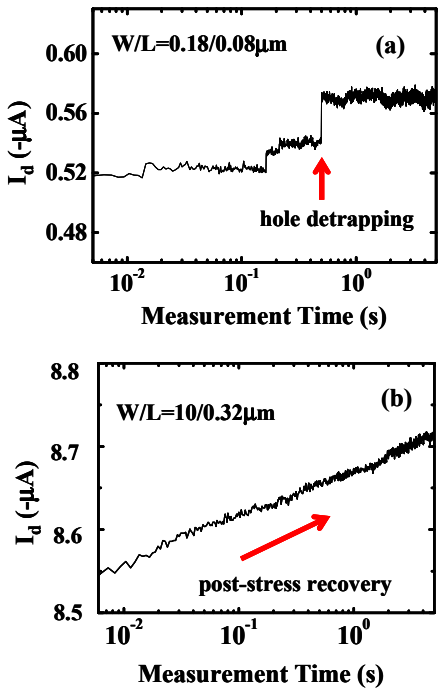


Fig. 4 Drain current evolution after a low V_g(=-2V) stress in (a) a small area device and (b) a large area device. Only hole detrapping are found at a low stress V_g. The measurement voltages are V_g/V_d=-1.2V/-0.2V and temperature is 25°C.

In Fig. 4, we monitor the current evolution after a low V_g (-2V) stress. Unlike Fig. 2 (a high V_g stress), the post-stress current exhibits a recovery mode and only hole detrapping is found. The stress V_g dependence can be explained by the fluence of injected carriers during stress.

Fig. 5 shows the band diagram and carrier flows in a high-k pMOSFET under -V_g stressing. We use a charge separation technique to measure the electron stress current (I_e) and the hole stress current (I_h) respectively (Fig. 6). The electron stress current increases drastically with $|V_g|$ and exceeds the hole stress current at a high stress $|V_g|$, thus explaining a large electron rate at a high stress $|V_g|$.

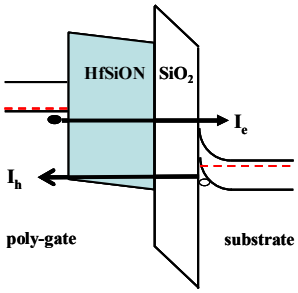


Fig. 5 Illustration of a band diagram and carrier flows in a high-k pMOSFET under -V_g stressing. In a charge separation measurement, the electron stress current (I_e) flows from the substrate to the gate and the hole stress current (I_h) flows from the source/drain to the gate.

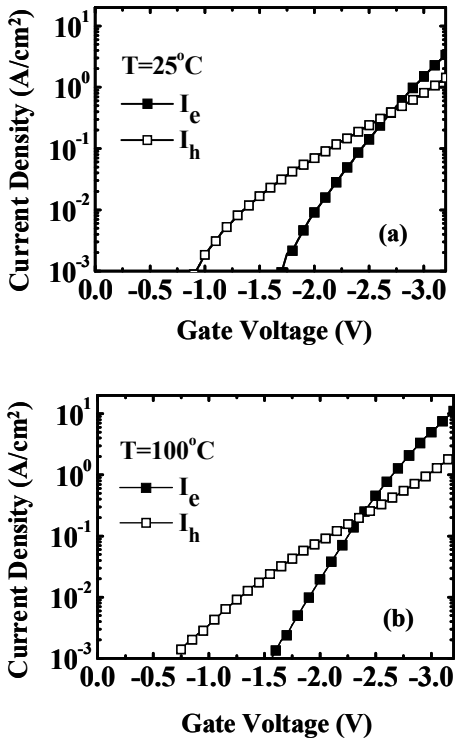


Fig. 6 Stress voltage dependence of electron injection current (I_e) and hole injection current (I_h). A charge separation technique is used to measure Ie and Ih. (a) T= 25°C and (b) T= 100°C.

In addition to a high stress voltage, a high stress temperature also favors electron trapping. Fig. 6(b) shows the electron and hole stress currents at an elevated temperature (T=100°C). Note that, as compared to the hole stress current, the electron stress current is enhanced to a larger extent at a higher temperature (Fig. 6). As a result, electron trapping is more sensitive to temperature than hole trapping. Fig. 7 shows the post-stress current evolution in a large area device for two different stress temperatures, T=25°C and 80°C. The stress V_g is -2.2V. The electron

detrapping phenomenon (turn-around behavior) is obtained only at a higher stress temperature.

(b) Measurement V_g dependence

The electron and hole detrapping paths can be inferred from the dependence of their emission times on measurement V_g. Two measurement V_g, -0.85V and -1V, are used in Fig. 8. A high stress V_g of -3.2V is chosen to ensure electron trapping and hole trapping during NBT stress.

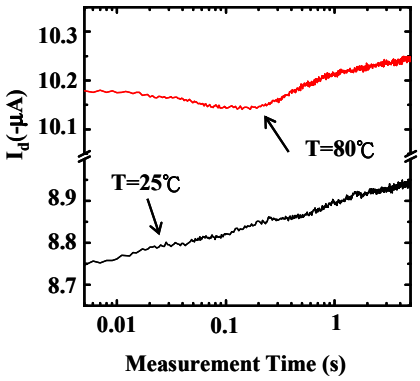


Fig. 7 Post-stress current evolutions with measurement time for two different stress temperatures, T= 25˚C and 80˚C. The stress voltage is -2.2V. The turn-around characteristic is observed only at T= 80˚C. Note that the Id measurement is biased in subthreshold region that Id is larger at a higher temperature.

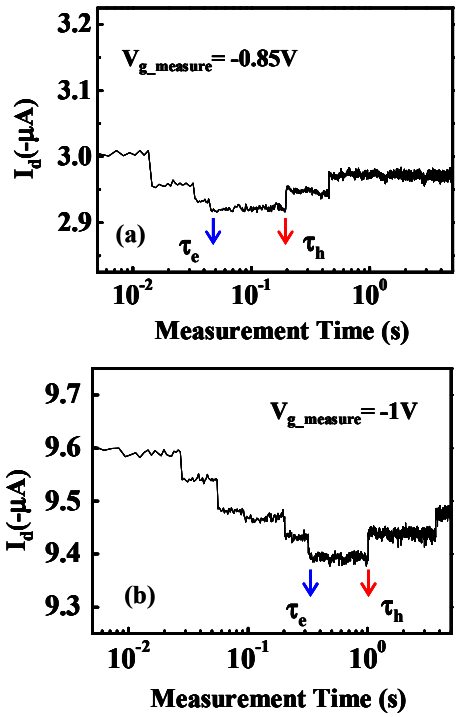
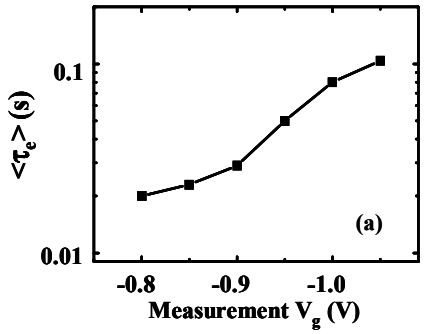


Fig. 8 Typical post-stress current evolution patterns. (a) measurement V_g=-0.85V and (b) V_g=-1.0V. The longest electron detrapping time (τ_e) and the shortest hole detrapping time (τ_h) are indicated. The trend is that both τ_e and τ_h increase with measurement $|V_g|$.

Typical post-stress current evolution patterns are shown in Fig. 8. In Fig. 9, we plot the electron and hole detrapping times ($<\tau_e>$ and $<\tau_h>$) versus measurement V_g. For simplicity, we only record the longest τ_e and the shortest τ_h. Ten measurements of the τ_e and the τ_h at each V_g in the same device were repeated by charge re-filling to take an average. The charge re-filling has the same voltage as NBT stress, but has a much shorter re-filling time (0.1sec). It is believed that no additional traps are created by the re-filling. Both electron and hole emission times increase with measurement $|V_g|$. Since a negative V_g exerts a repulsive force on a negative trapped charge, the positive dependence of the τ_e on $|V_g|$ implies trapped electron emission to the gate. Likewise, the positive dependence of the τ_h on $|V_g|$ suggests trapped hole emission to the substrate.



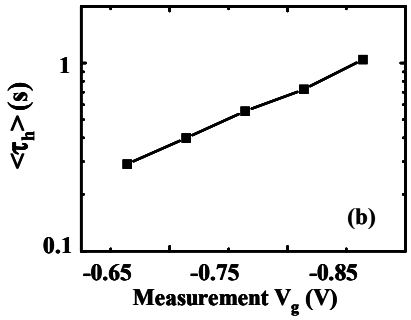


Fig.9 Average τ_e and τ_h are plotted against measurement V_g. We repeated measurement of each data point ten times by charge re-filling to take an average. Only the longest electron detrapping time and the shortest hole detrapping time (as shown in Fig. 8) are plotted in the figure.

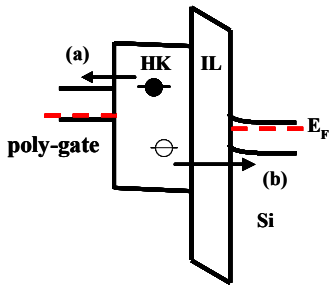


Fig. 10 Illustration of the energy band diagram in relaxation phase. (a) Trapped electron emission to the gate, and (b) trapped hole emission to the substrate.

(c) Charge detrapping model

The energy band diagram and charge detraping paths

in relaxation are drawn in Fig. 10. Thermally assisted tunneling for trapped charge emission is adopted [5]. The activation energy of trapped charges can be extracted from an Arrhenius plot of the τ_e and τ_h versus temperature (Fig. 11). The extracted activation energy is 0.20eV for trapped electrons and 0.14eV for trapped holes.

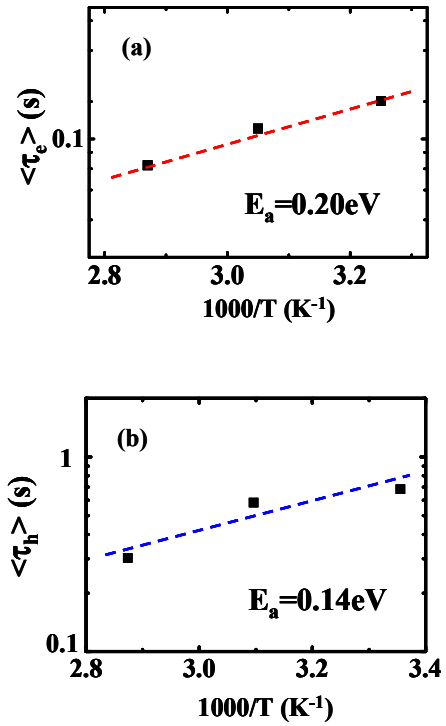


Fig. 11 Arrhenius plot of the τ_e and τ_h versus temperature, (a) trapped electrons and (b) trapped holes. The extracted activation energy is 0.2eV for electrons and 0.14eV for holes.

Conclusion

Post-NBT stress current instability due to electron detrapping and hole detrapping in a high-k gate dielectric pMOSFET has been explored. Post-stress current recovery and degradation modes are observed. Our study shows that electron trapping is more likely to occur as NBT stress voltage and temperature increase. The presence of electron trapping complicates the modeling and characterization of NBTI. In order to extrapolate a reliable NBTI lifetime, electron trapping effects should be carefully considered in voltage/temperature accelerated stress.

Acknowledgement

The authors would like to acknowledge financial support from National Science Council under contract # NSC95-2221-E009-271.

Reference

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