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Invited Paper

Low temperature bonding technology for 3D integration

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ABSTRACT

3D integration provides a promising solution to achieve system level integration with high function density, small form factor, enhanced transmission speed and low power consumption. Stacked bonding is the key technology to enable the communication between different strata of the 3D integration system. Low temperature bonding approaches are explored in industry to solve the performance degradation issue of the integrated devices. In this paper, various low temperature bonding technologies are reviewed and introduced, as well as the latest developments in world-wide companies and research institutes. The outlook for industrial application is also addressed in the paper.

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1. Introduction

Three-dimensional integrated circuits (3D IC) is emerging as a leading approach to combine mixed technologies to achieve high density integration with small form factor, high performance, low power consumption, and being a promising solution to overcome the limitations of Moore's law. To attain 3D integration structure, several key technologies have to be perfectly mastered, such as vertical interconnection by through silicon via (TSV), wafer thinning and handling, and wafer/chip stacked bonding (including chip-to-chip (C2C), chip-to-wafer (C2W) and wafer-to-wafer (W2W) bonding schemes). Among them, stacked bonding enables the communication between different strata of the 3D integration system. Conventional Cu–Cu thermo-compression is a popular bonding approach because it provides intrinsic interconnect and excellent bonding strength. However, high bonding pressure and temperature up to 350–400 °C are always required to perform the bonding integrity. These tough conditions may result in the bond-alignment deviation, high thermal stress, and possible damages to the bonded devices. It has been verified such high temperature could degrade the performance of DRAMs and other advanced devices [1].

Consequently, it is essential to explore alternative methods to alleviate bonding temperature and/or pressure to meet the requirement of low thermal budget and sensitive chips such as CIS, MEMS, LED and Bio application devices. In addition, low temperature bonding approaches are looked into the industry with great benefits to overcome issues related to (a) cracks of thinned and fragile wafer during bonding, (b) performance degradation under higher bonding temperature (>260 °C), (c) serious wafer/chip warpage and bonding misalignment, and (d) compatibility with the back-end-of-line process conditions and materials. In this paper, various low temperature bonding technologies, which could be performed under 250 °C, are reviewed in combination with the latest developments in corresponding companies or research institutes. Table 1 summarizes various low temperature bonding approaches, including innovative direct bonding, surface activated bonding (SAB), adhesive bonding, eutectic bonding, and emerging nanometal bonding technologies. Each technique will be introduced in detail, including its advantages and disadvantages, in the following sections.

2. Direct bonding

Wafer direct bonding uses the spontaneous adhesion of two wafers placed in direct contact under room temperature with short bonding time. It can offer high via density, good alignment, high bonding strength with stress free, and hermetic sealed bonding structures. In conventional direct bonding processes, the initial intimate contact bonds, mostly Si-to-Si and SiO_2-to-SiO_2, rely on the van der Waals attractive force between two extremely flat and clean surfaces. However, the subsequent high temperature annealing above 700–1000 °C is required to let the contact interface improve to strong covalent bonds (Si–O–Si) to ensure the bond strength and eliminate voids. In addition, the requirements of bonding environment and flat surface are very significant (root mean square (RMS) roughness lower than 0.5 nm) to perform the bonding integrity. These tough conditions are the drawbacks to limit its application. Therefore, surface treatments by wet chemical and/or dry plasma activation are developed to lower the annealing temperature to 200–400 °C or even unnecessary. These approaches can permit looser surface condition (RMS roughness up to 2 nm can still be bonded), and reduce the bonding environment limitation such as from ultrahigh vacuum to even the ambient air condition.

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Table 1
Comparison of various low temperature bonding technologies.

Bonding technology	Direct bonding	Surface activated bonding	Adhesive bonding	Eutectic bonding	Nanometal bonding
Major player	Ziptronix, LETI/STMicro	The university of Tokyo	WOW alliance	Infineon/IZM, IMEC, ITRI	RPI, IZM
Bonding material	Si–Si, SiO_2–SiO_2, Cu–Cu	Si–Si, Cu–Cu, Au–Au	Adhesive such as SU-8 and BCB	Eutectic alloy such as Au–In, Cu–Sn, In–Sn	Cu nanorod, Nanoporous Au bump
Bonding temperature	R.T.	R.T.	R.T.–350 °C	120–400 °C	150–400 °C
Specific requirement	Surface treatment, Post-bond annealing (200–400 °C)	Surface plasma activation, Ultrahigh vacuum	Usage of semiconductor compatible adhesive	Binary alloy with low eutectic point	Nanometal formation technique

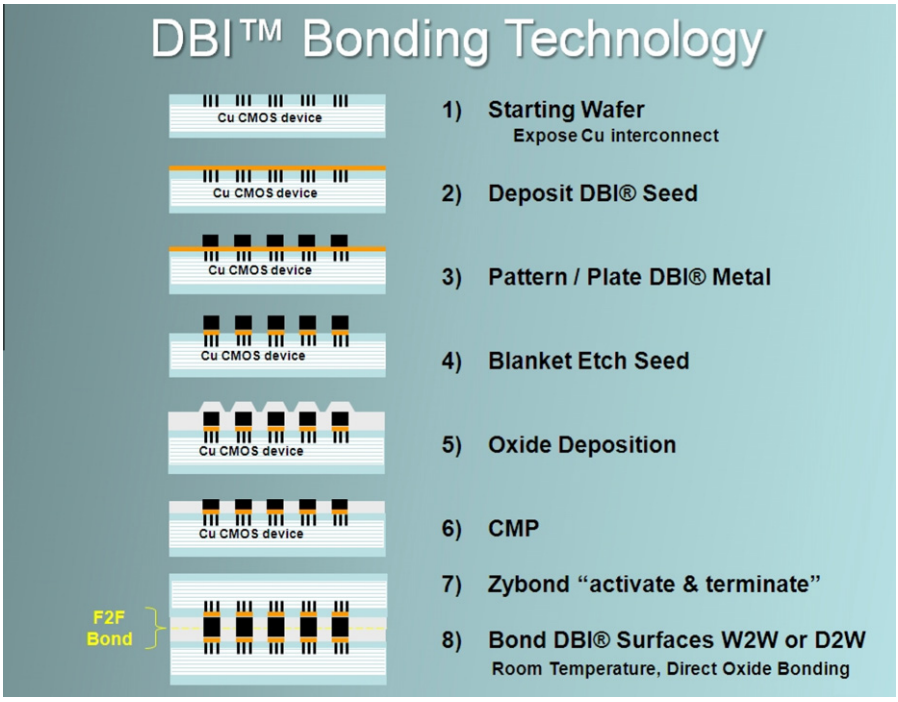

Fig. 1. DBI technology process flow [5].

Ziptronix provides a direct oxide bonding technology, named ZiBond™ [2], being completed at room temperature with no residual stresses. It employs NH_4OH exposure to terminate oxide surface with amine groups, and followed by direct surface contact to form covalent bonds spontaneously. The Ziptronix's DBI (Direct Bonding Interconnect) technology [3–5] is an evolution of ZiBond™, which utilizes the standard chemical–mechanical polish (CMP) technique to expose metal patterns embedded in the silicon oxide surface of each chip or wafer, thus enabling silicon and other technologies to be bonded and interconnected in a 3D fashion. Fig. 1 shows the process flow of DBI bonding technology [5]. Patterned metal contact structures are formed on target wafers. Silicon oxide is then deposited to cover the contact structures and wafer surface. CMP is used to planarize the wafer surface and expose the metal contacts. To perform ZiBond, the wafers are oxide-activated first, placed together with the metal contacts opposed, and finally room-temperature direct oxide bonded with preserved alignment accuracy since no external heat and pressure applied. After bonding, 300–350 °C annealing is employed to improve the inter-wafer bond strength and the metal–metal contact quality. With the planarized surface and high bonding alignment accuracy, DBI can provide fine interconnect pitch bonding. Fig. 2 demonstrates 3 μm-pitch bonded structures, allowing an interconnection density larger than 10 M/cm^2 using DBI technology [5].

LETI and STMicroelectronics developed direct hydrophilic Cu–Cu bonding at room temperature, atmospheric pressure, and ambient air [6–8]. This approach requires good hydrophily, low RMS roughness (<0.5 nm) and surfaces with free particle contamination to ensure hydrophilic direct bonding. By means of CMP, the RMS roughness and hydrophily of Cu film are improved from 15 nm to 0.4 nm and from 50° to 12°, respectively. Blanket wafers were successfully bonded at room temperature with a bonding strength

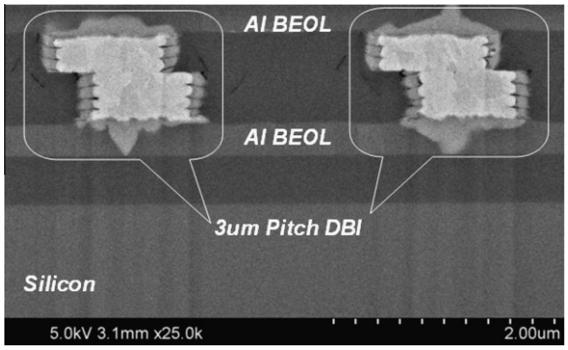

Fig. 2. 3 μm Pitch direct bond interconnects from Ziptronix DBI process [5].

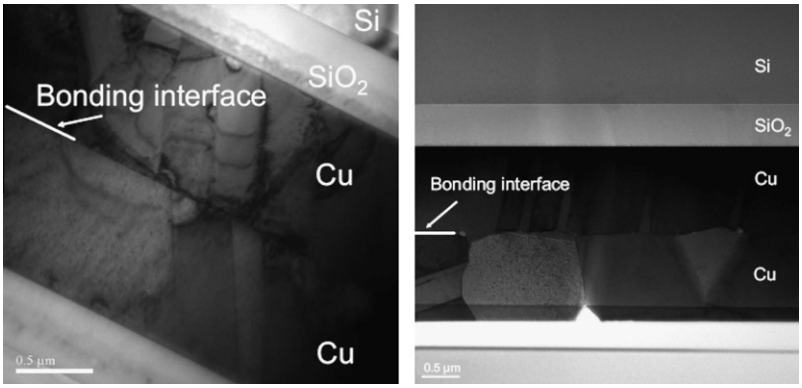

Fig. 3. The cross section of direct copper bonding interface before (left) and after (right) 400 °C annealing treatment [7].

of 2.8 J/m^2. Bond strength was improved to 3.2 J/m^2 after a post-bonding annealing at 100 °C for 30 min [6–8]. Fig. 3 demonstrates the cross section of bonding interface before and after annealing treatment. With a 30 min annealing at 400 °C, the interface turns wavy due to copper interdiffusion and grain growth. The appropriate surface preparation and the optimization of bonding process also allow an efficient conductivity through the bonding interface and a very low contact resistivity could be obtained. The specific contact resistance is 22.5 mΩ μm^2 and 140 mΩ μm^2 for 400 °C and 200 °C annealing, respectively. In addition, the thinning of the bonded pair down to 10 μm without delamination on the top surface confirms the high quality of the bonding. Although direct

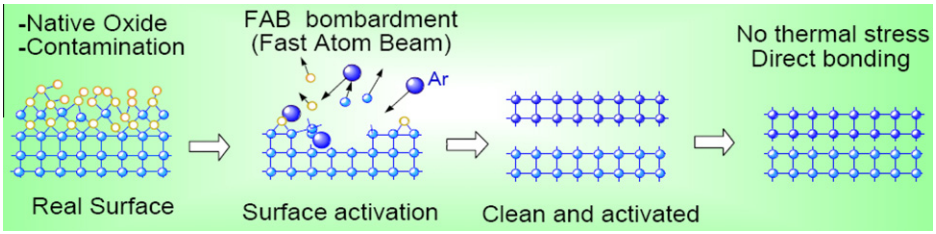

Fig. 4. The schematic flow of surface activated bonding [10].

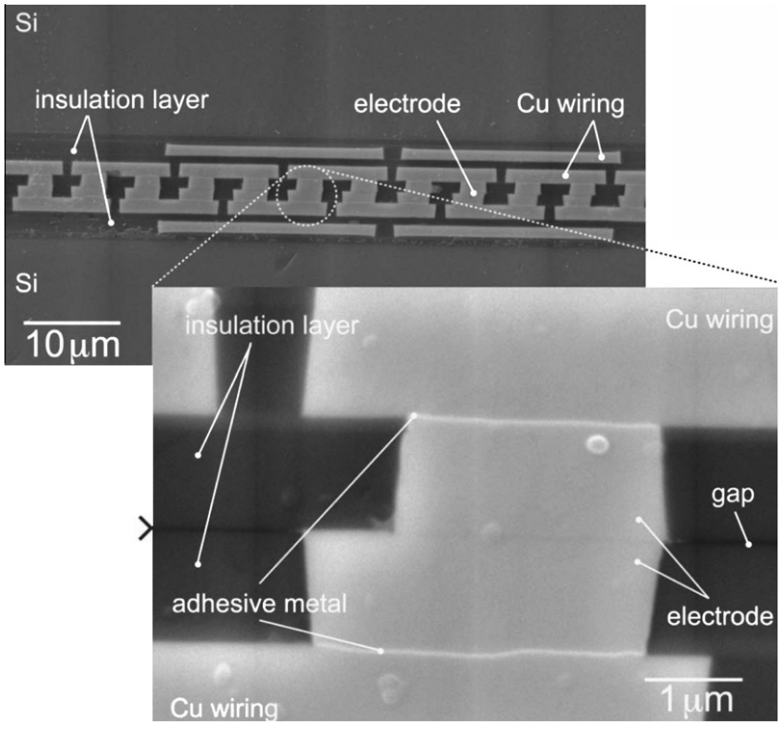

Fig. 5. Bumpless interconnect of 6 μm pitch Cu electrodes with SAB method [14].

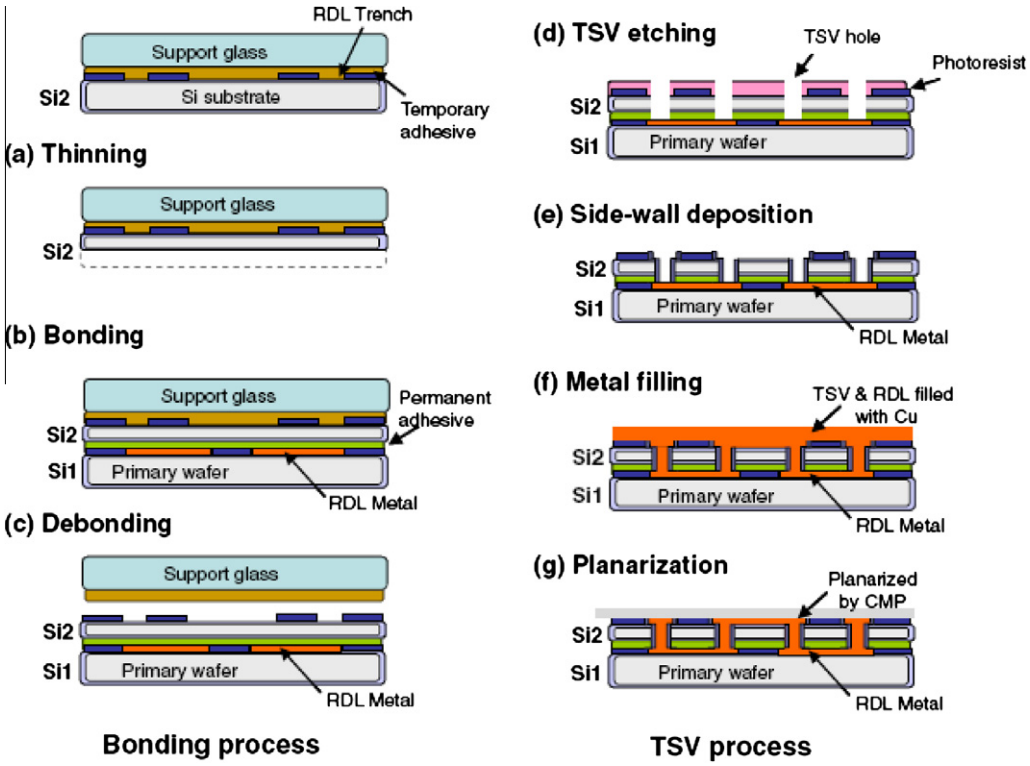

Fig. 6. The process flow of WOW stacking method [21].

copper bonding provides a promising solution for high density stacking with TSV process integration, a post bonding anneal is still required.

3. Surface activated bonding (SAB)

When the conventional direct bonding approach requires high temperature annealing which may result in thermal stress and generation of defects, surface activated bonding (SAB) provides strong bonding strength at room temperature without any annealing steps [9,10]. Fig. 4 shows the schematic flow of SAB technology [10]. Surface to be bonded is sputter-etched by ion or fast atom beam (e.g. Ar–FAB) to remove contaminant layers and absorbed molecules, and brought into contact at room temperature in ultra-high vacuum. When two wafers are mated and contacted in a small area, the contact area propagates spontaneously by surface attractive force between the wafers. Because the surface atoms have dangling bonds after etching and are in unstable state energetically, atoms from two surfaces can be bonded with strong chemical bonds under room temperature and pressure-free conditions. Tensile test results show that high bonding strength equivalent to bulk material is achieved at room temperature [9]. Without any heat treatment and applying pressure, SAB provides low-damage assembly and packaging processes suitable for delicate microstructures.

The University of Tokyo has successfully performed Si–Si, Au–Au, and Cu–Cu wafer bonding by SAB technology at room temperature without annealing [9–14]. The bonding energy (>1.95 J/m^2) and strength (>12 MPa) have been achieved. Fig. 5 presents that the bumpless interconnect of 6 μm pitch Cu electrodes is realized at room temperature with SAB method [14]. The alignment accuracy better than ±1 μm is obtained and the Cu surface with 2 nm roughness can be well-bonded with bond strength greater than 20 MPa. However, the whole bonding process has to be carried out under an ultrahigh vacuum condition (<10^{-5} Pa) that makes these processes expensive for mass production. Therefore, they further developed Si–Si room temperature bonding using fluorine-containing plasma activation [15,16], which can be performed in ambient air without any annealing and chemical cleaning treatment. This becomes an attractive wafer bonding option because of its low stress, damage, and process cost. Possible bonding mechanism, optimized bonding parameters, and bonding strength investigations have been reported in these publications [9–14].

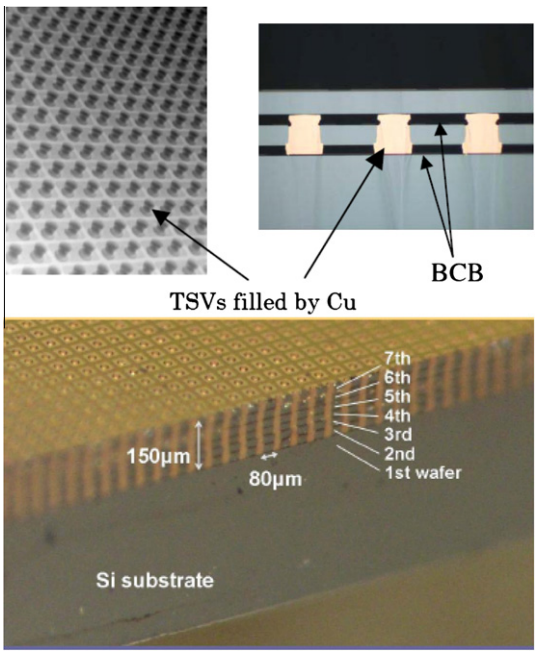

Fig. 7. Seven wafers stacked on a wafer with BCB bonding and TSV interconnection [20].

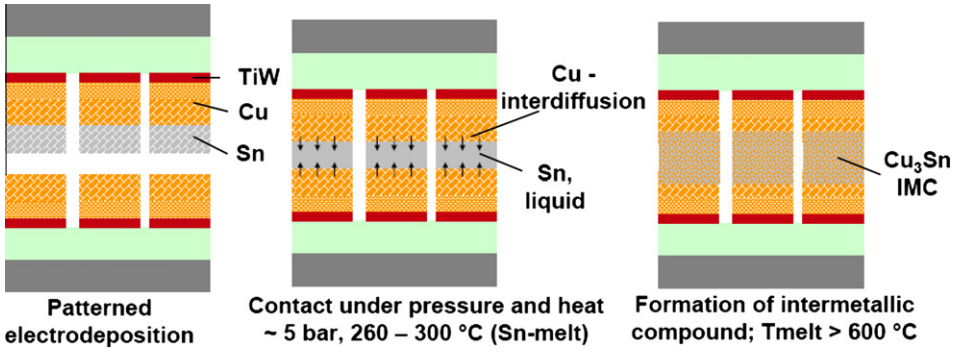

Fig. 8. The illustration of Cu–Sn solid–liquid interdiffusion bonding [26].

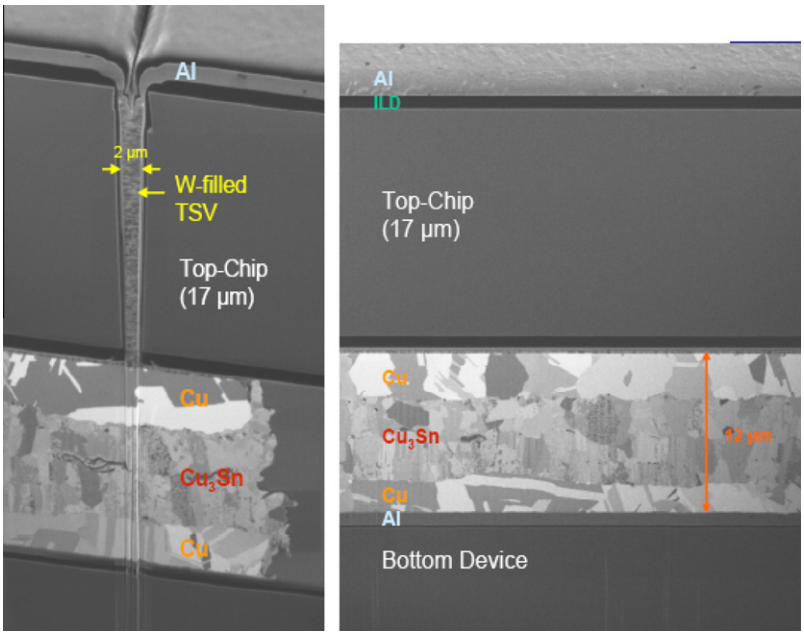

Fig. 9. The integration of 2 μm TSV and Cu–Sn SLID interconnection between stacked chips [26].

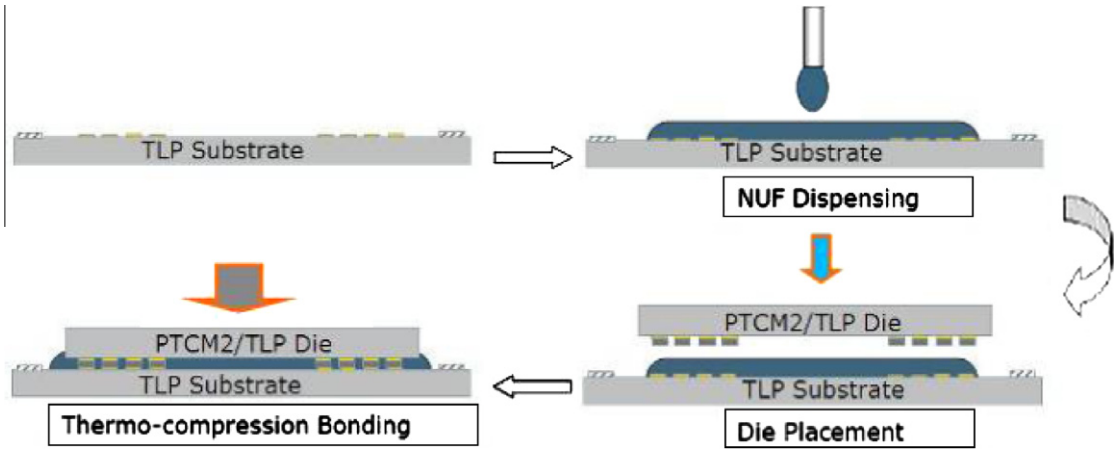

Fig. 10. The process flow of collective transient liquid phase bonding [27].

4. Adhesive bonding

Adhesive bonding is a low temperature and patternable technique using an intermediate layer for bonding. In 3D integration scheme, adhesive material can be used for wafer-to-wafer bonding followed by fabrication of TSV on proper position to form vertical interconnection between stacked wafers. The advantages include low bonding temperature (ranging from R.T. to 350 °C depends

on adhesives used) with required bond strength, excellent surface planarization property, high tolerance to particles, capability for moisture or gas hermetic sealing, and no metal ion contamination to device. However, high aspect ratio TSV formation after bonding increases the fabrication challenge and cost especially as via size becomes small. In addition, the shrinkage property of adhesives decreases the bonding accuracy, which limits its application as well. Therefore, adhesive bonding is usually adopted on wafer bonding with lower accuracy requirement, or collocated with other bonding methods to be an auxiliary to increase the bonding strength. The adhesive materials can be divided into photosensitive and non-photosensitive groups based on the applications. Each group has lots of choices with different bonding temperature and characteristics [17–19]. Nowadays SU-8 and BCB (benzocyclobutene) are the most popular adhesives for precision 3D adhesive bonding below 250 °C with outstanding wafer bonding capability, chemical and thermal resistance, bonding strength, and wide acceptance in IC manufacturing environments.

Wafer-on-wafer (WOW) technology development has used BCB adhesive bonding followed by low temperature TSV fabrication [20–23]. Fig. 6 illustrates the process flow of WOW stacking method [21]. The secondary wafer (Si 2) with transistors and interconnect metallization fabricated is temporarily bonded with support glass, and thinned down to 20 μm. This wafer is then permanently bonded to the primary wafer (Si 1) with BCB adhesive. After removing the support glass from the wafer stack, TSV and RDL are subsequently fabricated by Cu dual-damascene processes. In their scheme, 10 μm TSV with 25 μm depth (20 μm Si + 5 μm BCB) was designed to facilitate TSV fabrication, and 150 °C LT–TSV was developed to lower whole process temperature and induced stress. By repeating the bonding and TSV processes, a multi-stacked integrated circuit can be fabricated. They have successfully demonstrated seven thinned wafers stacking with BCB bonding and Cu–TSV interconnection as the image shown in Fig. 7 [20].

5. Eutectic bonding

Metal eutectic bonding is a popular bonding technique used in advanced MEMS packaging and 3D integration technologies. By performing wafer bonding with two different metals under their eutectic points, the low temperature bonding can be achieved. Because eutectic alloys at the interface are formed in a liquid phase, eutectic bonding facilitates surface planarization and provides a tolerance of surface topography and particles. In addition, there are no requirements on the ultrahigh vacuum bonding condition and post-bond annealing treatment. However, compared with the ultrafine pitch capacity of direct bonding technique, the interconnect pitch is limited by bump-to-bump fabrication. The commonly used eutectic bonding schemes (with the corresponding bond temperature) include Al–Si (~600 °C), Au–Si (380–400 °C), Au–Sn (~300 °C), Au–In (~275 °C), Cu–Sn (250–270 °C), Pb–Sn (~190°), In–Sn (~120 °C), etc. Although Sn–Pb is a mature and low temperature bonding method, it is not preferred due to the lead-free tendency on all electronic products. Au and In are noble metal materials, and the complete consumption of In to transfer to intermetallic compound (IMC) is required to prevent joint remelting due to its low melting point (156.6 °C). Therefore, Cu–Sn eutectic bonding has become a popular low temperature bonding approach for 3D integration.

Infineon and IZM implemented face-to-face chip integration by Cu–Sn solid–liquid interdiffusion (SLID) bonding [24–26]. The SLID principle is to sandwich low-melting component (e.g. Sn) in between two high-melting components (e.g. Cu), and melt the low-melting component at a constant temperature until the completely metallurgical transformations without liquid phase existed. Fig. 8 shows the illustration of Cu–Sn SLID bonding [26]. One of the surfaces to be joined was electrodeposited with Cu, and the other with Cu and a topping Sn layer. When brought together and heated, the sandwich configuration should form a permanent Cu_3Sn IMC joint. The required temperature is often slightly higher than Sn melting point (232 °C), and the requirement of contact force is not critical. The inter-metallic phase is thermo-stable up to 600 °C with electric resistivity between Cu and Sn, which aids to develop a cost efficient bonding process with reliable short interconnects. Fig. 9 demonstrates the successful integration of 2 μm TSV and Cu–Sn SLID interconnection between stacked chips [26].

IMEC developed high throughput die-to-wafer bonding by so-called collective transient liquid phase (TLP) bonding process as shown in Fig. 10 [27]. It adopts Cu–Sn for metallic interconnect in combination with no-flow underfill as the bonding adhesive. The TSV-dies are pick-and-placed onto a landing wafer with the tacky no-flow underfill has been previously coated, which can weakly bond the dies to prevent from moving. This operation is performed at room temperature with the pick-and-place process repeated until the full wafer is populated. The fully populated wafer is then moved to a wafer bonder where pressure and heat are applied to all stacked dies at once. The collective TLP bonding is performed at 250 °C with underfill reflows and the metallic interconnect forms between all stacked dies simultaneously. Fig. 11 demonstrates the optical image of a collectively bonded wafer, where 50 μm TSV die bonded to corresponding landing wafer using Cu–Sn TLP bonding method [27].

ITRI and NCTU developed carrier-less 3D integration platform, shown in Fig. 12, by wafer-level micro-bump/adhesive hybrid bonding technology [28]. Cu–Sn micro-bump for metallic interconnect and BCB polymer as dielectric adhesive are adopted for hybrid bonding at 250 °C. The photo-definable BCB is spin-coated and patterned on both TSV-wafer with Cu–Sn bumps and base wafer with Cu pads to obtain the hybrid schemes. Two wafers are then aligned

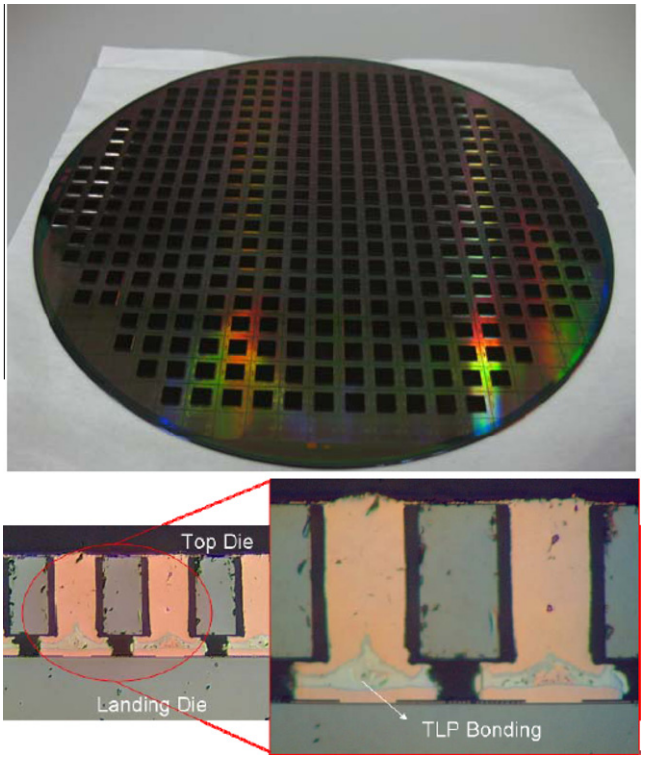

Fig. 11. Optical image of a collectively bonded wafer, where 50 μm TSV die bonded to corresponding landing wafer using Cu–Sn TLP bonding method [27].

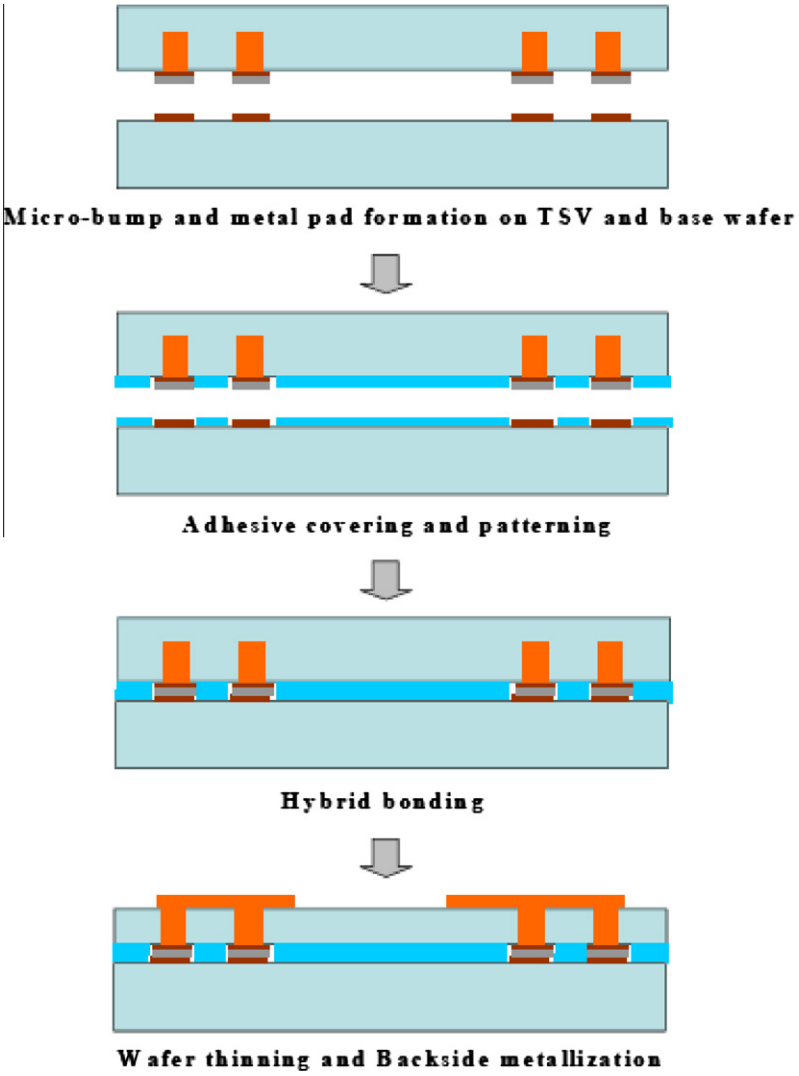

Fig. 12. The carrier-less 3D integration platform developed with micro-bump/adhesive hybrid bonding in ITRI [28].

and bonded to form solder joint interconnect with BCB adhesive sealed bonding to increase the bond strength and joint reliability. With the adhesive serving reinforcement of the mechanical stability, the bonded TSV-wafer can endure the severe wafer thinning process to expose the TSV, and implementation of the backside RDL processes with the base wafer support. If required, a third wafer (or more) can be further added to achieve multi-layer 3D structures [28].

6. Nanometal bonding

The general metal diffusion bonding, such as Cu–Cu and Au–Au bonding, provides intrinsic interconnect and excellent mechanical strength. However, the bonding temperature higher than 300 °C and high bonding pressure are required to perform the bonding integrity. Recently the nanometal materials are studied to lower the bonding temperature and pressure. RPI developed low temperature wafer bonding by Cu nanorod array [29–31]. They observed that surface melting disintegration of the nanorod arrays occurred at a temperature significantly below the Cu bulk melting point. Base on this unique property, they performed wafer bonding using Cu nanorod arrays as a bonding intermediate layer at temperatures ranging from 200 °C to 400 °C. Fig. 13 shows the schematic illustration of the Cu nanorod bonding [31]. The wafers are coated with a vast array of Cu nanorods with a diameter of 10–20 nm grown by an oblique angle deposition technique. Subsequently the two wafers are bonded at an external pressure of 0.32 MPa to facilitate the formation of nano-structured bonds at the interface. The FIB/SEM results show that the Cu nanorod arrays fused together accompanying by grain growth at a bonding temperature as low as 200 °C. A dense Cu bonding layer with homogeneous structure was obtained upon 400 °C as the image shown in Fig. 14 [29].

IZM developed another low temperature bonding approach by nanoporous Au bump interconnect [32]. Nanoporous gold bumps were deposited on silicon wafers by electroplating silver–gold alloy followed by etching silver to provide a nanoporous gold layer as an open-porous sponge with 70–80% porosity. The porous interconnects provide advantages, such as compressibility to compensate for any coplanarity and particle issues, and reduced stiffness results in potentially higher bond yield and extended reliability. Nanoporous gold bumps were bonded each other and investigated the microstructure revolution at different bonding temperatures. As the results shown in Fig. 15, the nanoporous structure was densified with temperature increasing from 150 °C to 400 °C, which turned the brown bump color into yellow [32].

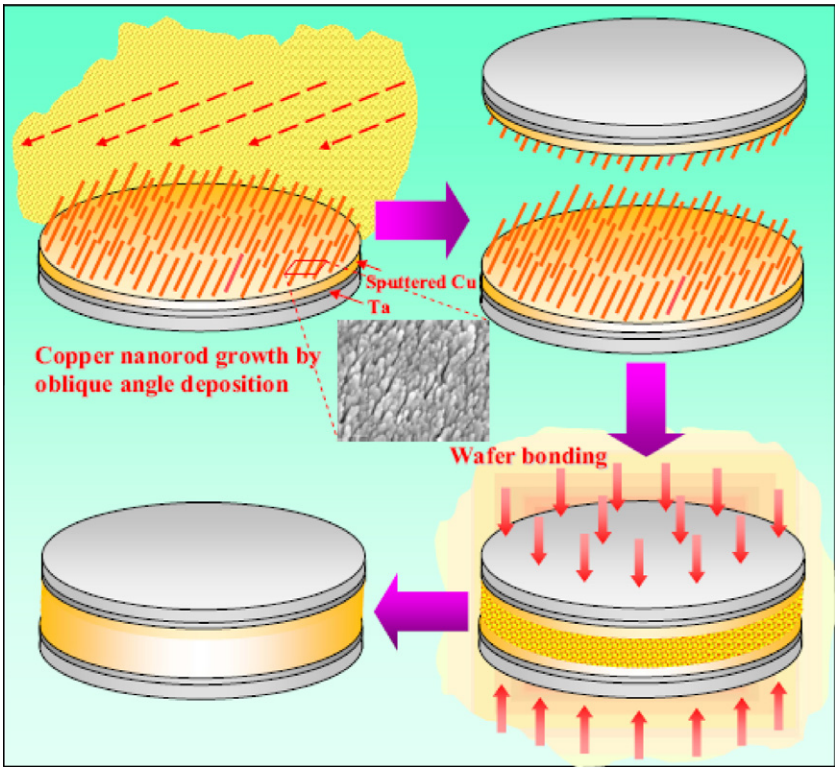

Fig. 13. The schematic illustration of copper nanorod bonding [31].

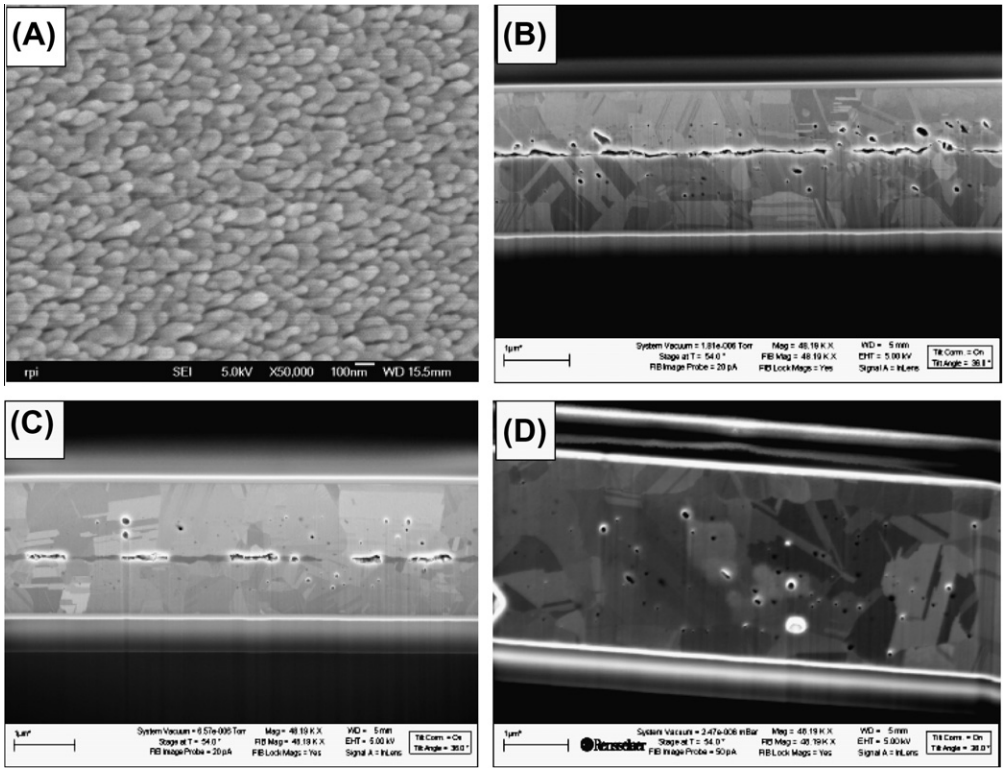

Fig. 14. (A) SEM image of as-deposited copper nanorod arrays and cross-sectional FIB/SEM images of copper nanorod bonding at (B) 200 °C, (C) 300 °C and (D) 400 °C respectively [29].

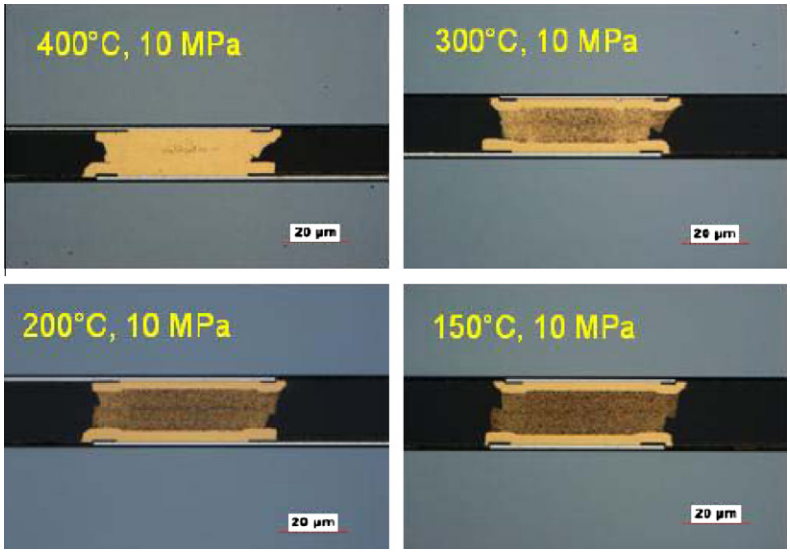

Fig. 15. Flip chip bonding of nanoporous gold bumps by different bonding temperature at 10 MPa [32].

7. Outlook

Various low temperature bonding technologies have been addressed and compared in this paper. Considering the application for mass production, DBI and copper direct bonding with oxide hermetic sealing are good alternatives. Both methods have not only the excellent capacity for fine pitch and high density integration but also the constitutional advantage on the flow separation of short contact bonding and batch annealing treatment, which is suitable for high throughput production without bottlenecks. In addition, they provide the gate-level truly 3D integration with the significant benefits of size reduction, increased system performance, low power consumption, and reduced production costs. However, it is expected the annealing temperature could be further lowered to meet the requirements of low thermal budget and sensitive devices. SAB technique is another candidate if the high requirements of bonding environment could be improved. As aforementioned, room temperature bonding performed in ambient air has been successfully demonstrated using specific plasma activation. It will become an attractive bonding approach with low stress, damage and production cost. Furthermore, low temperature hybrid bonding by eutectic bumps and adhesive sealing provides another potential solution for 3D integration. From the back-end process and packaging point of view, it is a simplified and low cost bonding approach with high mechanical strength and reliability, and will be also suitable for future industrial applications.

8. Conclusions

This review paper summarizes various low temperature bonding technologies for 3D integration, including the research and development efforts from corresponding companies or research institutes. Direct bonding enables bonding at room temperature with very fine interconnect pitches, but extremely flat surface and post-bond annealing treatment are required to guarantee the bonding performance. SAB technology provides room temperature direct bonding without the requirement of post-bond annealing, but the severe bonding environment is a drawback for industrial application. Adhesive bonding has better particle contamination tolerance, but TSV formation after bonding limits via aspect ratio and density. Eutectic bonding and nanometal bonding for direct interconnection can be performed at low temperature. However, the un-bonded air-gap area may result in reliability issues, which is recommended to be improved by hybrid bonding approach. Several potential technologies, including innovative direct bonding such as DBI and copper direct bond, SAB with specific plasma activation, and low temperature hybrid bonding by eutectic bump and adhesive sealing, are good candidates with significant advantages on low damage to device, high throughput and low production costs for mass production applications.

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