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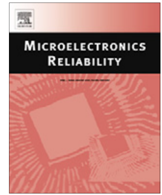

Invited Paper

Wafer-level Cu–Cu bonding technology

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ABSTRACT

Semiconductor industry currently utilizes copper wafer bonding as one of key technologies for 3D integration. This review paper describes both science and technology of copper wafer bonding with regard to present applications. The classification of Cu bonding, bonding mechanisms, process developments, its microstructure evolution, as well as other characterizations are reviewed. Researches about patterned Cu bonding, future prospects, and 3D integration using Cu bonding are discussed in this paper.
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1. Introduction

Three-dimensional integrated circuits (3D IC) have been regarded as the most hopeful solution for increasing transistor density in the future semiconductor applications. The main advantages of 3D IC include heterogeneous integration with abbreviated interconnections due to vertical stacking [1]. At present, copper wafer bonding is one of the most promising approaches for 3D IC applications because it provides low costs and high throughput for advanced CMOS integration when compared to other bonding approaches. One purpose to use Cu as bonding medium is because of its usage in metal level [2]. Cu bonding becomes beneficial in the 3D structure from its excellent electrical and thermal conductivity.

Academic institutions initiated methodical and purposeful studies of copper wafer bonding around 2000, after which many researchers anticipated that this approach would become the key technology for 3D IC. Hence, thorough researches were undertaken in order to uncover the evolution of its mechanisms and scientific principles [2]. In addition, concerns over the reliable Cu bonded structures coupled with overall thermal budget restrictions, required that a set of parameters be established for optimizing bonding process conditions by balancing mechanical bond strength and Cu bonding temperature. Current researches on copper wafer bonding, including 'hybrid copper bonding' [3], both from academic and industrial institutions focus on the application for 3D integration. This review paper will give a detailed report about wafer-level Cu bonding technology.

2. Current Cu bonding techniques

Because copper wafer bonding layers simultaneously offer electrical connection and mechanical strength, the process is attractive for 3D IC applications. The methodology has two classifications: One is 'thermal-compression Cu bonding', also known as diffusion Cu bonding, a technology that achieves good wafer bonding results. Although its design scheme is simple and costs less, thermal-compression Cu bonding does require higher temperature. The second is 'surface-activated bonding', a method that, when compared to thermal-compression, enables two Cu surfaces to bond at room temperature [4]. Both techniques are currently employed to achieve successful Cu bonding as described below.

2.1. Thermal compression Cu bonding

The use of thermal-compression bonding in 3D applications establishes both mechanical and electrical connections between two wafers in one step. Cu films from both wafers bond on the application of compressive force and heat which allows sufficient adhesion for bonding. Thermal compression differs from surface activation in that it uses a sufficiently high bonding force to ensure contact between wafer surfaces at 400 °C or lower and completes the inter-diffusion of Cu atoms. The post-bonded wafers are optionally then annealed in nitrogen to further enhance the bond strength.

Since this bonding mechanism is based on inter-diffusion of Cu atoms, it requires neither ultra clean surfaces nor ultra-high vacuum. However, the increased bonding temperature is an important factor because higher temperatures enhance diffusion and thus improve bonding quality. The latter characteristic leaves room for the development of innovative improvements that may achieve comparable bonding at lower temperatures. Another consideration is that bonding temperatures must be compatible with the temperature limits that do not negatively affect device performance. On the other hand, thermal-compression Cu bonding has both attracted and received greater attention and development in industry as well as academia due to its simpler design and lower cost requirements. Hence, this paper places greater emphasis on this technique, including the development and achievements of thermal-compression-Cu-bonding.

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2.2. Surface activated Cu bonding

Typically, thermal compression bonding of Cu layers is performed at temperatures ⩾300°. Hence, thermal costs are restrictive and as such have called for methods that decrease required bonding temperature if possible, which then led to the development of the surface activated process as a low temperature bonding methodology. In this latter scheme, the bonding process begins by preparing two exquisitely clean and flattened copper surfaces with the intention of achieving sufficient bonding energy from extant adhesive forces between two clean solid surfaces under contact [5,6]. This process and equipment aims to achieve Cu bonding at room temperature and is technologically, conventionally and conditionally made possible only within an ultra-high-vacuum (UHV). In addition, both copper surface-activated wafers must be free of foreign contaminants. All surface contamination and native oxides must be removed so that unflawed surfaces are presented for activation. Hence, this method requires ultra-high-vacuum (UHV) conditions to complete the bonding process at room temperature.

There is no need for thermal annealing to increase bonding strength in this scheme. The bonded structures acquired by this method show such robust strength within a 'void free' interface that tensile tests demonstrate the bonds are equivalent to those of bulk materials achieved at low temperature. For example, utilizing the AFM tip pull-off method in 2007, Tadepalli and Thompson measured the adhesive strength of Cu–Cu bonds at about $\sim$3 J/m^2 [7]. These Cu–Cu bonds had been accomplished at room temperature under UHV as described [7].

In addition to Cu, this same bonding technique can be applied to all materials as the bonding mechanism is based on contact between activated surfaces. Furthermore, when bonding two dissimilar materials, problems that otherwise occur due to thermal mismatch are of less concern. Nevertheless, an Ar ion beam is used to bombard the Cu surfaces within UHV to activate Cu surfaces prior to bonding. Hence, the process and equipment required for this method is complex and remains a major concern when utilizing this technique for mass production.

3. Cu–Cu bonding mechanisms

The investigation of Cu bonded layers includes the evolution of microstructure morphology and grain orientation during the process of bonding. The morphological observations undertaken include distinct, non-distinct and zigzag interfaces within the bonded layer as well as any abnormal grain developments occurring during bonding and annealing. Further discussion of the relation between these morphologies now follows.

3.1. The evolution of microstructure and morphology in Cu–Cu bonding

Bonded Cu grain structure reaches a steady state of homogeneity after the post-bonding nitrogen anneal. After bonding, some bonded wafers were annealed at 400 °C in ambient nitrogen from 30 to 60 min. Fig. 1a–c shows cross-sectional TEM images of the bonded Cu–Cu layer [8]. The sequence of changing morphology during the process of bonding is as follows: Fig. 1a is before bonding; Fig. 1b is after 30 min of bonding; and Fig. 1c is after 30 min of both bonding and nitrogen annealing. As shown in Fig. 1a, the pre-bond Cu grains have a major (1 1 1) grain orientation with an average size of 300 nm. In Fig. 1b, the bonded interface is jagged and clearly observable after 30 min. The distribution of grain size here ranges from 300 to 700 nm. Additionally, these grains have respective orientations of (1 1 1), (2 0 0) and (2 2 2). After a further

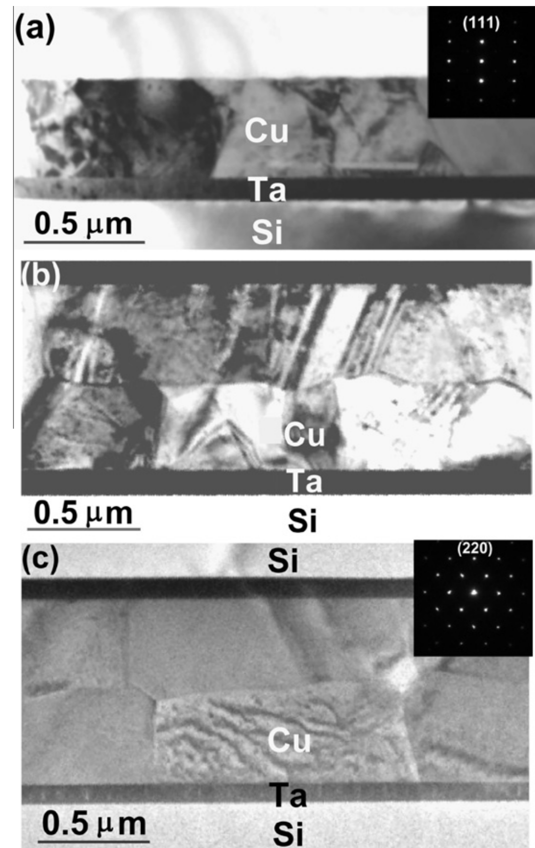

Fig. 1. (a–c) TEM images of Cu bonded layers (a) before bonding, (b) after 400 °C bonding for 30 min, and (c) after 400 °C bonding for 30 min followed by nitrogen anneal at 400 °C for 30 min [8].

30 min of temperature bonding along with annealing in ambient nitrogen, Fig. 1c shows well developed grain texture with a preferred (2 2 0) orientation and 800 nm grain size [8].

According to the results of these morphological observations, after 30 min of bonding one may clearly see that inter-diffusion of both Cu surface layers began during initial bonding. The jagged Cu–Cu interface that follows in Fig. 1b, however, indicates incomplete grain growth. As also shown in Fig. 1b, both Cu surface layers remain distinguishable, which demonstrates that both bonding time and supplied energy were insufficient to complete any grain growth of the bonded layer. During the post-bonded annealing stage, sufficient energy is then imparted to complete the grain growth. The distinguishable interface eventually vanishes as both Cu films homogeneously merge during the final phase. As seen in Fig. 1c, therefore, the two Cu layers are no longer discernable [8].

Fig. 2 shows a distribution of average grain size under different process durations and conditions [8]. The large distribution of grain

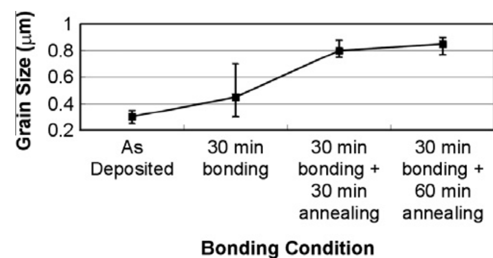

Fig. 2. Average grain sizes as a function of different bonding conditions [8].

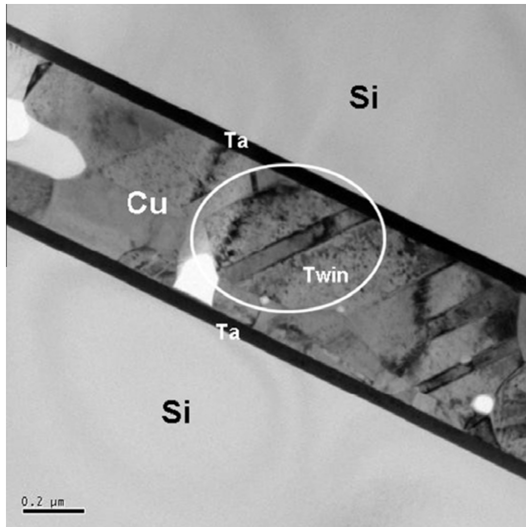

Fig. 3. The morphology of Cu bonded layers [9].

size perceived after 30 min of bonding is due to incomplete grain growth. However, beyond the 30 min period of annealing, no significant increase in grain size is observed. Nevertheless, grain growth does accelerate during the first 30 min of the post-bonded initial annealing stage. This phenomenon demonstrates that a certain amount of time is required for the annealing process to complete grain growth. Fig. 3 shows a well-bonded Cu–Cu layer that lacks any discernable interface left over from the initial bonding process [8]. Instead, grain structures and twins were observed across the bonded layer [9], which indicates that the both Cu layers have merged to become one bonded layer and interface is removed [10].

3.2. Grain orientation in Cu bonded layer

Grain orientation is also important and when compared to the behavior of the bond's evolving morphology during the bonding process, a similar pattern of preferred orientation evolves during the development of the Cu bonded layer. Fig. 4 shows XRD patterns of freshly deposited Cu and bonded layers under different conditions in which the preferred orientation changes from (1 1 1) to (2 2 0) [8]. Here Cu film demonstrates a (1 1 1) preferred grain orientation with marked intensity and sharpened curve. During further annealing, however, in-plane strain increases yet again when the bonded wafer is heated from room to high temperature. Hence, secondary grain growth occurs yielding a (2 2 0) orientation. This energetic advantage minimizes stress forces in the bonded layer so that after bonding and annealing, growth of

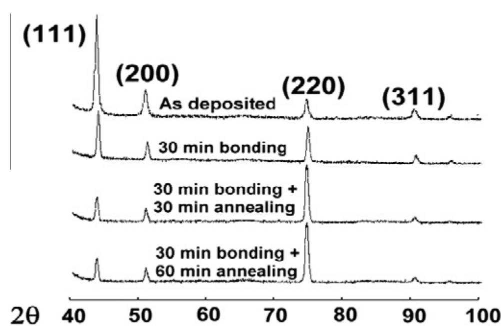

Fig. 4. XRD patterns for different bonding conditions [8].

(2 2 0) oriented grains occurs more readily than do orientations of either (1 1 1) or (0 0 2). Furthermore, since (2 2 0) grains have lower stress yields, the growth also minimizes surface tension. This yielding and energy minimization of stress throughout the entire system consequently leads to this particular grain growth [8,11].

The Cu bonded layer is in a state of biaxial strain due to its attachment to both sides of the relatively thick Si substrate. In addition, in-plane stress on the grain as well as products from both biaxial strain and modulus are also functions of the grain orientation factor *Cijk*, which means that the yield stress of the grain also depends on its orientation. Previous research has demonstrated that the orientation factor *Cijk* of (2 2 0) has the least value—calculated at 1.42 as compared to 3.46 of (1 1 0), which is the largest [12]. This means that the yield stress of (2 2 0) is much smaller than that of (1 1 1). Therefore, grains of initially equal sizes such as (2 2 0) will yield before (1 1 1) grains. Once the (2 2 0) grains yield, they have an energetic advantage for further growth. Since Cu, with a preferential (1 1 1) orientation, also has a longer electromigration lifetime than those that prefer the (2 2 0) orientation, any abnormal (2 2 0) grain growth during Cu wafer bonding is hardly desirable for IC fabrication. It is therefore necessary to develop methods that suppress transformations of (1 1 1) to (2 2 0) while maintaining maximum bonding strength during Cu wafer bonding [8].

4. Cu bonding development

Wafer bonding, including thermal-compression Cu bonding, consists of a two-step process. The first is preparation of the wafer surface in terms of cleanliness, surface chemistry and intermediate layer properties. The second is the actual bonding. When 'as-prepared' Cu-coated wafers are properly aligned, the wafer pair is clamped to a bonding chuck and transferred to the bonding chamber. The chamber is then evacuated after a nitrogen purge and followed by temperature elevation of the chuck while force is applied to the wafer pair. The Cu metalized wafers are successfully bonded at 400 °C under 4000 mbar for 30 min, then annealed at 400 °C for 30 min in a nitrogen ambient atmosphere [10]. Post-bonding annealing is necessary in order to facilitate further Cu interdiffusion and grain growth so that higher bond strength is achieved.

As bonding quality is directly associated with the fabrication process and bonding parameters, systematic trials are required to obtain the desired data and results. The following section describes the development of a quality fabrication process for Cu bond pads and Cu bonding parameters. Although most results were developed at the wafer-level scale, consequent conclusions and guidelines remain valid for die-level Cu bonding technology.

4.1. Fabrication and surface preparation of Cu bond pads

An appropriate design for Cu damascene bond pads can increase the area of bi-surface contact and thus provide greater facilitation for a more comprehensive bonding. Two Cu damascene bond pads encompassed by recessed materials such as oxide are required to achieve full contact. Therefore, SiO_2 CMP followed by dilute HF wet etching are steps utilized for surface treatment in the oxide recessing process [13]. These steps are undertaken to achieve the best possible Cu bond pad fabrication. Surface cleanliness is crucially significant to the quality of the final bonding, most especially when bonding temperature is low or bonding duration is abbreviated. Surface cleaning includes HCl wet cleaning plus a DI water rinse in order to achieve the cleanest possible copper surface [10]. All surface contamination and native oxide must be removed in order to assure that both Cu surfaces are fully engaged during

the bonding process. Hence, prior to bonding, the process of Copper pad fabrication in addition to surface treatments directly affect the quality of Cu bond pads.

4.2. Cu bonding parameters

After preparation of the Cu surface, the actual bonding process is accomplished in compliance with several parameters which include the ambient condition of the chamber, bonding temperature, pressure, duration and annealing options. However, due to cost considerations and device performance limitations, certain modifications of these guidelines must be adhered to.

There is no mistaking that superior ambient conditions within the bonding chamber improve the quality of Cu–Cu bonding. Hence, a high vacuum environment is applicable in order to reduce both surface contaminants and the formation of Cu surface oxides. To achieve both ends and thus avoid poor bonding quality, vacuum conditions of 10^{-4} torr, as provided by standard commercial thermo-compression bonders, have demonstrated the facility conducive for good bonding quality [10,14]. In addition, nitrogen gas purges of the bonding chamber (vacuum) optimize the ambient conditions of the chamber [10].

The required bonding temperature parameters dominate the quality of final bonding because the bonding mechanism is based on Cu atom inter-diffusion. Higher bonding temperatures increase diffusion activity [15], and consequently improve the bonding quality while, simultaneously, an appropriate temperature ramping rate may be kept as low as 6 °C/min [14]. However, owing to thermal budget device limitations, temperature ramping must not rise too high or too quickly as either may damage extant devices and affect their performance.

For complete bonding, sufficient bonding pressure is required to ensure that both Cu surfaces approximate adequately for robust adhesion. Current commercial schemes utilize a minimum bonding pressure of $\sim$1000 N before any temperature ramping is initiated; after which 10,000 N is applied for patterned Cu pads on 200 mm wafers [10].

Longer bonding duration also improves the bond's quality [15]. However, when considering mass production for 3D IC applications, abbreviation of the bonding process duration is a significant cost consideration for high output manufacturing. Nevertheless, in order to achieve the best bonding quality, a processing duration longer than 30 min is necessary for wafer-level Cu bonding.

During the post-bonding anneal in ambient nitrogen, bonded layers are provided with sufficient energy to complete optimal grain growth and thus achieve a stable, steady state microstructure [10]. Hence, the post-bonding nitrogen anneal improves both the microstructure and strength of the bonded layer when the bonding temperature is >300 °C. If the bonding temperature is <300 °C, the strength of the bond's adhesion may be too weak to withstand the thermal stress of the post-bonding annealing treatment [16].

5. Cu bonding technology

5.1. Structural design

Bonding quality also has additional dependencies related to the structural design of the Cu pads and layout of the circuits. Using the 'seal design' prevents moisture from permeating the bonding area. This unique structural design provides excellent mechanical support [13]. Fig. 5 shows such a seal design with regard to extra-Cu-bond regions that circumvent the electrical interconnects as well as the chip's edge [13]. In addition, it must be remembered that the structural design of the Cu bond pads themselves also serves to determine not only the circuit's placement but the bonding quality as well.

The placement of a Cu bond pad affects the available bonding area for the entire wafer/chip, and both the pad's pattern-density (total bond area) and size (interconnect size) are related to placement. Several pattern densities from <1% to 35% have been investigated for effects on bonding quality [14]. Failure percentages in the dicing test are reduced as bond density increases. The bonding area usually passes the dicing test when the pattern density is >13% [14]. Several sizes of Cu bond pads from 2 to 16 μm have been investigated to assess the pros and cons of their respective structural designs with a view towards bonding strengths of corresponding sizes of equal bonding density (i.e., total bonding area). Fig. 6 illustrates bonding qualities for a variety of Cu bond pad structural designs [13]. However, we note that, on the basis of experimental results, bond pad size neither correlates with nor strongly affects consequent bonding quality [14].

5.2. Alignment accuracy of Cu–Cu bonding

Wafer to Wafer alignment is a very important step for 3D integration such that high alignment accuracy is a necessary requirement for many integration schemes. After wafer surface cleaning and Cu deposition processes, the pair of wafers must come into contact with their corresponding contact pads. The accuracy of alignment for each layer strongly correlates with functionality, reliability and performance of the Cu bonded structure. Bonded structures are readily and directly inspected by microscopy if the wafers are transparent. If the wafers are opaque, an IR inspection is undertaken instead to assess alignment accuracy. Fig. 7 shows an IR image of bonded Cu circular-to-pad structure [14]. Using the optimized bonding conditions as reported above, any post-boding misalignment can be kept within a 0.5 μm range (the alignment resolution of an EVG aligner) [14].

5.3. Reliable Cu bonding and multi-layer stacking

As shown in Fig. 8, Cu bonding technology was initially applied to achieve multi-layer stacking structure [17]. After completing the copper deposition process on the bottom wafer, two wafers are bonded with Cu film as the bonding medium. They are then ground and etched-back, followed by the removal of any Si substrate after which copper is again deposited in preparation for the next upper wafer bonding [17].

Multiple layer silicon stacking based on Cu bonding has successfully been applied to 3D integration technology. A four-layer-stack structure is observed in Fig. 9 that demonstrates the complete homogeneity of all bonded Cu layers and furthers shows that the original bonding interfaces cannot be distinguished [17]. This indicates that the bonded structures are strong enough to withstand applied stress during both grinding- and etching-back stages.

The four-layer stacking in Fig. 9 is the result of a sequential process in which the direction of stacking uses face-to-face bonding followed by face-to-back bonding [17]. A multiplicative approach is used to achieve the four-layer stack which is fabricated by bonding two wafer stacks after performing wafer thinning. Subsequent multiplication is possible if necessary and represents an approach representing and promising technique for the development of multi-layer and multi-functional silicon stacks [18]. Fig. 10 shows a four-layer stack achieved by using the techniques described by this flow chart [18].

5.4. Non-blanket Cu–Cu bonding

Cu, as the bonding medium, can be used in either pad-to-pad or line-to-line multi-layer stacking. Fig. 11 shows a cross section of

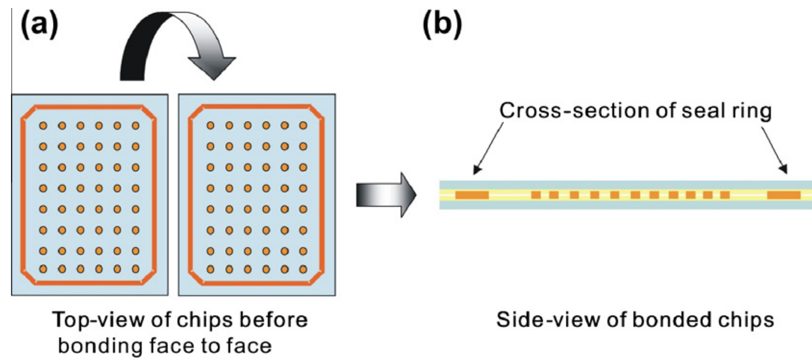

Fig. 5. Schematic diagram of chip seal design concept [13].

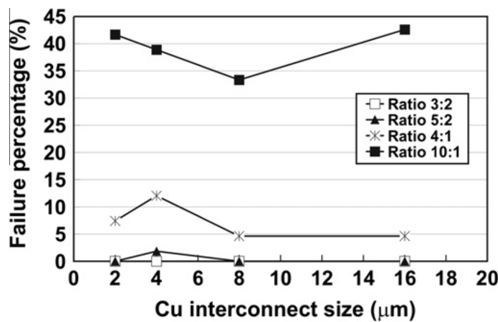

Fig. 6. Failure percentage results of dicing test for various Cu interconnect pattern geometry. Ratio is taken as pitch-to-diameter [14].

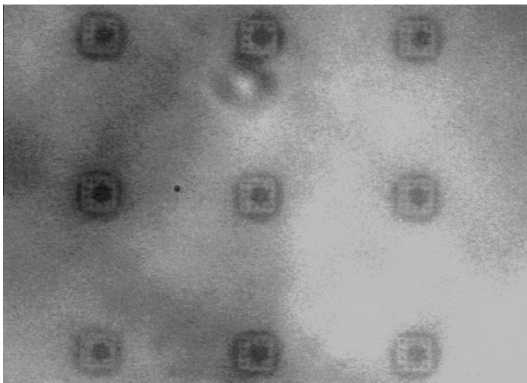

Fig. 7. IR image showing typical misalignment results after bonding [14].

2–9 μm Cu lines in which the spacing between bonded lines is 5.3 μm [19]. Nonetheless, two bonding issues remain that concern reliability; one of which is the formation of a void. Interfacial voids within the bonded lines are shown in Fig. 11 [19]. These faults affect quality and can lead to serious reliability problems. Hence, optimizing bonding conditions for processing must be achieved to prevent void formation. The second remaining concern is that any empty space left between bonded lines reduces mechanical support between the active layers. In addition, empty space may also lead to deficient bonding strength and cause failure to withstand applied stresses during the bonding process. Furthermore, any moisture contained in the empty space can potentially corrode the bonded Cu lines. Therefore, Damascene Cu lines and hybrid bonding of Cu and dielectric bonds have been extensively investigated in order to resolve both issues [20–24].

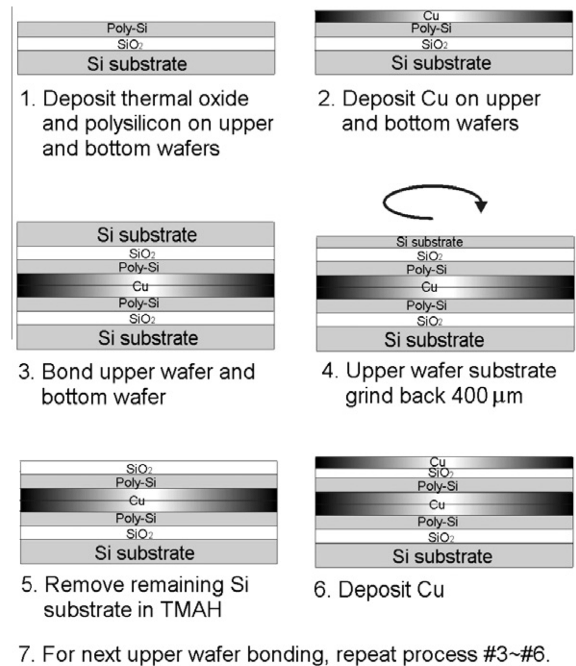

Fig. 8. Schematic diagram of fabrication flow for the multiple silicon layer stacking based on Cu bonding [17].

6. Cu bonding characterizations

A number of techniques can be used to characterize a bond. The quality of a wafer-level Cu bonding can be evaluated by measuring bonding strength, describing interfacial morphological imaging, assessing electrical performance, and investigating thermal reliability. In the following passages, we introduce several ways to evaluate Cu bonding quality, including bond interface imaging, bond strength measurements, electrical connectivity, and thermal reliability. These characterizations help researchers to further their efforts as they represent standard application guidelines in both industry and academia.

6.1. Bonding interface imaging

Cross-sectional imaging analysis is especially useful in the evaluation of bonding layer quality. Electron microscopy via TEM (transmission electron microscopy) or SEM (scanning electron microscopy) is a method used to examine the bonded layer's morphology. Through TEM observation, we can observe the extent of the bonded interface. In addition, a bonded layer that survives

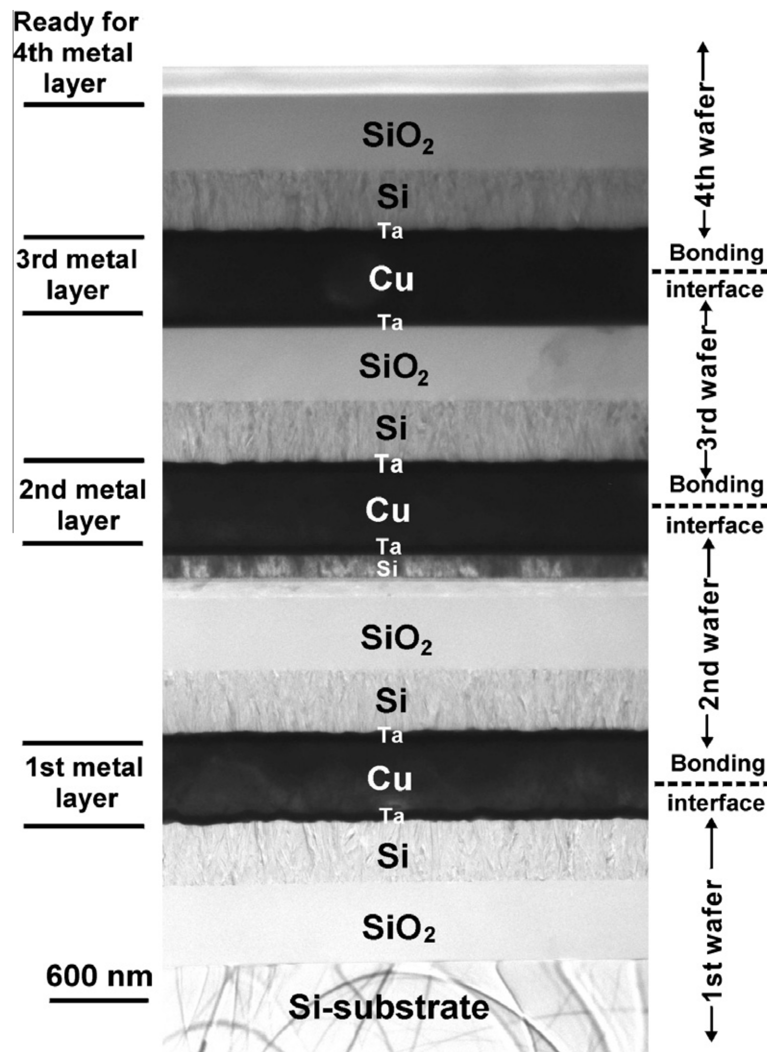

Fig. 9. Multiple silicon layers stacking based on Cu bonding, grind back, and etch back [17].

TEM sample preparation indicates that the bonded layer reached essential bond strength. For examining the morphology of bonded layers, TEM observation results are classified into three groups [15] :

(a) No Interface but Grain Structure; identified as 'Grain'.
(b) Interface Structure; identified as 'Interface'.
(c) And failure of TEM sample preparation; identified as 'TEM failed'.

Fig. 12 shows a reference map that includes results from image analyses and dicing tests under different bonding temperatures and durations and represents an important reference for future real applications [16].

6.2. Bonding strength measurement

Although Cu bond imaging analysis delineates the microstructure morphology of the Cu bonded interface, it nevertheless remains a significant assay to measure the strength of the bond. Various mechanical tests such as the pull, shear, dicing and tape tests have been developed to evaluate Cu bonding strength. For blanket Cu wafer bonding, the optimal Cu bonding strengths as measured by pull and shear tests can be as high as 70 MPa and 80 kg w (*units* referred by the facility) respectively [25]. Among these tests, however, the dicing test is the easiest and most commonly utilized method. The bonded specimen is identified as a "failed piece" if it separates due to the stress of sawing. As stated previously, post-bonding annealing in ambient nitrogen at temperatures >300 °C is necessary to facilitate further Cu interdiffusion and grain growth, which collectively optimize bond strength [25].

6.3. Bonding oxide examination

Residual oxides within metallic lines raise resistance and decrease performance. It is extremely important to prevent atmospheric copper oxidation at elevated temperatures. A well-bonded Cu–Cu layer has a low oxide concentration with uniform distribution. The distribution of oxidation in diverse regions of bonded wafers was examined by energy dispersive spectroscopy (EDS). Fig. 13 illustrates examples of tested areas [10]. In a well-bonded layer, the quantity of oxygen is always less than 3 wt.% when detectable amounts range from 5 to 500 nm [10]. The detection threshold of EDS therefore indicates that original oxides from the Cu layer's surface are removed during pre-cleaning process with HCl and that any remaining oxygen may be considered of negligible effect during bonding. Nonetheless, residual oxygen atoms may readily diffuse into the Cu layer and be distributed throughout

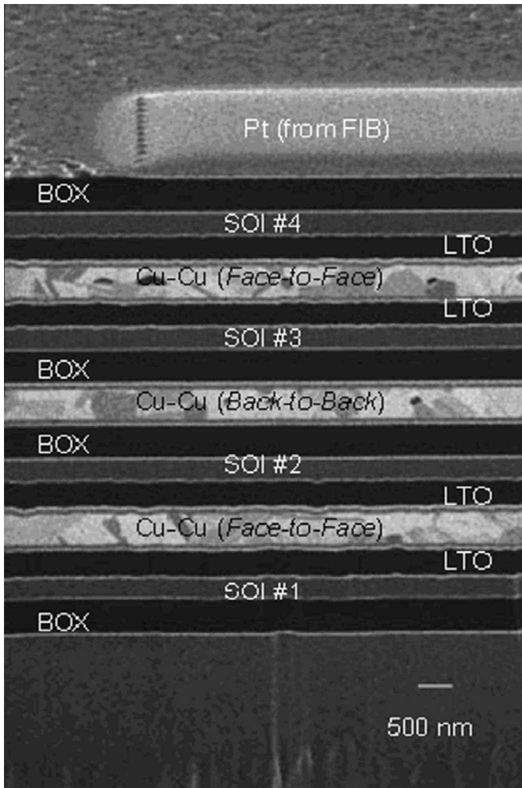

Fig. 10. FIB image clearly shows a silicon four-layer stack achieved by stacking two silicon bi-layer stacks. This paves a promising path to multi-layer and multi-functionality silicon stack [18].

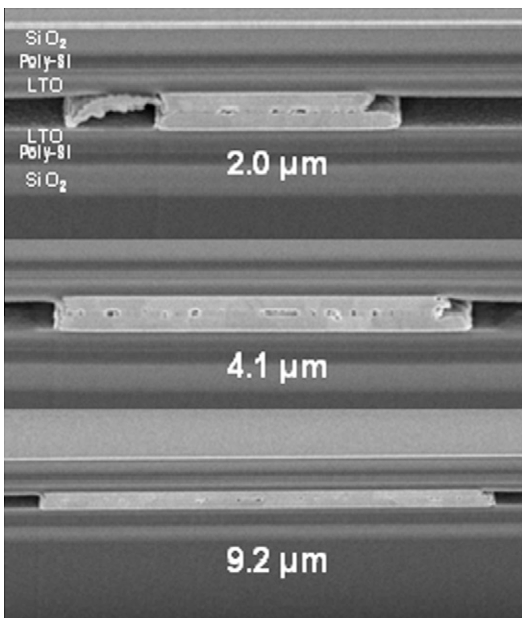

Fig. 11. Non-blanket bonding of Cu lines [19].

during the bonding process. In addition, this may occur with thermo-pressure duration under high temperatures even if surface oxygen on the Cu layer is only partially removed or if new oxides form before bonding. Table 1, for example, shows an example of low level oxygen (less than 3 wt.%) with uniform oxygen distribution across the bonded layer [10].

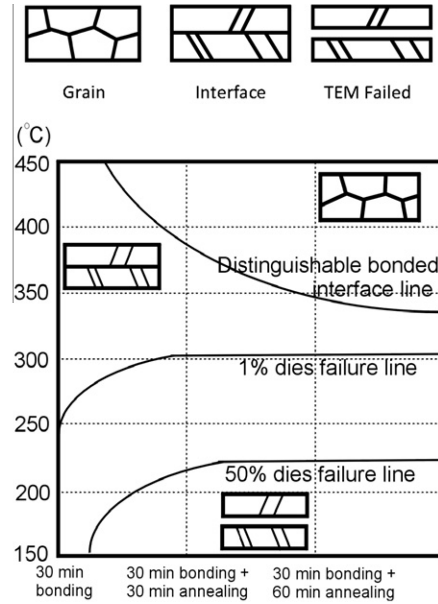

Fig. 12. Morphology and strength map for copper wafer bonding [16].

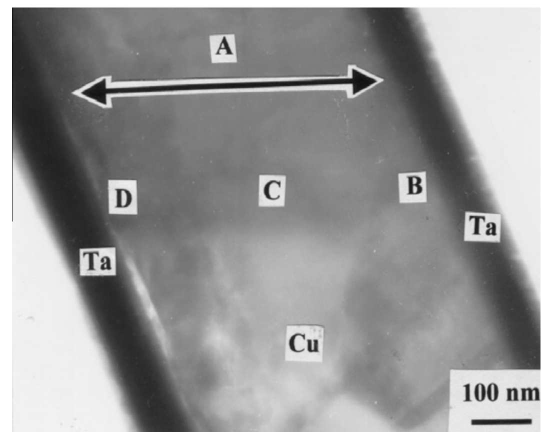

Fig. 13. XTEM image for EDS tested areas [10].

Table 1
EDS examination for oxygen in different areas of the bonded layer [10].

Beam size (nm)	Oxygen (wt.%)	Location description
500	2.67	Whole bonded layer
25	2.13	Near tantalum layer
5	2.22	Near tantalum layer
25	2.53	Near bonded interface
5	2.78	Near bonded interface
25	2.98	Near tantalum layer
5	2.89	Near tantalum layer

6.4. Bonding electrical characterization

To measure the contact resistance of bonded interconnects, a circuit placement on each wafer would be required. Electrical characterization results include specific contact resistance and via chain measurement. A novel test structure for contact resistance measurement of bonded Cu interconnects in three-dimensional integration technology is proposed and fabricated [26]. The specific contact resistance of bonded Cu interconnects with different sizes

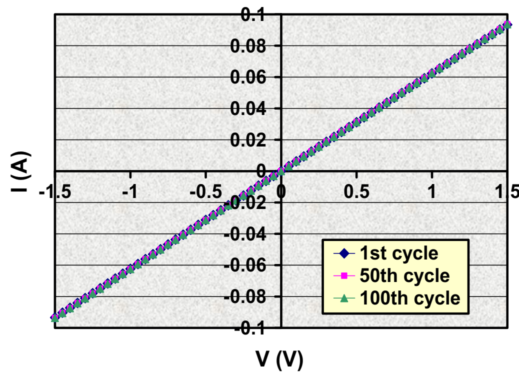

Fig. 14. Stable *I–V* characteristics of Cu bonded chain after multiple current stressing [14].

is approximately 10^{-8} Ω-cm^2 [14,26]. The number is consistent with measurements taken from similar structures build by depositing and patterning metal lines [27,28]. Fig. 14 shows that the chain measurements have excellent performance and stability of bonded interface across wafers after multiple stress cycles [14].

6.5. Cu bonding's thermal reliability

Thermal reliability testing is another common method of evaluating the quality of Cu bonded structures. Various researchers report that well-bonded Cu structures across wafers successfully pass thermal reliability tests [14]. The reported sample was subjected to more than a thousand deep thermal cycles, of between −55 °C and +125 °C, in order to test for thermal reliability.

In addition to the evaluation methods described so far, it will be necessary and of interest for researchers to study the reliability of Cu bonded wafers based on pad size and pitch connection density.

7. Future prospects for Cu bonding

Now regarded as a key technology of 3D IC, the research on copper bonding was initially and systematically unveiled around the year 2000. However, since that time its mechanism and parameters have undergone extensive scrutiny revealing much detail and greater comprehension. Notwithstanding this expanded purview, thermo-compression copper bonding under high temperature remains subject to restraints of thermal budgeting so that reliability issues cause misgivings that can become somewhat problematic. Therefore, academic and industrial researchers have attempted to reduce bonding temperatures by several means as follows:

(1) A lower threshold temperature of 200 °C permitting copper nanorods to partially gather an interface was formed by oblique angle deposition (OAD) in an electron-beam evaporator. This exercise yielded further insights to the sintering phenomenon that occurs with grain growth [29].
(2) Solid–liquid inter-diffusion bonding (SILD) is a method that uses a second metal with a lower melting point such as Sn at 232 °C [30,31]. The Sn is placed between the two copper layers to achieve a Cu/Sn/Cu structure. Typically, it does require a slightly higher bonding temperature than Sn's melting point in order to ensure good bonding quality but at a lower Cu bonding temperature.
(3) Utilizing CMP to reduce the roughness of Cu film from 15 nm to 0.4 nm RMS; copper direct bonding at room temperature under atmospheric pressure has been investigated by CEA-LTEI [32].
(4) A novel method called Cu–Cu pillar bonding has demonstrated an all-copper chip-to-wafer bond by initially electroplating a 20 h growth of 50 μm Cu pillars. After low temperature nitrogen annealing, bonding of Cu pillars then formed via electroless copper plating [33].
(5) SAM (self-assembled monolayer) is formed on a surface and depends on the right temperature and suitable ambient environment. This method offers a passivation layer so that oxide and contaminants on the Cu surface are effectively suppressed by a monolayer that is copper bonded at 250 °C; which presents a significant reduction in bonding temperature as compared to general thermo-compression copper bonding [34–36].
(6) Another innovative technique consists of high precision diamond cutting (milling) of the wafer to planarize its structures [37]. This technique also allows for creating very flat Cu surfaces that can be used to bond die or wafers using Cu–Cu thermo-compression bonding at lower temperatures (i.e., reduced to 250 °C).

8. Application of Cu wafer bonding

As described above, copper wafer bonding that complies with excellent characterizations for stacking integration, mechanism strength and electrical properties using the thermal-compression approach can be offered for applications in BEOL packaging, MEMS and 3D-IC [38–41]. Additionally, its manufacture as CMOS image sensors (CIS), microprocessor/stacked memory, mixed signal AS-IC and mobile electronics may all be fabricated with large numbers of TSVs vertically connecting between chips or wafers. In 2006, P.R. Morrow reported on the integration of 300 mm wafer stacking via Cu–Cu bonding with 65 nm strained Si/low-k metallization CMOS/SRAM technology, which fabrication method has been development utilizing face-to-face Cu pad bonding with sizes of 5×5 μm^2 and 6×40 μm^2 [42].

9. Conclusion

In conclusion, this review paper describes the method of thermal-compression Cu bonding technology for 3D integration. The method is based on mechanisms utilizing high bonding force to ensure contact between two Cu wafer surfaces at elevated temperatures in order to better facilitate the inter-diffusion of Cu atoms. In addition, alternative bonding developments and parameter exploration of reliable bonding processes are also discussed.

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