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A novel switching strategy for FOC motor drive using multi-dimensional feedback quantization

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ABSTRACT

This work proposes a new switching strategy for field oriented control of motor driver to minimize the power of filtered error. By modifying pulse-width resolution and system operating frequency, the switching number is reduced without sacrificing the speed performance. Noise shaping induced by different sampling rates is analyzed. Conventional space vector pulse width modulation is shown to be a special case of the proposed strategy. Another case with zero-bit pulse-width resolution, MDFQM, is proposed. Experimental results show that MDFQM can reduce switching number and heat dissipation of transistors. This property enhances the control efficiency, reliability and durability of power stage.

1. Introduction

Field-oriented control (FOC) (Boldea & Nasar, 1992; Vas, 1990) is widely used for AC motor drives such as induction and PM synchronous motors (Arahal & Duran, 2009; Oliveira, Araujo, & Dias, 2010). The technique enables accurate control of motor current (torque) in both transient and steady-state stages. Implementing a digital control algorithm using FOC on an embedded digital signal processor (DSP) enhances dynamic performance in terms of response time and power conversion. In FOC, the requirement of position sensor data (e.g., encoder) was further replaced by on-line analysis of the voltages and currents in the machine windings (Acarnley & Watson, 2006; Frederik, Belie, Sergeant, & Melkebeek, 2010; Hinkkanen, Harnefors, & Luomi, 2010).

Voltage waveforms of phase windings resulting from FOC signals are typically synthesized by[1] SVPWM when a switch-type inverter is used. For three-phase motors with sinusoidal windings, the FOC signals are the waveforms of the two-phase static frame (α–β axis) obtained from the rotating frame (d–q axis) multiplied by the electronic rotation matrix. There are a number of performance criteria to determine the merit of a modulation scheme for FOC; namely, EMI, harmonic distortion, linear modulation range, inverter efficiency, etc. Multi-level inverters have less harmonic content compared to two-level inverters (Seo, Choi, & Hyun, 2001). Recently, Lopez, Alvarze, Doval-Gandoy, and Freijedo (2008) proposed a complete solution for minimizing switching state transitions during synthesis of multi-level, multi-phase SVPWM within each PWM cycle. Hu, Chen, Shen, and Tang (2011a) treated the same problem via the algebraic techniques and further proved that the solution also gives the least conduction time for the power transistors. However, multi-level inverters require additional power devices and are suitable for high voltage and high power drivers (Kouro, Bernal, Miranda, Silva, & Rodriguez, 2007; Newton & Summer, 1998). For low and medium power applications, two-level inverter is still the major choice in implementation.

Numerous studies have attempted to improve the efficiency of two-level inverters. To reduce harmonics, randomized SVPWM schemes such as randomly sequenced space vectors (Lai, 1999), spread spectrum carrier (Boys & Handley, 1992), dithered switching period (Trzynadlowski, Borisov, Li, & Qin, 2005), and randomly modulated carrier (Habetler & Divan, 1991), have been reported. Further, model predictive control (Arahal, Barrero, Toral, Duran, & Gregor, 2009) and sliding mode control (Oliveira et al., 2010) are applied to current control for induction machines. For since the switching loss of power MOSFETs dominates the total power loss in the inverter (Shen, Xiong, Cheng, Fu, & Kumar, 2006), reducing the switching number without increasing the harmonics distortion is a major issue in improving power consumption and the operational lifetime of the switches (Arnet & Deyst, 2002). For microprocessor implementation, quantizing the duty ratio of each switching period obtains a sampling frequency higher than that provided by PWM. If the switching decision is made at each sampling period rather than each carrier period, the technique is essentially the sigma-delta modulation for the single channel case (Frazier & Kazimierczuk, 2000). Gupta, Ghosh, and Joshi (2009) further investigated the feedback modulation by retaining the triangular carrier. Hu et al. recently proposed a

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[1] SVPWM: Space vector pulse-width modulator.

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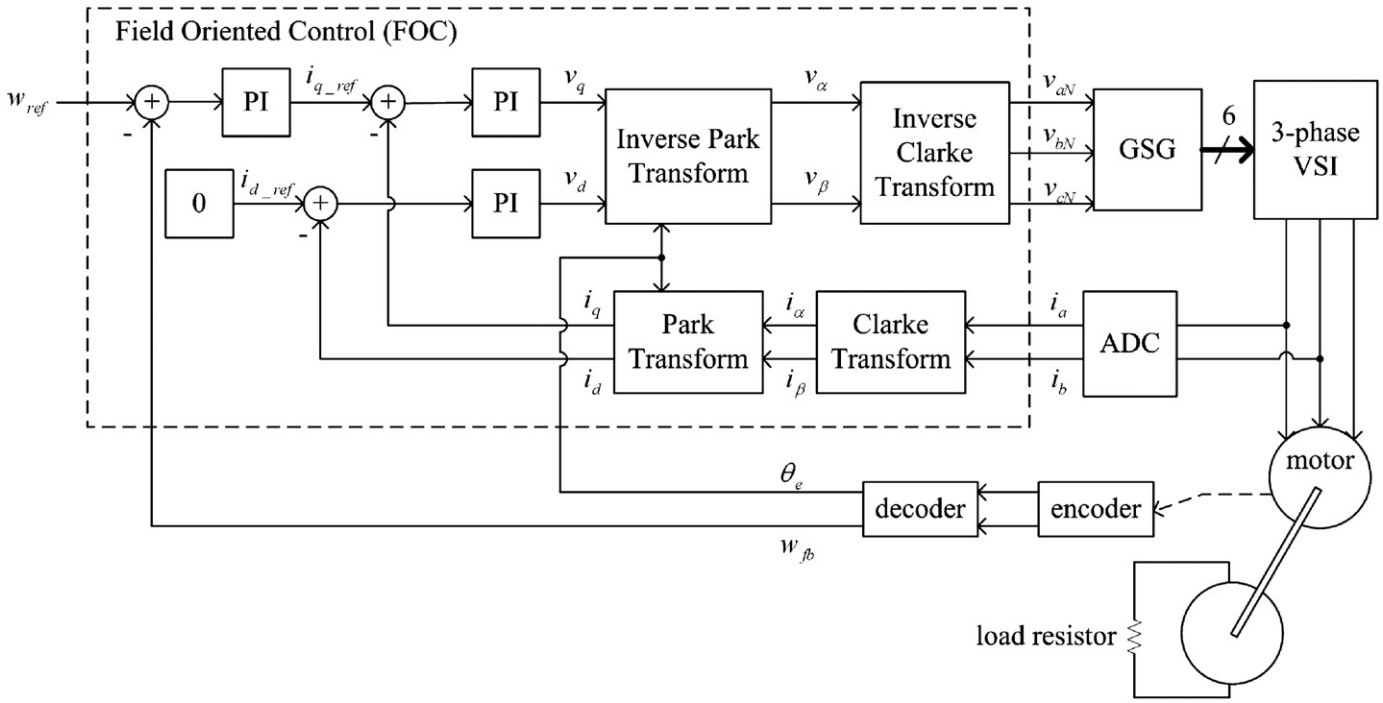

Fig. 1. Architecture of field oriented control (the desired d-axis current is zero for PMSM motor).

multi-dimensional[2] MDFQM for an array of switching elements (Hu and Chen, 2009) and applied the technique to a three-phase voltage source inverter (Hu, Chen, Shen, & Tang, 2011b). For sinusoidal references, it was found out in (Hu et al., 2011b) that the number of switching events is smaller than the corresponding SVPWM scheme at comparable harmonic contents.

This study investigated an FOC using a general gating signal generator considering filtered quantization error. The quantization error was induced by the finite pulse-width resolution within one input period in the implementation. Two extreme cases with infinite/zero bit pulse-width resolution were examined. It is shown that SVPWM is exactly a special case of the proposed gating signal generator with infinite pulse-width resolution. The proposed method is applied to control a permanent magnet synchronous motor (PMSM) under the FOC framework. Both cases (infinite/zero bit pulse-width resolution) are implemented at different load conditions to compare their performance. To show the effect of reduction in switching events, the temperature of the power device is monitored as an index of heat dissipation (power loss). It is concluded that the case with zero bit pulse-width resolution (denoted as multi-dimensional feedback quantization modulator—MDFQM) results in better conversion efficiency without sacrificing control performances.

The rest of this paper is organized as follows. Section 2 introduces the FOC framework, and Section 3 proposes a general gating signal generator that minimizes the power of weighted error. Two extreme cases are discussed, one of which is SVPWM. Section 4 then gives the experimental results for speed ripple, switching number and power MOSFET temperature. Conclusions are finally drawn in Section 5.

2. Field oriented control

Fig. 1 is a block diagram of the field-oriented control system. Three-phase currents produced on the motor windings are transformed into stator reference frame (α–β plane) by Clarke transformation (see (3)). The rotating reference plane ($d-q$ plane) is then obtained by coordinate transformation with respect to the rotor angle (Park transformation, see (1)). The direct component of the stator current, i_d, is used as a control quantity for the rotor flux. Maintaining a constant rotor flux obtains a motor torque that is proportional to the quadrature component i_q. A detailed explanation of the vector oriented analysis of AC machines can be found in Quang and Dittrich (2008).

Two closed loops to control both i_d and i_q are usually implemented (the two inner PI blocks in Fig. 1). For permanent magnet synchronous motor (PMSM), the rotor flux is maintained by the permanent magnets. Therefore, the reference d-axis current i_{d_ref} is set to zero unless field weakening is desired. The reference q-axis current i_{q_ref} is produced from the outer speed control loop. After the real rotor angle θ_e and the motor speed w_{fb} are obtained from the decoder, w_{fb} is compared with desired speed w_{ref} to find i_{q_ref}. In the inner loops, the actual i_d and i_q are compared with i_{d_ref} and i_{q_ref} to find desired v_d and v_q, respectively, which are then transformed into three-phase desired voltage values (v_{aN}, v_{bN} and v_{cN}) by inverse Park transformation and inverse Clarke transformation. The Park transformation and its inverse transformation are shown in (1)–(2) and (3)–(4) the (inverse) Clarke transformation

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad \text{(Park transformation)} \tag{1}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \cos\theta_e & -\sin\theta_e \\ \sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \quad \text{(inverse Park transformation)} \tag{2}$$

where θ_e is the electrical rotation angle

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \quad \text{(Clarke transformation)} \tag{3}$$

[2] MDFQM: Multi-dimensional feedback quantization modulation.

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad \text{(inverse Clarke transformation)} \quad (4)$$

Once the desired three-phase voltages are obtained, the gating signal generator (GSG in Fig. 1) computes the gating signals for three-phase VSI to drive the motor. Conventional approaches to this block include Sinusoidal PWM (SPWM) and space vector PWM (SVPWM). This work proposes a general framework for the gating signal generator. The quantization scheme of GSG determines the gating signal that enhances the efficiency and performance of the generator. The details are discussed in the next section.

3. General switching strategy for three phase systems

3.1. Basic concept

The GSG block input (refer to Fig. 1) is a three-dimensional desired phase voltage vector, $\mathbf{v}_r = \begin{bmatrix} v_{aN} & v_{bN} & v_{cN} \end{bmatrix}^T$ satisfying

$$v_{aN} + v_{bN} + v_{cN} = 0 \quad (5)$$

Therefore, two elements adequately represent the input reference. The GSG block outputs are six gating signals for power transistors in the three-phase voltage source inverter (VSI). Notably, each of the eight gating states corresponds to a phase voltage vector ("basic vector") produced on the motor windings. Assume that the input sampling frequency is f_c and that the system operates at b-bit pulse-width resolution, i.e., the outputs are updated at a rate $2^b \times f_c$ Hz. The average phase voltage produced on the motor windings within one input period is then

$$\overline{\mathbf{v}}(k) = \frac{1}{2^b} \sum_{j=0}^{2^b-1} \mathbf{v}(j) \quad (6)$$

where $\mathbf{v}(j)$, one of the basic vectors, is the corresponding phase voltage vector induced by the jth selected gating state within one input period. Note that the image of $\overline{\mathbf{v}}$ is all possible linear combinations of 2^b basic vectors. For example, Fig. 2 shows the possible value of $\overline{\mathbf{v}}$ when $b=0$, 1 and 4 on α–β plane. When infinite pulse-width resolution is applied, i.e., $b \to \infty$, the image of $\overline{\mathbf{v}}$ includes the entire α–β plane.

The objective of GSG is to decide gating states (or $\mathbf{v}(j)$) that minimize filtered error power. The filtered error is defined as the weighted difference (in frequency domain) between the desired and the actual phase voltage vectors. In the application of motor control, a first order integrator $z/z-1$ (lowpass filter) is selected as the weighting filter for each phase to enhance low-frequency-band performance. This integrator can be expressed in state-space form as

$$\mathbf{x}(k+1) = \mathbf{x}(k) + (\mathbf{v}_r(k) - \overline{\mathbf{v}}(k)) \text{ and } \mathbf{e}(k) = \mathbf{x}(k) + (\mathbf{v}_r(k) - \overline{\mathbf{v}}(k)) \quad (7)$$

where $\mathbf{e}(k) \in R^3$ is the filtered error vector for each phase, and $\mathbf{x}(k) \in R^3$ is a system state vector. The problem then becomes

$$\min_{v(j) \in \text{basic vectors}} |\mathbf{e}(k)|_2^2 = \min_{v(j) \in \text{basic vectors}} |\mathbf{x}(k) + \mathbf{v}_r(k) - \overline{\mathbf{v}}(k)|_2^2 \quad (8)$$

where $\overline{\mathbf{v}}(k) = (1/2^b) \sum_{j=0}^{2^b-1} \mathbf{v}(j)$. The quality function in (8) implies the same concept as SVPWM that the mean output voltage is equal to the reference input when infinite pulse-width resolution is applied (Hu et al., 2011b).

Remark 1. For efficient switching (i.e., to avoid output voltage cancellations) and to prevent excessive switching transitions, SVPWM uses two adjacent basic vectors and two zero state vectors in one input period (Hu et al., 2011b), which yield six switching transitions within each period.

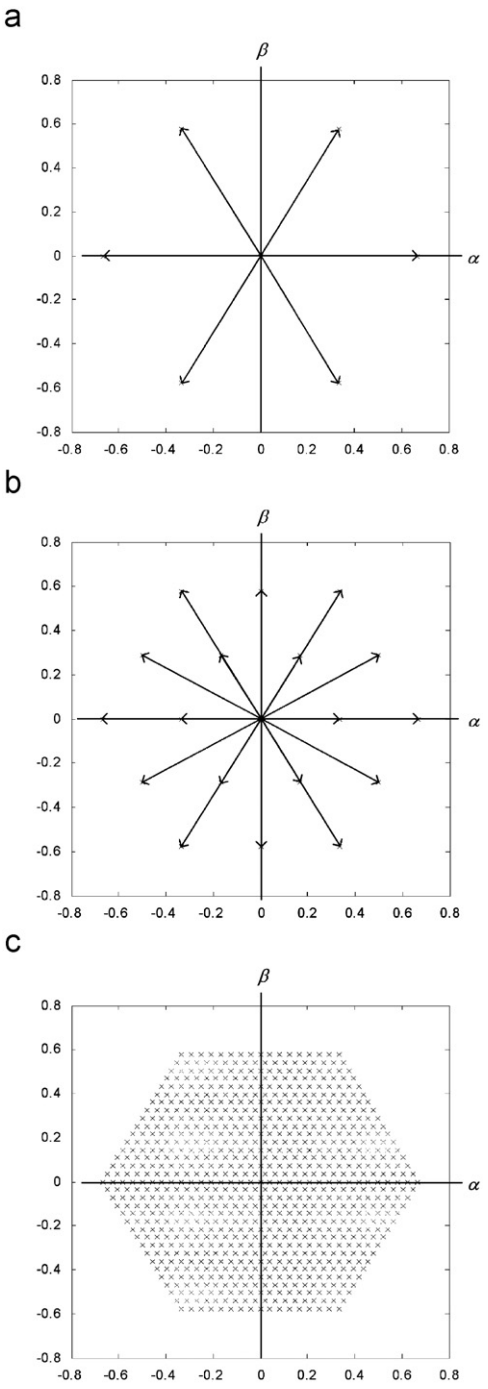

Fig. 2. Image of $\overline{\mathbf{v}}$ for different pulse-width resolution, (a) $b=0$, (b) $b=1$, and (c) $b=4$.

3.2. Noise shaping of GSG

An advantage of GSG is the intrinsic noise shaping effect which is apparent when the input and output relation to (7) is written in the frequency domain

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} = \begin{bmatrix} \frac{z}{z-1} & 0 & 0 \\ 0 & \frac{z}{z-1} & 0 \\ 0 & 0 & \frac{z}{z-1} \end{bmatrix} \begin{bmatrix} V_{aN} - \overline{V}_1 \\ V_{bN} - \overline{V}_2 \\ V_{cN} - \overline{V}_3 \end{bmatrix} \quad (9)$$

where $\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}$, $\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix}$ and $\begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \\ \overline{V}_3 \end{bmatrix}$ are Fourier transforms of elements in $\mathbf{e}(k)$, $\mathbf{v}_r(k)$ and $\overline{\mathbf{v}}(k)$. This three-input three-output system has a diagonal transform matrix, so one channel can be expressed as

$$E_1 = \frac{z}{z-1}(V_{aN} - \overline{V}_1)$$

or equivalently

$$\overline{V}_1 = V_{aN} - \frac{z-1}{z}E_1 \tag{10}$$

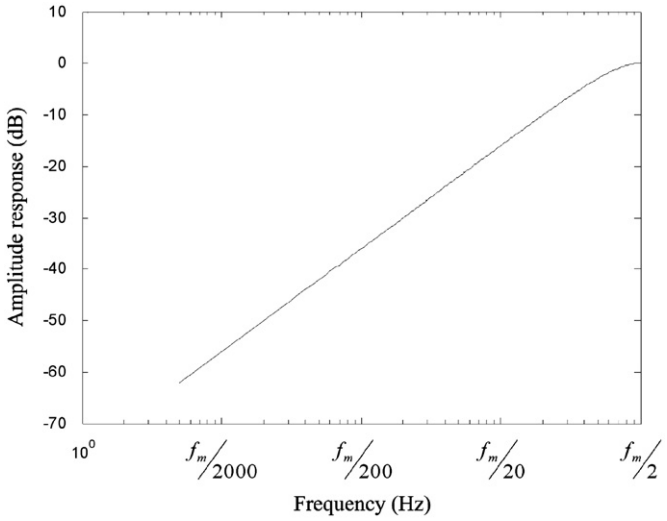

Fig. 3. Frequency response of the difference filter.

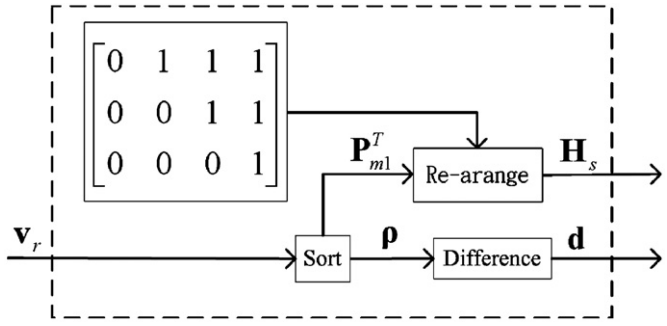

Fig. 4. Implementation block diagram of SVPWM.

The left-hand side of (10) shows the real phase signal (in average sense), which consists of the desired phase signal V_{aN} and a noise term $(z-1/z)E_1$. Notably, the noise term is the accumulated error E_1 filtered by a high-pass filter $(z-1)/z$ (difference filter), i.e., the frequency bands of the noise E_1 are separated from the desired signal V_{aN}.

Fig. 3 plots the frequency response of the difference filter $(z-1)/z$ when GSG is operated at a rate f_m Hz. Noise reduction is at least 40 dB when $(f_m/f_c) > 200$ (where f_c is the sampling frequency of the reference input). This ratio is commonly referred to as the oversampling ratio (OSR). This work considers gating signals produced under two extreme conditions:

Case I. Infinite pulse-width resolution within one input period with OSR=1 (denoted as SVPWM)

Case II. 0-bit pulse-width resolution within one input period with OSR=4 (denoted as MDFQM)

Remark 2. Case I is identical to the SVPWM with carrier frequency f_c Hz, i.e., six switches per input period.

Remark 3. In Case II, $\overline{\mathbf{v}}(k_c)$ (see (2)) is one of the seven basic vectors. The system (3) operates at the rate $f_m = 4f_c$ Hz, and the zero-order-hold is used to up-sample the reference input. Therefore, a maximum of four state transitions can occur within one reference period, and the switching number is lower than that in SVPWM when successive states are adjacent. Notably, since the frequency of the reference signal f_i is usually low, i.e., $f_i \ll 0.5f_c$, OSR=4 is satisfactory. For example, when f_i=100 Hz and f_c= 5 kHz, then $0.5f_c/f_i = 25$. If the oversampling ratio is 4, i.e., $f_m/f_i = 20k/100 = 200$, the MDFQM can achieve a -40 dB noise attenuation for a 100 Hz reference input.

3.3. Solution and implementation

The main task when implementing the system is finding the basic vector(s) (or gating state(s)) that minimize the power of filtered error (refer to (8)). Intuitively, the minimum value of (8) occurs at

$$\overline{\mathbf{v}}(k) = \mathbf{x}(k) + \mathbf{v}_r(k) \tag{11}$$

The following simple method for implementing a VSI drive was proposed in Hu et al. (2011b). Assume that all signals are normalized to 1. To synthesize $\mathbf{x}(k)+\mathbf{v}_r(k)$ by basic vectors within one input period, first define a permutation matrix $\mathbf{P}_{m1} \in R^{3\times 3}$ satisfying $\mathbf{P}_{m1}(\mathbf{x}+\mathbf{v}_r) = \boldsymbol{\rho} = \begin{bmatrix} \rho_1 & \rho_2 & \rho_3 \end{bmatrix}^T$, where $\rho_1 \geq \rho_2 \geq \rho_3$.

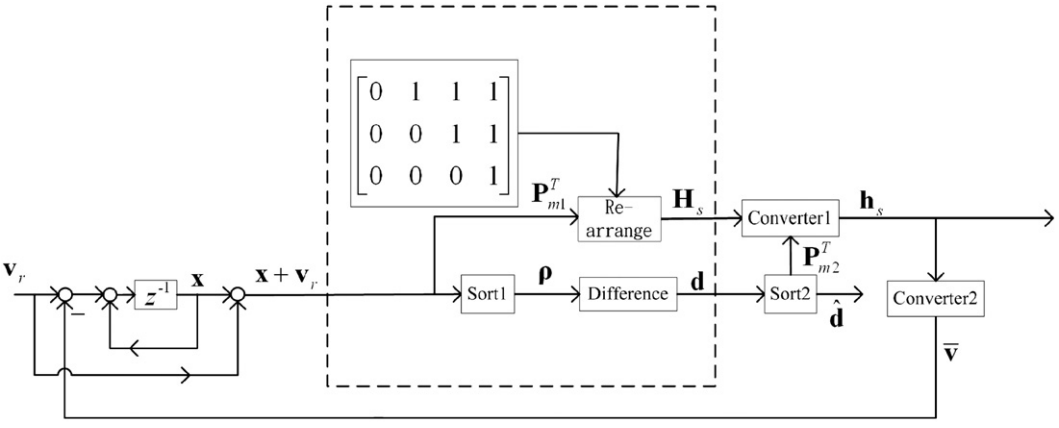

Fig. 5. Implementation block diagram of MDFQM.

The gating signals for inverters are then columns of

$$\mathbf{H}_s = \mathbf{P}_{m1}^T \begin{bmatrix} 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix},$$

and the corresponding duties are

$$\mathbf{d} = \begin{bmatrix} \gamma(1-\rho_1+\rho_3) \\ \rho_1-\rho_2 \\ \rho_2-\rho_3 \\ (1-\gamma)(1-\rho_1+\rho_3) \end{bmatrix}$$

where $\gamma \in [0 \quad 1]$. Note that the first and last columns of $\mathbf{H}_s$ correspond to zero phase voltages, i.e., when $\gamma=0.5$, the system acts as a centered space vector PWM (McGrath, Holmes, & Meynard, 2006). Several modifications are made to adapt the special conditions in Case I and II. In Case I, $\gamma=0.5$ and the pulse-width resolution of the system is infinite, yielding a zero filtered error, i.e., $\mathbf{e}(k)=0$, $\forall k$. Therefore, $\mathbf{x}(k)=0$, $\forall k$, and (11) becomes $\bar{\mathbf{v}}(k)=\mathbf{v}_r(k)$. Therefore, the system contains no feedback signals. Fig. 4 shows the implementation block diagram, in which the "Rearrange" block produces the gating signal $\mathbf{H}_s$ as described above, and the "Difference" block generates the corresponding duty ratios as

$$\mathbf{d} = \begin{bmatrix} 0.5(\rho_1-\rho_3) \\ \rho_2 \\ \rho_3 \\ 0.5(\rho_1-\rho_3) \end{bmatrix}.$$

For Case II with zero bit pulse-width resolution, only one gating state is used. The state that corresponds to maximum duty ratio is selected in order to minimize the power of filtered error, i.e., an additional step is needed to find the maximum element in $\mathbf{d}$. Note that duties for two zero states should be combined into one gating state, i.e., $\gamma=1$. Fig. 5 is a detailed block diagram showing that the "Converter1" performs permutation of column vectors in $\mathbf{H}_s$ and extracts the first column as the gating signals $\mathbf{h}_s$:

$$\mathbf{h}_s = \mathbf{H}_s \mathbf{P}_{m2}^T \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}.$$

The "Sort1" and "Sort2" block satisfy

$$\mathbf{P}_{m1}(\mathbf{x}+\mathbf{v}_r) = \boldsymbol{\rho} = \begin{bmatrix} \rho_1 & \rho_2 & \rho_3 \end{bmatrix}^T, \quad \text{where } \rho_1 \geq \rho_2 \geq \rho_3 \text{ (sort1)}$$

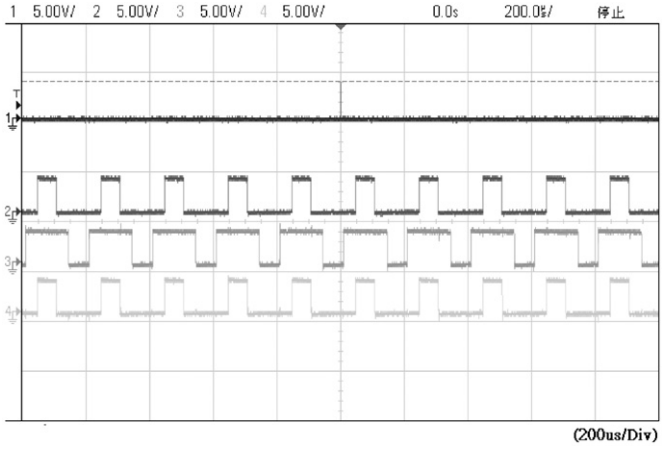

Fig. 6. Gating commends produced by SVPWM, channel 1: trigger signal, channel 2: gating commends for phase a, channel 3: gating commends for phase b, channel 4: gating commends for phase c.

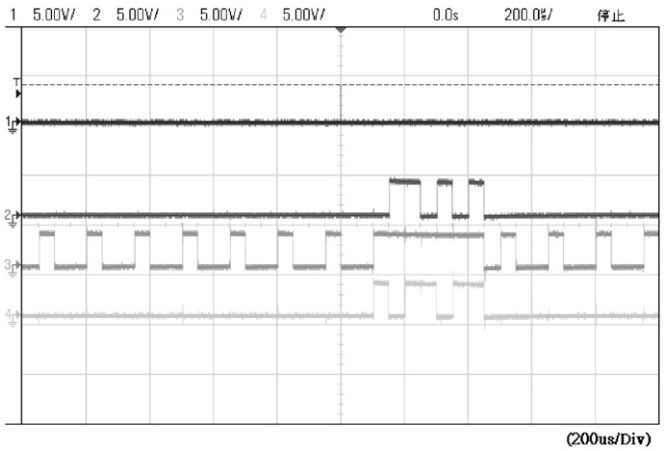

Fig. 7. Gating commends produced by MDFQM, channel 1: trigger signal, channel 2: gating commends for phase a, channel 3: gating commends for phase b, channel 4: gating commends for phase c.

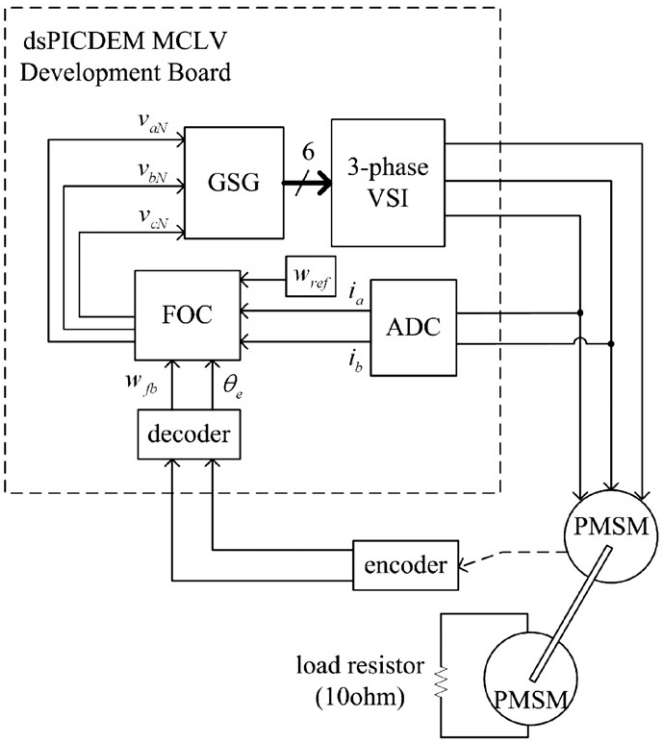

Fig. 8. Block diagram of experimental setup.

Table 1
Detail parameters of the PMSM.

Product	Ho HSING HVP-75
Rated power	750 W
Pole pairs	2
Rated speed	3500 rpm
Resistance	3.05 Ω/2ϕ
Inductance	7.32 mH/2ϕ
Weight	10.9 kg

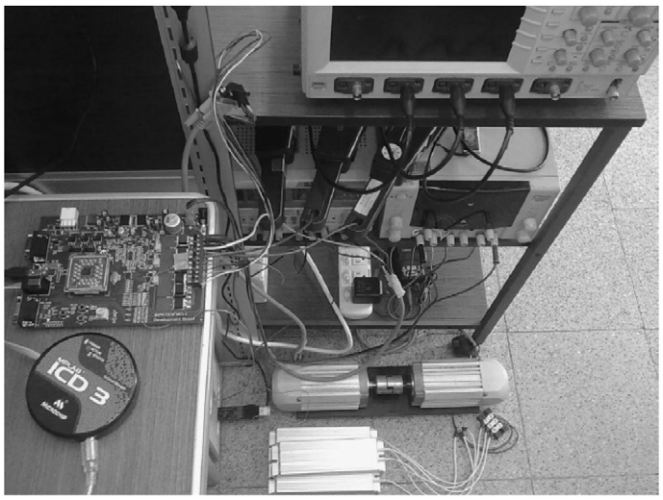

Fig. 9. Experimental platform.

and

$$\mathbf{P}_{m2}\mathbf{d} = \hat{\mathbf{d}} = \begin{bmatrix} \hat{d}_1 & \hat{d}_2 & \hat{d}_3 & \hat{d}_4 \end{bmatrix}^T, \quad \text{where } \hat{d}_1 \geq \hat{d}_2 \geq \hat{d}_3 \geq \hat{d}_4 \text{ (sort2)}$$

Last, to consider the quantization error, the produced phase voltage $\bar{\mathbf{v}}$ is calculated in "Converter2" by multiplying $\mathbf{h}_s$ and

$$\begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix}, \quad \text{i.e., } \bar{\mathbf{v}} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \mathbf{h}_s.$$

Remark 4. To precise explain the gating signals produced by SVPWM and MDFQM, Figs. 6 and 7 show gating signals for upper switches of the three phase legs. The carrier frequency is 5 kHz. Noted that for each phase leg, two state transitions occur within every 1/(5 kHz)=200 us in SVPWM (refer to Fig. 6). Different from SVPWM, MDFQM decides the switching states every 1/(20 kHz)=50 us. Once the switching states are updated

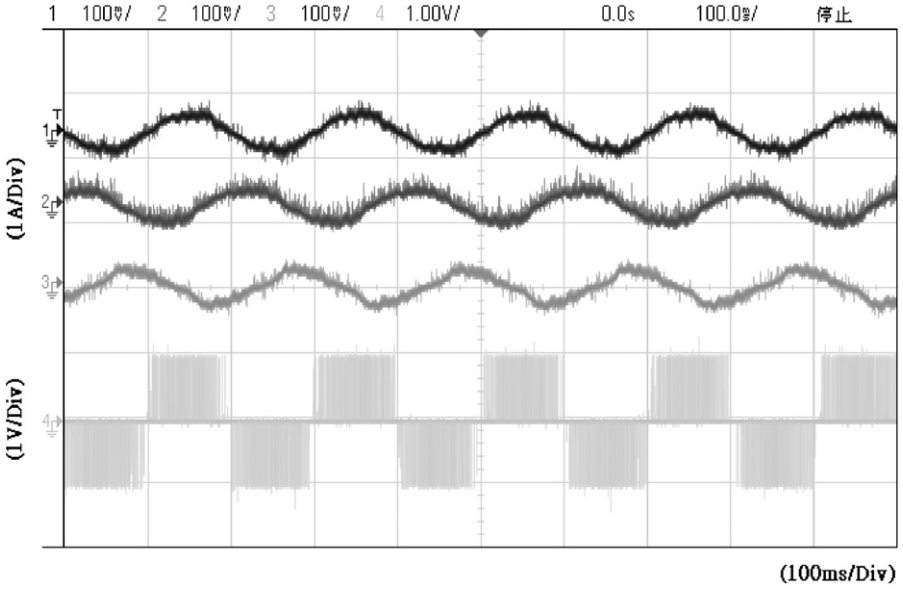

Fig. 10. Steady state response of SVPWM (from top to bottom): three phase currents, line-to-line voltage v_{ab}.

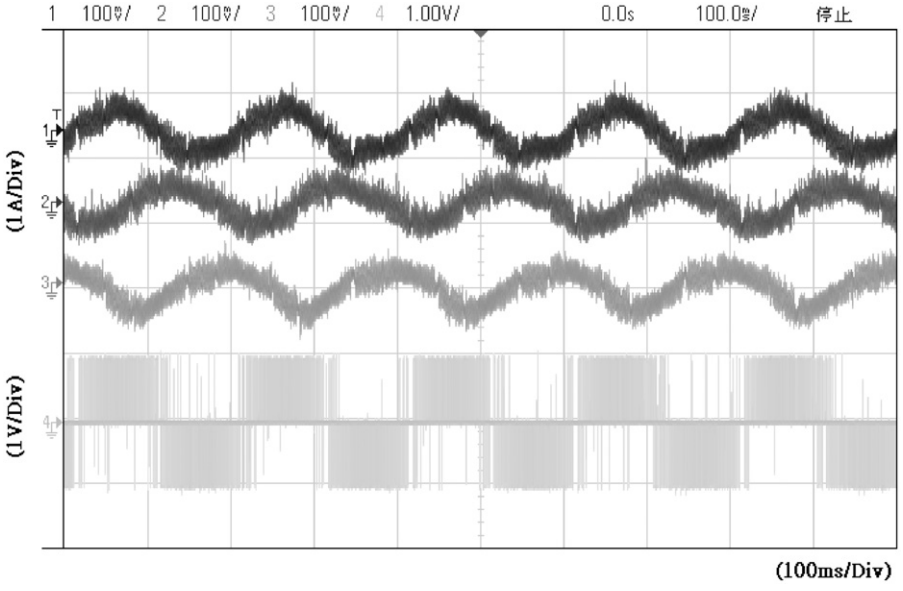

Fig. 11. Steady state response of MDFQM (from top to bottom): three phase currents, line-to-line voltage v_{ab}.

according to the minimum error power, they will hold at the same states until next 50 us. Therefore, the minimum pulse of MDFQM is 50 us (Fig. 7).

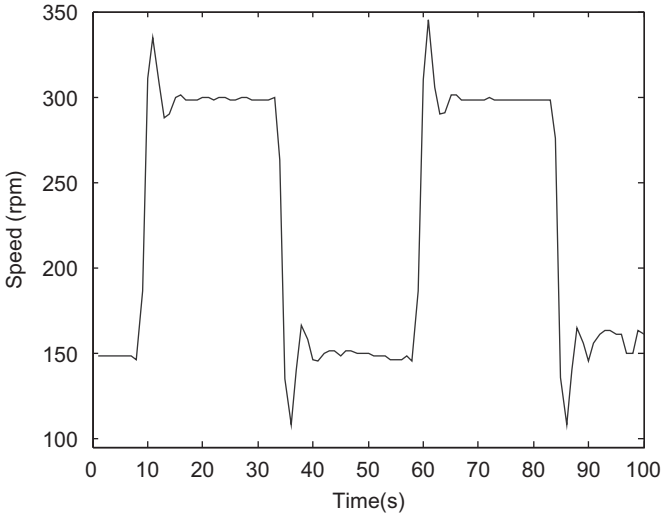

Fig. 12. Dynamic speed response of SVPWM.

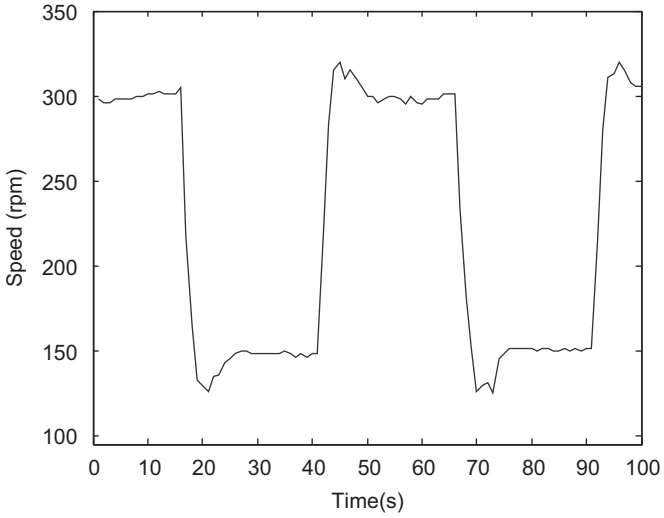

Fig. 13. Dynamic speed response of MDFQM.

4. Experimental results

4.1. Experimental platform

A DSP-based motor control development system was used in the experiments (dsPICDEM MCLV Development Board). Fig. 8 is a block diagram of the experimental setup for controlling a permanent magnetic synchronous motor (PMSM). Another PMSM with three 10 Ω resistances connected was used as a load. Table 1 gives the detailed data for the two motors. The encoder signals from the motor are connected to the DSP board for position/speed calculation and the current sensors feedback the motor currents to the control system. Fig. 9 depicts the platform.

Both SVPWM and MDFQM are used for speed control. Three different carrier frequency f_c=3 kHz, 4 kHz and 5 kHz are used and the dead-time of the gating signals is 2 us. The resulting motor speed, VSI switching number, and MOSFET temperatures are measured for comparison between SVPWM and MDFQM. The mean square error (MSE) of the speed is defined as

$$MSE(u_{ref}) = \frac{1}{n}\sum_{i=1}^{n}(u_{ref}-u_i)^2 \tag{12}$$

where u_{ref} is the reference speed (in rpm) and u_i is the estimated motor speed. A total of n (n=100) samples are taken into consideration.

4.2. Steady state and dynamic responses

The steady state responses of three phase currents, line-to-line voltage are measured as shown in Figs. 10 and 11. The carrier frequency is 5 kHz and a 150 rpm speed commend is applied. For dynamic speed responses, a step up/down speed commend jumping between 150 rpm and 300 rpm is applied. The responses of SVPWM and MDFQM are depicted in Figs. 12 and 13. For a fare comparison, the current/speed controllers used in SVPWM and MDFQM are the same.

Though the ripple of current waveforms is larger using MDFQM than using SVPWM, the speed overshoot and speed ripple of MDFQM is reduced. Noted that the current/speed controllers can also influence the current/speed responses of the system. There must exist an optimized current/speed controller for MDFQM. However with the aim of confirming the feasibility of the novel switching strategy, the optimized design of current/speed controller is not discussed in this work.

4.3. Speed ripple and switching number

To have precise comparison, Table 2 shows the various speeds applied as the reference and the mean square error of both cases.

Table 2
Mean square error of various speed references.

	$\frac{MSE(u_{ref})}{u_{ref}} \times 100(\%)$					
Sampling frequency f_c	3 kHz		4 kHz		5 kHz	
Speed(rpm)	SVPWM (%)	MDFQM (%)	SVPWM (%)	MDFQM (%)	SVPWM (%)	MDFQM (%)
100	5.60	2.05	7.59	1.69	6.80	3.58
150	1.95	1.43	2.26	2.29	3.45	0.93
200	1.83	0.93	1.57	1.46	1.84	1.95
250	1.05	1.17	0.99	1.12	0.92	1.18
300	0.43	0.59	0.68	1.04	0.51	0.88
350	0.80	0.75	0.59	0.80	0.73	0.99
400	0.89	0.89	0.62	0.89	0.74	1.20
450	0.84	0.85	0.78	0.74	0.60	0.73
500	0.82	1.18	0.77	1.02	0.90	1.02

Fig. 14 compares the switching numbers of both cases for different carrier frequencies. The data show that the two cases have comparable speed response. Further, MDFQM switching numbers are reference-dependent, and all are lower than those of SVPWM. Table 3 gives the reduction ratios under different reference speeds and sampling frequencies f_c. The reduction ratio attains 30% when reference speed is 200 rpm and achieves 50% for 150 rpm. At a low speed of 100 rpm, the switching number of

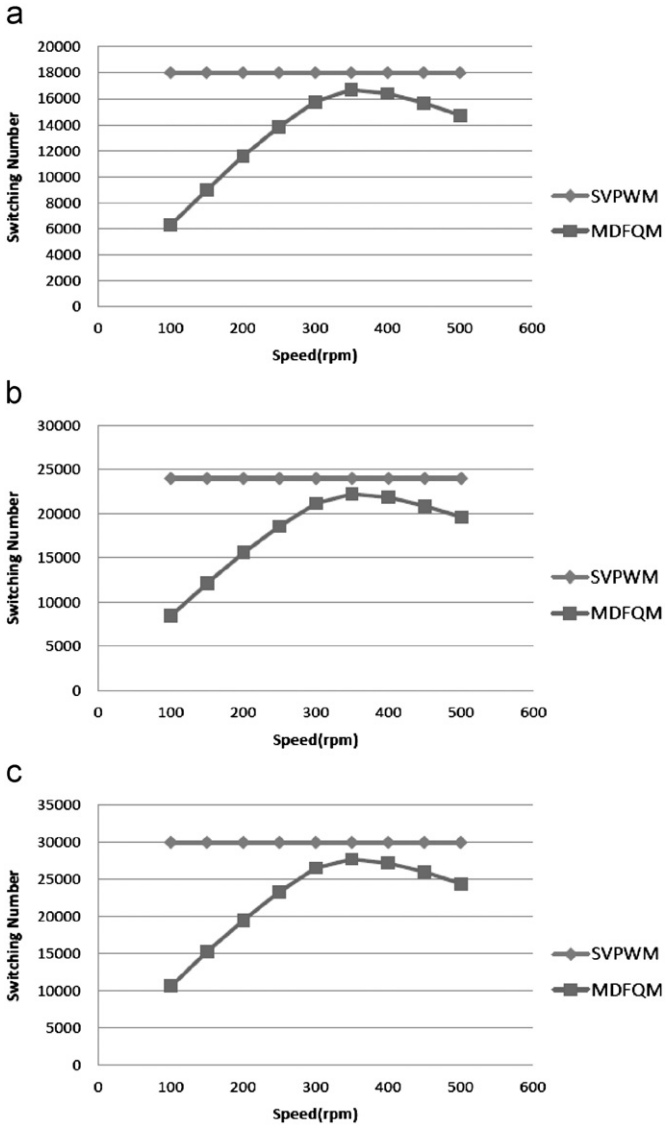

Fig. 14. Switching numbers of both cases, (a) f_c=3 kHz, (b) f_c=4 kHz, and (c) f_c=5 kHz.

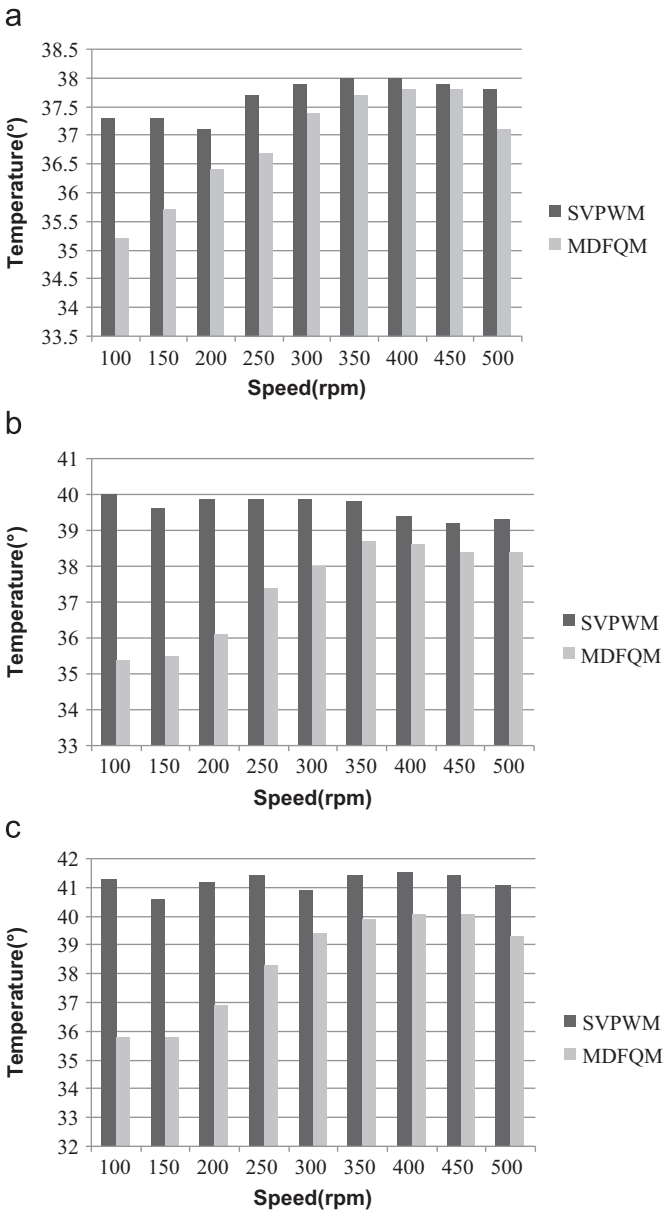

Fig. 15. MOSFET surface temperature, (a) f_c=3 kHz, (b) f_c=4 kHz, and (c) f_c=5 kHz.

Table 3
Switching number comparison for MDFQM and SVPWM.

Sampling frequency f_c	Number of switching per second								
	3 kHz			4 kHz			5 kHz		
Speed (rpm)	SVPWM	MDFQM	Reduction ratio (%)	SVPWM	MDFQM	Reduction ratio (%)	SVPWM	MDFQM	Reduction ratio (%)
100	18,000	6307	65.0	24,000	8481	64.7	30,000	10,667	64.4
150	18,000	8956	50.2	24,000	12,075	49.7	30,000	15,272	49.1
200	18,000	11,588	35.6	24,000	15,570	35.1	30,000	19,555	34.8
250	18,000	13,831	23.2	24,000	18,553	22.7	30,000	23,334	22.2
300	18,000	15,765	12.4	24,000	21,128	12.0	30,000	26,537	11.5
350	18,000	16,668	7.4	24,000	22,230	7.4	30,000	27,776	7.4
400	18,000	16,394	8.9	24,000	21,825	9.1	30,000	27,211	9.3
450	18,000	15,668	13.0	24,000	20,858	13.1	30,000	26,019	13.3
500	18,000	14,725	18.2	24,000	19,598	18.3	30,000	24,422	18.6

MDFQM is about one-third that of SVPWM yielding a superior performance of MDFQM in both speed ripple and the efficiency of switching decision.

4.4. Surface temperature of MOSFET's

Reduced switching number increases the operational lifetime of MOSFETs and reduces power loss. To confirm this, MOSFET surface temperatures were measured at various speeds. Fig. 15 shows the temperature after 15 min of operation. It is seen that, at 400 rpm, temperatures were comparable because switching number was reduced by only 10%. However, at 150 rpm, the temperature differences between both cases are quite significant (about 50% reduction as shown in Table 3).

5. Conclusion

A general gating signal generator considering quantization scheme induced by finite pulse-width resolution is proposed and applied to motor speed control. Two extreme cases were considered: infinite pulse-width resolution with OSR=1 (denoted as SVPWM) and zero bit pulse-width resolution with OSR=4 (denoted as MDFQM). Implementations of the two cases were discussed in detail. The experiments measured steady state currents, speed ripple, switching number and MOSFET temperature. The experiments showed that, compared to SVPWM, MDFQM obtains a greater reduction in switching number. Under a specific speed, the maximum achievable reduction ratio is about 65%, which implies that more than half of the power is reserved when MDFQM is used as the gating signal generator.

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