A Comparative Study of NBTI and RTN Amplitude Distributions in High-κ Gate Dielectric pMOSFETs

J. P. Chiu, Y. T. Chung, Tahui Wang, Min-Cheng Chen, C. Y. Lu, and K. F. Yu

***Abstract*—Random telegraph noise (RTN) and negative bias temperature (NBT) stress-induced threshold voltage (V_t) fluctuations in high-κ gate dielectric and metal-gate pMOSFETs are investigated. We measured RTN amplitude distributions before and after NBT stress. RTN in poststressed devices exhibits a broader amplitude distribution than the prestress one. In addition, we trace a single trapped charge-induced ΔV_t in NBT stress and find that the average ΔV_t is significantly larger than a ΔV_t caused by RTN. A 3-D atomistic simulation is performed to compare a single-charge-induced ΔV_t by RTN and NBTI. In our simulation, the probability distribution of a NBT trapped charge in the channel is calculated from the reaction-diffusion model. Our simulation confirms that the NBT-induced ΔV_t indeed has a larger distribution tail than RTN due to a current-path percolation effect.**

***Index Terms*—Amplitude, negative bias temperature instability (NBTI), random telegraph noise (RTN), simulation.**

I. INTRODUCTION

RANDOM telegraph noise (RTN) and negative bias temperature instability (NBTI) are recognized as two major reliability issues in CMOS scaling [1]–[5]. Single-charge trapping/detrapping-induced threshold voltage fluctuations in RTN and NBTI have been widely explored [3], [4]. Similar phenomenology has been found in both of them. For example, discrete charge trapping/detrapping is observed in RTN and NBTI traces, as shown in Fig. 1. The abrupt changes of a threshold voltage (ΔV_t) in Fig. 1 are realized due to a single-charge trapping/detrapping in a gate dielectric. Previous studies have shown that the magnitude of the ΔV_t varies from a device to a device in RTN measurement and from a trapped charge to a trapped charge during NBT stress [4]. The ΔV_t magnitude distribution can be approximated by an exponential function, i.e., $f(|\Delta V_t|) = \exp(-|\Delta V_t|/\sigma)/\sigma$, either for RTN [6] or for NBTI [4]. A 3-D atomistic Monte Carlo simulation [7], [8] has shown that the ΔV_t distribution tail is attributed to a current-path percolation effect arising from random dopants in substrate. Since RTN traps in unstressed devices and NBT stress created charges may have a different spatial distribution in the channel, their current-path percolation effects and thus the ΔV_t distribution may be different and require a further study.

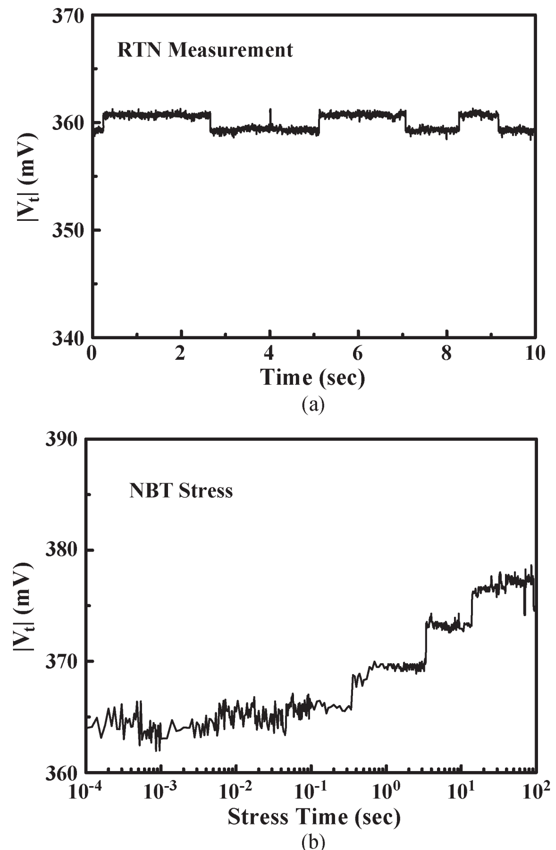

Fig. 1. (a) RTN measured at $V_D = -0.05$ V and a target I_D of -500 nA. The V_t waveform is obtained from the measured drain current divided by a transconductance. (b) Threshold voltage trace in NBT stress. The stress condition is $|V_g - V_t| = 1.5$ V, and the measurement condition is the same as RTN measurement.

In this letter, we characterize RTN and NBTI in high-$\kappa(HfO_2)$ gate dielectric and metal gate pMOSFETs. The devices have a drawn gate length of 30 nm and a gate width of 80 nm. A 3-D Monte Carlo simulation is performed to calculate RTN and NBTI caused ΔV_t distributions due to a percolation effect. In NBTI simulation, the reaction-diffusion (R-D) model [9] is employed to calculate a trap creation probability distribution in the channel.

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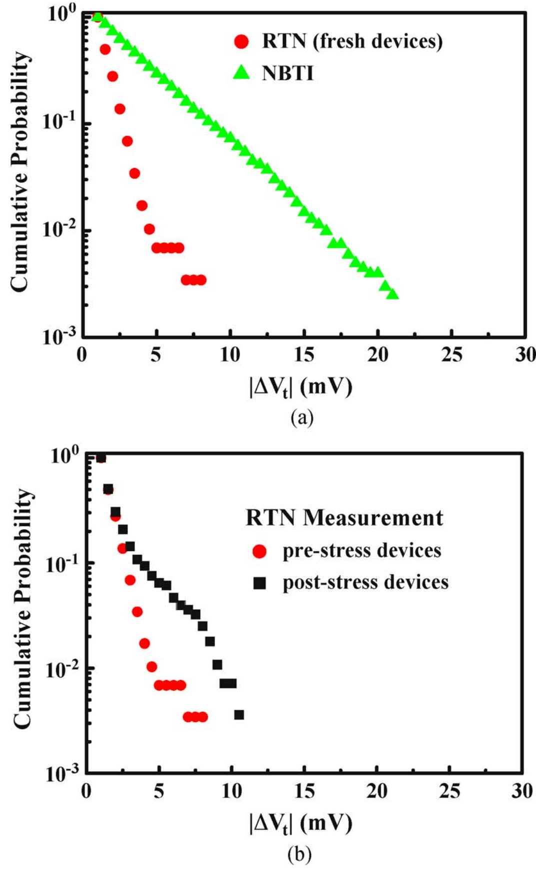

Fig. 2. (a) Complementary cumulative probability distribution of a single trapped charge-induced ΔV_t in RTN versus NBTI. RTN is measured in fresh devices. (b) Complementary cumulative probability distributions of a single-charge-induced ΔV_t for RTN in fresh devices and in post-NBT stress devices. The minimum detectable ΔV_t is about 1 mV.

II. Measurement Results and Discussion

In RTN measurement, the drain voltage is −0.05 V, and the gate voltage is adjusted to have a target drain current of −500 nA. A typical RTN waveform is shown in Fig. 1(a). The threshold voltage fluctuations are obtained from a measured drain current divided by a transconductance. Two-level switching due to a single-charge trapping/detrapping is observed. In NBTI characterization, the stress condition is $|V_g - V_t| =$ 1.5 V and $V_D = 0$ V at room temperature. Threshold voltage variations with stress time are also traced in the same condition as RTN measurement with a switch delay time less than 1 μs using Agilent B1500. A representative NBTI trace is shown in Fig. 1(b). Each sudden V_t jump is due to creation of a single trapped charge. We collect all the single-charge-induced ΔV_t in about 300 samples. The complementary cumulative probability distribution of ΔV_t amplitude is shown in Fig. 2. In Fig. 2(a), we compare RTN and NBTI amplitude distributions. The RTN distribution is measured in fresh devices. The NBTI has a considerably broader amplitude distribution ($\sigma = 3.34$ mV) than RTN ($\sigma = 1.12$ mV), suggesting that NBTI has a larger impact on CMOS reliability than RTN due to a larger ΔV_t tail. Moreover, we compare RTN amplitude distributions in pre-NBT stress devices and in post-NBT stress devices in Fig. 2(b). The poststress one apparently has a larger ΔV_t tail. As a result, we conclude that NBT stress created traps have a larger single-charge-induced ΔV_t distribution tail.

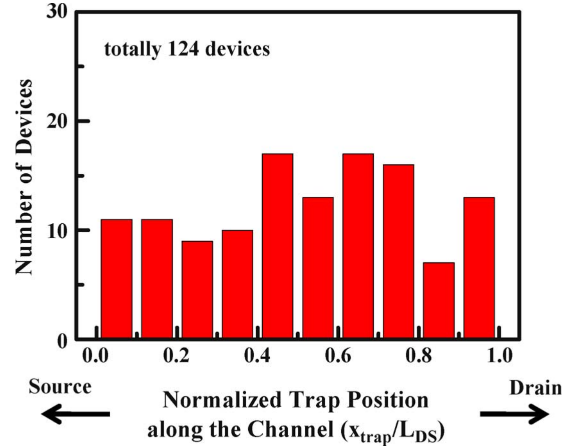

Fig. 3. RTN trap position distribution along the channel extracted from 124 devices. x_{trap} is the distance of a trap from the source, and L_{DS} denotes a channel length.

III. Simulation of a NBT Stress-Induced ΔV_t

To explore the physics that a NBT stress created charge has a larger ΔV_t distribution tail, we performed a 3-D atomistic Monte Carlo simulation for both RTN and NBTI. In RTN amplitude simulation, substrate dopants are randomly and discretely placed in a simulated device, and an RTN trap is randomly selected in the channel. The random placement of an RTN trap is based on an assumption that RTN traps in fresh devices (for example, process-induced traps) have a uniform distribution in the channel. This assumption is actually verified by measurement. In Fig. 3, we extract an RTN trap lateral position in 124 devices by using a method similar to [10], [11] and the trap position distribution is rather uniform along the channel.

In NBTI simulation, to select a trapped charge position, we first calculate a trap creation probability at each grid point in the surface of the channel. According to the R-D model and assuming that the reaction phase dominates the process, the NBT trap generation rate, in the initial stage of stress (i.e., the trap density N_t is small), can be expressed by

$$\frac{dN_t}{dt} = k_F N_0 \tag{1}$$

where N_0 is the total number of Si-H bonds. k_F is the Si-H dissociation rate constant, which is formulated as [12]

$$k_F \propto p \cdot \exp\left(\frac{E}{E_o}\right) \tag{2}$$

where p is a channel surface hole concentration, and E is a local electric field. The local hole concentration p and the electric field E are obtained from a 3-D device simulation with random substrate dopants. Thus, the relative trap creation probability at each point of the channel can be calculated from the product of p and $\exp(E/E_0)$. Fig. 4 shows the calculated trap creation probability versus a local surface hole concentration in

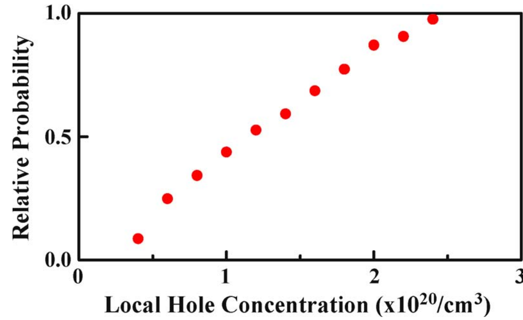

Fig. 4. Relative NBT trap creation probability versus a local surface hole concentration. A local hole concentration and a surface electric field are calculated from a 3-D device simulation with random and discrete substrate dopants. In the calculation, E_0 in (2) is about 1.1 MV/cm.

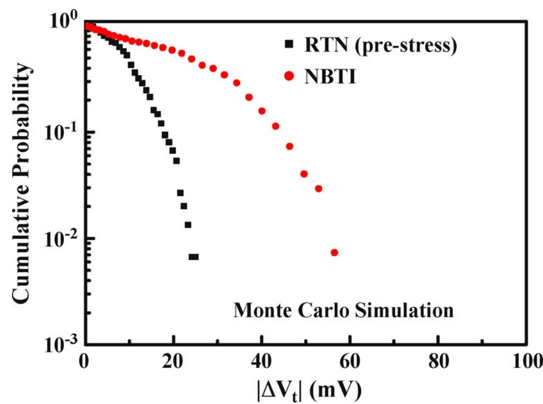

Fig. 5. Complementary cumulative probability distributions of RTN and NBTI amplitudes from 3-D atomistic simulation. The simulated devices have a gate length of 30 nm and a gate width of 30 nm.

NBT stress. The result shows that the trap creation probability increases with a hole concentration. In other words, a trap tends to be created in a high hole density region (i.e., a critical current path) in NBT stress. In our NBTI amplitude simulation, we select a trapped hole position according to the calculated probability distribution rather than a uniform probability distribution for RTN. 200 simulations are performed for each distribution curve in Fig. 5. It should be mentioned that the simulated device size is $W/L = 30\ \mathrm{nm}/30\ \mathrm{nm}$ rather than a measured device size of $W/L = 80\ \mathrm{nm}/30\ \mathrm{nm}$. The reason is that the simulation time is about 2 hours for a $W/L = 30\ \mathrm{nm}/30\ \mathrm{nm}$ device, but is about 3 days for a $W/L = 80\ \mathrm{nm}/30\ \mathrm{nm}$ device. The entire probability distribution consists of more than 200 devices. Thus, the total simulation time becomes prohibitive for a real device size. In addition, it is not our intention to directly fit the simulation to the measurement result because we do not know an exact doping profile in measured devices. Instead, our purpose is to show, by simulation, that the ΔV_t distributions from traps created according to the R-D model and from traps induced by process, which are believed to have a random distribution in the channel, have different amplitudes and σ. This result is expected to be the same regardless of a device size.

The simulated RTN and NBTI amplitude distributions are compared in Fig. 5. Our simulation confirms that the NBTI has a larger ΔV_t tail. The reason is that a NBT charge tends to be created in a critical path and a trapped charge in a critical current path has a larger influence on a channel current, thus resulting in a larger ΔV_t due to a percolation effect. The difference in the shape of the distribution in measurement (Fig. 2) and in simulation (Fig. 5) is believed due to a different device size. A device size effect on the shape of the distribution can be found in [8]. A similar argument can be applied to poststress RTN in Fig. 2(b). In poststressed devices, there exist two kinds of RTN traps, process-induced traps (initial traps) and stress-created traps. The initial traps have a tight ΔV_t distribution, while the stress created traps have a broader one. The overall distribution in poststress devices therefore has a larger distribution tail.

IV. Conclusion

Single trapped charge-induced ΔV_t distributions in RTN and NBTI are characterized and simulated in pMOSFETs. Our simulation method takes into account a trap creation probability in NBT stress. Our study shows that a NBT stress created charge has a larger ΔV_t distribution tail than prestress RTN. This large NBT tail poses to be a serious CMOS reliability concern and should be carefully considered in a precise NBTI lifetime model.

References

[1] N. Tega, H. Miki, Z. Ren, C. P. D'Emic, Y. Zhu, D. J. Frank, J. Cai, M. A. Guillorn, D.-G. Park, W. Haensch, and K. Torii, "Reduction of random telegraph noise in high-κ/metal-gate stacks for 22 nm generation FETs," in *IEDM Tech. Dig.*, 2009, pp. 771–774.

[2] M. Tanizawa, S. Ohbayashi, T. Okagaki, K. Sonoda, E. Eikyu, Y. Hirano, K. Ishikawa, O. Tsuchiya, and Y. Inoue, "Application of a statistical compact model for random telegraph noise to scaled-SRAM $V_{\min}$ analysis," in *VLSI Symp. Tech. Dig.*, 2010, pp. 95–96.

[3] C.-T. Chan, C.-J. Tang, T. Wang, H. C.-H. Wang, and D. D. Tang, "Characteristics and physical mechanisms of positive bias and temperature stress-induced drain current degradation in HfSiON nMOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 6, pp. 1340–1346, Jun. 2006.

[4] B. Kaczer, T. Grasser, P. J. Rousse, J. Franco, R. Degraeve, L.-A. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger, "Origin of NBTI variability in deeply scaled pFETs," in *Proc. IRPS*, 2010, pp. 26–32.

[5] T. Grasser, H. Reisinger, W. Goes, T. Aichinger, P. Hehenberger, P.-J. Wagner, M. Nelhiebel, J. Franco, and B. Kaczer, "Switching oxide traps as the missing link between negative bias temperature instability and random telegraph noise," in *IEDM Tech. Dig.*, 2009, pp. 1–4.

[6] K. Fukuda, Y. Shimizu, K. Amemiya, M. Kamoshida, and C. Hu, "Random telegraph noise in flash memories: Model and technology scaling," in *IEDM Tech. Dig.*, 2007, pp. 169–172.

[7] A. Asenov, R. Balasubramaniam, A. R. Brown, and J. H. Davies, "RTS amplitudes in decananometer MOSFETs: 3-D simulation study," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 839–845, Mar. 2003.

[8] M. Compagnoni, A. Mauri, S. M. Amoroso, A. Maconi, E. Greco, A. S. Spinelli, and A. L. Lacaita, "Comprehensive investigation of statistical effects in nitride memories—Part II: Scaling analysis and impact on device performance," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2124–2131, Sep. 2010.

[9] M. A. Alam and A. Krishnan, "NBTI: Process, device and circuit," in *Proc. IRPS*, 2005, p. 212, Tutorial.

[10] S. Lee, H.-J. Cho, Y. Son, D. S. Lee, and H. Shin, "Characterization of oxide traps leading to RTN in high-κ and metal gate MOSFETs," in *IEDM Tech. Dig.*, 2009, pp. 1–4.

[11] H.-C. Ma, Y.-L. Chou, J.-P. Chiu, Y.-T. Chung, T.-Y. Lin, T. Wang, Y.-P. Chao, K.-C. Chen, and C.-Y. Lu, "A novel random telegraph signal method to study program/erase charge lateral spread and retention loss in a SONOS flash memory," *IEEE Trans. Electron Devices*, vol. 58, no. 3, pp. 623–630, Mar. 2011.

[12] M. A. Alam and S. Mahapatra, "A comprehensive model of PMOS NBTI degradation," *Microelectron. Reliab.*, vol. 45, no. 1, pp. 71–81, Jan. 2005.