Band-to-Band-Tunneling Leakage Suppression for Ultra-Thin-Body GeOI MOSFETs Using Transistor Stacking

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***Abstract*—This letter indicates that the ultra-thin-body (UTB) germanium-on-insulator (GeOI) MOSFETs preserve the leakage reduction property of stacking devices, while the band-to-band-tunneling leakage of bulk Ge-channel devices cannot be reduced by stacking transistors. The seemingly contradictory behavior of the stack-effect factors is explained by the difference in the flows of band-to-band-tunneling hole fluxes for UTB GeOI and bulk Ge-channel devices and validated by TCAD mixed-mode simulations. At 300 K, the stack-effect factors of UTB GeOI MOSFETs range from 6.8 to 40 ($N = 2$) and from 12 to 142 ($N = 3$) at $Vdd = 0.5{-}1$ V. As the temperature increases or Vdd decreases, the stack-effect factor for UTB GeOI devices decreases, while the stack-effect factor for bulk Ge-channel MOSFETs increases, because the subthreshold leakage current becomes more significant at higher temperature or lower voltage with respect to the band-to-band-tunneling leakage current.**

***Index Terms*—Band-to-band-tunneling leakage, germanium, germanium-on-insulator (GeOI), stacking effect, ultra-thin-body (UTB).**

I. Introduction

GERMANIUM has been proposed as an alternative channel material to enhance mobility and current drive [1], [2]. With technology scaling, the OFF-state leakage current increases drastically, and leakage power has become a major contributor to the total power. Bulk Ge-channel devices with high permittivity and low bandgap suffer from short-channel effects (SCEs) and severe band-to-band-tunneling leakage current. Moreover, for bulk Ge-channel devices, the higher substrate doping density and the employment of the "halo" profiles (used to reduce SCEs) result in significantly larger band-to-band-tunneling current through the reverse-biased drain–substrate and source–substrate junctions. Ultra-thin-body (UTB) germanium-on-insulator (GeOI) MOSFET has been proposed as a promising device architecture [3]–[6] due to its better control of SCEs compared with the bulk Ge-channel MOSFET.

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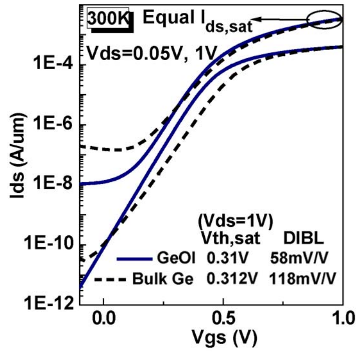
Transistor stacking has been widely known and used for subthreshold leakage reduction in bulk CMOS circuits [7], [8]. In serially connected (stacked) OFF transistors, the intermediate node will be charged by the leakage through the top transistor to a higher-than-ground potential; thus, the gate-to-source voltage of the top transistor becomes negative [12]. In addition, the threshold voltage of the top transistor increases due to the reverse-biased body-to-source voltage since its body is connected to ground and its source is at the intermediate node potential [12]. As a result, the subthreshold leakage of a stack of OFF transistors is significantly less than that of a single device. However, the stacking effect of a Ge-channel device is different since its leakage current is dominated by the band-to-band-tunneling leakage at normal operating voltage (> 0.8 V) and room temperature. In this letter, the effectiveness of stacking to reduce the band-to-band-tunneling-dominated leakage currents in UTB GeOI MOSFETs and bulk Ge-channel MOSFETs is compared and analyzed.

II. Device Design and TCAD Simulation Methodology

In this work, the UTB GeOI and bulk Ge-channel devices are designed with 25-nm gate length (Lg). Fig. 1(a) shows the Ids–Vgs characteristics of UTB GeOI and bulk Ge-channel MOSFETs at $Vds = 0.05$ and 1.0 V. The device parameters are listed in Fig. 1(b), and the schematics of a UTB GeOI MOSFET with thin buried oxide (BOX) and raised source/drain structure and its bulk Ge-channel counterpart are shown in Fig. 1(c). Gate direct-tunneling leakage is ignored in this study due to the use of high-k gate dielectric. As can be seen, with equal drive current at 1.0 V, the bulk Ge-channel device has higher $Ioff$ than the UTB GeOI MOSFET. The UTB GeOI devices/circuits are analyzed using TCAD mixed-mode simulations [9]. The band-to-band-tunneling model proposed by Schenk [10] is used and calibrated with the experimental data [6] to accurately describe the band-to-band-tunneling leakage current.

III. Stacking Effect Comparison Between GeOI and Bulk Ge-Channel Devices

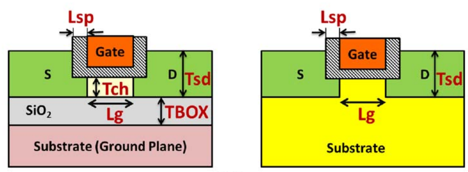
Fig. 2 shows the stack-effect factors for UTB GeOI and bulk Ge-channel devices. As two or more OFF devices are stacked,



(a)

MOSFETs	GeOI	Bulk Ge
Lg (nm)	25	25
EOT (nm)	0.7	0.7
Gate dielectric	permittivity=22	
Nch (cm^{-3})	1E16	3E18
Tch (nm)	5	--
TBOX (nm)	10	--
Lsp(nm)	10	10
Tsd (nm)	22.5	22.5
Nsd(cm^{-3})	5.5E19	5.5E19
Work function (eV)	4.38	4.42

(b)



(c)

Fig. 1. (a) Ids–Vgs characteristics at $Vds = 0.05$ and 1 V for bulk Ge-channel and UTB GeOI devices. The bulk Ge-channel and GeOI devices are designed with equal drive current at $Vgs = Vds = 1$ V. (b) UTB GeOI and bulk Ge-channel device parameters. (c) Schematics of a UTB GeOI MOSFET with thin BOX structure and raised source/drain and a bulk Ge-channel MOSFET with raised source/drain investigated in this work.

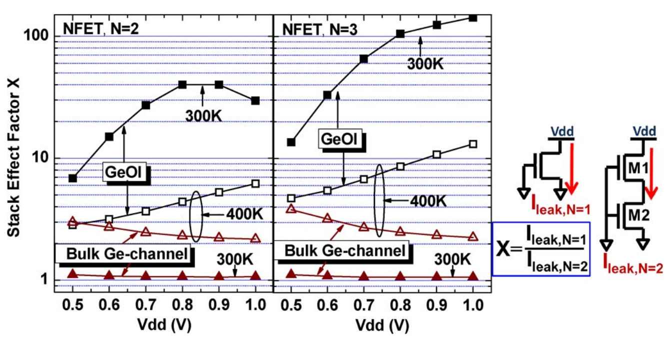
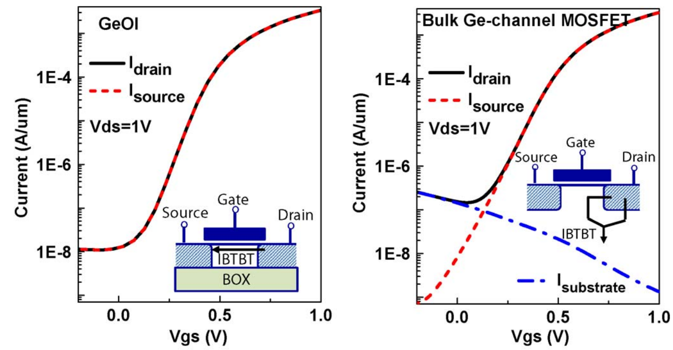


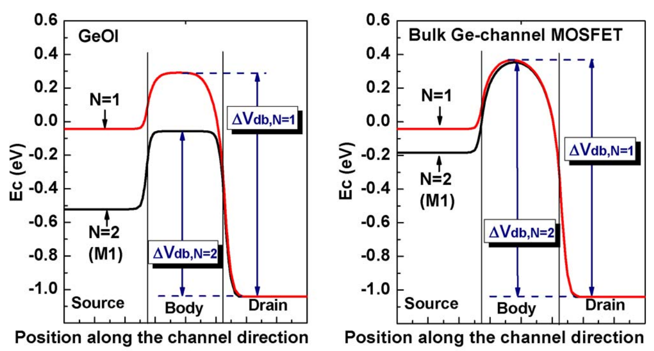
Fig. 2. Stack-effect factors for UTB GeOI and bulk Ge-channel MOSFETs with $N = 2$ and $N = 3$. N is the number of stacked devices. The UTB GeOI devices show much larger stack-effect factor than the bulk Ge-channel devices at 300 K.

the leakage is reduced from that of a single device by a factor X (stack-effect factor) [11]. At 300 K, the leakage currents for both UTB GeOI and bulk Ge-channel MOSFETs are dominated by band-to-band-tunneling leakage currents, and the UTB GeOI stacked devices show 6 to 37 times (two OFF stacked devices, $N = 2$) and 12 to 133 times $(N = 3)$ larger stack-effect factors than the bulk Ge-channel counterparts. At 300 K, the stack-effect factor of bulk Ge-channel stacked devices is almost equal to one, which means that the band-to-band-tunneling leakage of bulk Ge-channel devices cannot be suppressed by stacking transistors. As the temperature rises from 300 K to 400 K or Vdd decreases, the stack-effect factor for UTB GeOI stacked devices decreases, while the stack-effect factor for bulk Ge-channel stacked devices increases. This is because, as the temperature increases or Vdd decreases, the subthreshold leakage current becomes more significant while the relative contribution of the band-to-band-tunneling leakage current decreases due to its stronger voltage dependence and weaker temperature dependence for both UTB GeOI and bulk Ge-channel MOSFETs. For bulk Ge-channel devices, the subthreshold leakage current can be reduced by transistor stacking; therefore, the stack-effect factor of bulk Ge-channel stacked devices increases as the temperature increases and Vdd decreases. On the other hand, UTB GeOI stacked devices show smaller stack-effect factor at high temperature and low Vdd because the subthreshold leakage of GeOI devices becomes more significant while the band-to-band-tunneling leakage is reduced.



(a) (b)

Fig. 3. (a) Drain current (I_{drain}) and source current (I_{source}) for the UTB GeOI MOSFET at $Vds = 1$ V and 300 K. (b) I_{drain}, I_{source}, and substrate current $(I_{\mathrm{substrate}})$ for the bulk Ge-channel MOSFET at $Vds = 1$ V and 300 K. As band-to-band tunneling occurs at $Vgs = 0$ V, I_{drain} equals I_{source} for the UTB GeOI MOSFET, while $I_{\mathrm{substrate}}$ equals I_{drain} for the bulk Ge-channel MOSFET.



(a) (b)

Fig. 4. Energy band diagrams for the (a) UTB GeOI MOSFET and (b) bulk Ge-channel MOSFET with $N = 1$ and $N = 2$ at 300 K and $Vdd = 1$ V. (M1: Top transistor of the stacked devices.)

The seemingly contradictory behavior of the stack-effect factors for UTB GeOI and bulk Ge-channel devices is explained as follows. As band-to-band tunneling occurs across the drain–body junction in the UTB GeOI NMOS, a hole flux flows into the body region and reaches the source side. The hole flux reduces the drain–body potential difference, thus reducing the band-to-band-tunneling current. For bulk Ge-channel NMOS, the hole flux flows into the substrate contact, and the band-to-band-tunneling current cannot be suppressed by stacking bulk Ge-channel transistors. Fig. 3 shows that, as band-to-band tunneling occurs across the drain–body junction at $Vgs =$ 0 V, the band-to-band-tunneling current of the UTB GeOI MOSFET flows into the body and reaches the source side, and the drain current (I_{drain}) equals the source current (I_{source}). On the other hand, for the bulk Ge-channel MOSFET, the

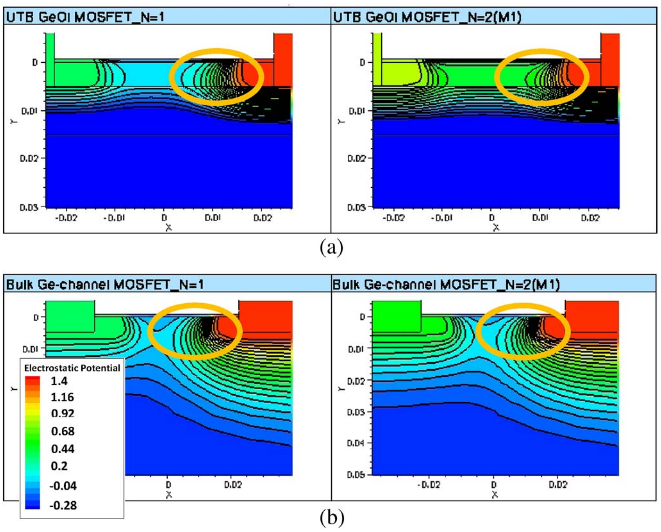


Fig. 5. Potential contours for the (a) UTB GeOI MOSFET and (b) bulk Ge-channel MOSFET with $N = 1$ and $N = 2$. Each line in the body region is an equipotential line at 300 K and $Vdd = 1$ V. (M1: Top transistor of the stacked devices.)

band-to-band-tunneling current flows into the substrate contact, and $I_{\rm drain}$ equals the substrate current $(I_{\rm substrate})$. Fig. 4 shows the energy band diagrams for UTB GeOI and bulk Ge-channel devices with $N = 1$ and $N = 2$ along the channel for the top transistor (M1) of the stacked devices. As can be seen, for the UTB GeOI MOSFET, the drain-to-body potential drop can be effectively reduced by transistor stacking ($N = 2$ device), whereas for the bulk Ge-channel MOSFET, the drain-to-body potential drops are comparable for the $N = 1$ and $N = 2$ cases. Fig. 5 shows the equipotential contours for $N = 1$ and $N = 2$ UTB GeOI [Fig. 5(a)] and bulk Ge-channel [Fig. 5(b)] devices, respectively. The equipotential lines are always perpendicular to the electric field, and the band-to-band tunneling strongly depends on the electric field. As can be seen, for the UTB GeOI device, the drain-to-body potential drop (electric field) is reduced by stacking transistors $(N = 2)$ compared with the $N = 1$ GeOI device, while for bulk Ge-channel MOSFETs, the drain-to-body potential drops (electric field) are comparable for the $N = 1$ and $N = 2$ devices.

The transistor-stacking technique has been proven quite effective in lowering the standby (subthreshold) leakage of a circuit [13], [14]. Our results show that, for any device structure with an isolated body, the band-to-band-tunneling leakage current can be reduced by transistor stacking due to the raised body potential.

IV. Conclusion

The band-to-band-tunneling leakage currents of UTB GeOI MOSFETs can be reduced by transistor stacking, while the band-to-band-tunneling leakage currents of bulk Ge-channel MOSFETs cannot be suppressed by transistor stacking. The UTB GeOI stacked devices show 6 to 37 times $(N = 2)$ and 12 to 133 times $(N = 3)$ larger stack-effect factors than the bulk Ge-channel counterparts at 300 K. As the temperature increases or Vdd decreases, the stack-effect factor for UTB GeOI stacked devices decreases, while the stack-effect factor for bulk Ge-channel stacked devices increases, because the subthreshold leakage current becomes more significant at higher temperature or lower voltage with respect to the band-to-band-tunneling leakage current.

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References

[1] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. A. Pianetta, S.-P. Wong, and K. C. Saraswat, "Experimental demonstration of high mobility Ge NMOS," in *IEDM Tech. Dig.*, 2009, pp. 453–456.
[2] T. Yamamoto, Y. Yamashita, M. Harada, N. Taoka, K. Ikeda, K. Suzuki, O. Kiso, N. Sugiyama, and S. Takagi, "High performance 60 nm gate length germanium p-MOSFETs with Ni germanide metal source/drain," in *IEDM Tech. Dig.*, 2007, pp. 1041–1043.
[3] E. Batail, S. Monfray, C. Tabone, O. Kermarrec, J. F. Damlencourt, P. Gautier, G. Rabille, C. Arvet, N. Loubet, Y. Campidelli, J. M. Hartmann, A. Pouydebasque, V. Delaye, C. Le Royer, G. Ghibaudo, T. Skotnicki, and S. Deleonibus, "Localized ultra-thin GeOI: An innovative approach to germanium channel MOSFETs on bulk Si substrates," in *IEDM Tech. Dig.*, 2008, pp. 397–400.
[4] C. Royer, A. Pouydebasque, K. Romanjek, V. Barral, M. Vinet, J. Hartmann, E. Augendre, H. Grampeix, L. Lachal, C. Tabone, B. Previtali, R. Truche, and F. Alain, "Sub-100 nm high-K metal gate GeOI pMOSFETs performance: Impact of the Ge channel orientation and of the source injection velocity," in *Symp. VLSI Technol.*, 2009, pp. 145–146.
[5] V. P.-H. Hu, Y.-S. Wu, and P. Su, "Investigation of electrostatic integrity for ultra-thin-body GeOI MOSFET using analytical solution of Poisson's equation," *Semicond. Sci. Technol.*, vol. 24, no. 4, p. 045017-1, Apr. 2009.
[6] L. Hutin, C. Royer, J. Damlencourt, J. Hartmann, H. Grampeix, V. Mazzocchi, C. Tabone, B. Previtali, A. Pouydebasque, M. Vinet, and O. Faynot, "GeOI pMOSFETs scaled down to 30-nm gate length with record OFF-state current," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 234–236, Mar. 2010.
[7] Z. Chen, M. Johnson, L. Wei, and K. Roy, "Estimation of standby leakage power in CMOS circuits considering accurate modeling of transistor stacks," in *Proc. Int. Symp. Low Power Electron. Des.*, 1998, pp. 239–244.
[8] W. Jiang, V. Tiwari, E. D. L. Iglesia, and A. Sinha, "Topological analysis for leakage prediction of digital circuits," in *Proc. Asia South Pacific Des. Autom. Conf. Int. Conf. VLSI Des.*, 2002, pp. 39–44.
[9] Sentaurus TCAD, C2009-06 Manual.
[10] A. Schenk, "Rigorous theory and simplified model of the band-to-band tunneling in silicon," *Solid State Electron.*, vol. 36, no. 1, pp. 19–34, Jan. 1993.
[11] S. Narendra, V. De, S. Borkar, D. Antoniadis, and A. Chandrakasan, "Full-chip subthreshold leakage power prediction and reduction techniques for sub 0.18 um CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 501–510, Mar. 2004.
[12] S. Mukhopadhyay, C. Neau, R. T. Cakici, A. Agarwal, C. H. Kim, and K. Roy, "Gate leakage reduction for scaled devices using transistor stacking," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 4, pp. 716–730, Aug. 2003.
[13] V. De, Y. Ye, A. Keshavarzi, S. Narendra, J. Kao, D. Somasekhar, R. Nair, S. Borkar, A. Chandrakasan, W. Bowhill, and F. Fox, "Techniques for leakage power reduction," in *Design of High-Performance Microprocessor Circuits*. Piscataway, NJ: IEEE Press, 2001, pp. 46–61.
[14] Y. Ye, S. Borkar, and V. De, "New technique for standby leakage reduction in high-performance circuits," in *VLSI Symp. Tech. Dig.*, 1998, pp. 40–41.