High-Performance Poly-Si Thin-Film Transistors With L-Fin Channels

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***Abstract*—For the first time, we construct poly-Si thin-film transistors (TFTs) with novel L-shaped poly-Si fin channels (poly-Si TFTs with L-fin channels, called LFin-TFTs). The L-fin channels of LFin-TFTs are similar to the multiple-gated fin channels of FinFETs. The LFin-TFTs exhibit a low supply gate voltage (3 V), a good subthreshold swing (SS) ∼190 mV/dec, and a high on/off current ratio $(I_{ON}/I_{OFF}) > 10^6$ $(V_D = 1\ V)$ without hydrogen-related plasma treatments. After Ni salicidation, the devices exhibit steep SS ∼ 148 mV/dec and $I_{ON}/I_{OFF} \sim 10^7$. After NH_3 plasma treatment, the characteristics of the devices are further improved. The LFin-TFTs have steeper SS ∼ 132 mV/dec, higher $I_{ON}/I_{OFF} > 10^7$, and threshold voltage $(V_{TH}) \sim$ 0.036 V.**

***Index Terms*—FinFETs, L-fin, multiple gate, NH_3 plasma, Ni salicidation, poly-Si thin-film transistors (TFTs).**

I. Introduction

Better gate electrostatic control of the channel potential in nonplanar device structures has been a research goal for more than a decade [1]–[4]. To this end, multiple-gated metal–oxide–semiconductor field-effect transistor architectures such as FinFETs are expected to be used beyond the 22-nm technology node due to their excellent short-channel effect (SCE) immunity [5]. From a transistor variation and mismatch perspective, FinFETs are considered particularly suitable for further static random access memory (SRAM) scaling, owing to their improved SCE behavior and lower channel doping concentration [6]. Compared to conventional planar transistors, FinFETs with double gates are a promising architecture [7] for further scaling. Recently, high-performance low-temperature poly-Si thin-film transistors (TFTs) have been developed for the employment of active-matrix liquid crystal displays on a glass substrate and for driving integrated circuits (ICs) for the applications of system-on-panel (SOP) and the 3-D IC elements such as SRAM and dynamic random access memory [8]–[10].

Furthermore, high-speed display driving circuits require TFTs to operate at low voltages and high driving currents, with a low threshold voltage (V_{TH}). In this letter, we demonstrate poly-Si TFTs with novel L-fin channels (LFin-TFTs) without the use of advanced lithographic tools. High-performance LFin-TFTs with low V_{TH}, good subthreshold swing (SS), and high on/off current ratio (I_{ON}/I_{OFF}) can be obtained. These hold great promise for the realization of SOP and 3-D IC.

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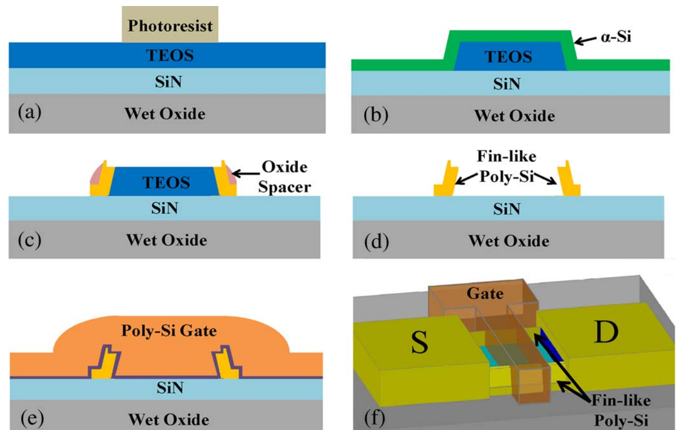

Fig. 1. (a)–(e) Key process flows of the LFin-TFTs and (f) 3-D schematic structure of the LFin-TFTs.

II. Experiment

The key process steps are shown in Fig. 1. The LFin-TFTs were built on Si wafers capped with a 500-nm thermal oxide layer. Si_3N_4 (150 nm)/tetraethoxysilane (TEOS) (150 nm) dummy structures were then deposited by low-pressure chemical vapor deposition (LPCVD) [Fig. 1(a)]. The TEOS was patterned and overetched to the Si_3N_4 in the dry etching step, and a 45-nm-thick amorphous Si (a-Si) layer was deposited by LPCVD at 500 °C [Fig. 1(b)]. Next, the a-Si layer was crystallized by solid-phase crystallization at 600 °C for 24 h in a N_2 ambient. After TEOS spacer was formed, the S/D region patterns were then defined by an I-line stepper. The S/D and the poly-Si L-fin channels were fabricated by anisotropic selective dry etching [Fig. 1(c)], and the TEOS dummy layer and spacer were removed using dilute HF solution [Fig. 1(d)]. The TEOS dummy layer and spacer protected the sidewalls of the L-fin channel during dry etching. A 10-nm-thick LPCVD TEOS oxide layer and an *in situ* doped n^+ poly-Si gate with a thickness of 250 nm were then deposited [Fig. 1(e)]. After gate patterning by dry etching step, the n^+ S/D regions were implanted with arsenic (As^+; 25 keV at 5×10^{15} cm^{-2}) and activated at 600 °C in a N_2 ambient. Fig. 1(f) shows the 3-D schematic structure of the LFin-TFTs. For comparison, the LFin-TFTs with Ni salicidation (called LFin-Ni) were achieved by rapid thermal annealing at 450 °C for 30 s, and

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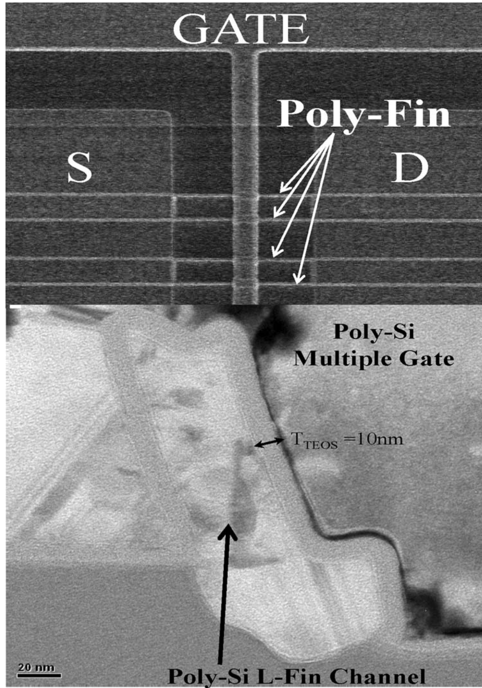

Fig. 2. SEM and cross-sectional TEM images of gate-stacked L-fin channels.

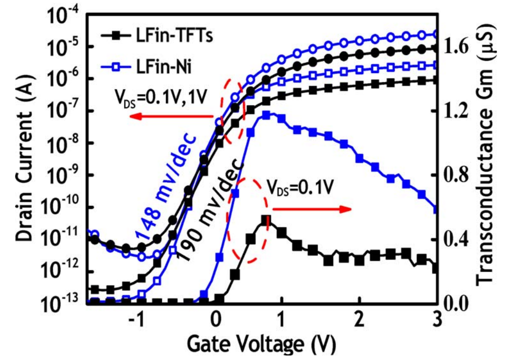

Fig. 3. Transfer characteristics of LFin-TFTs and LFin-Ni. The well-behaved transfer characteristics of the LFin-Ni are due to the reduction in S/D parasitic resistance.

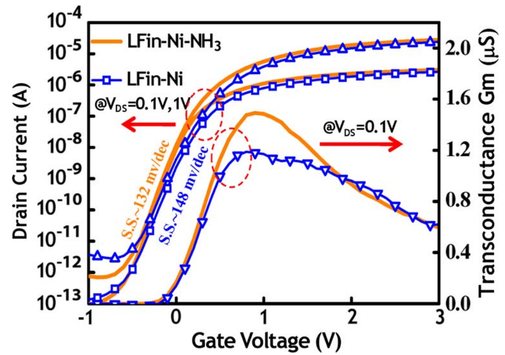

Fig. 4. Transfer characteristics of LFin-Ni-NH_3 and LFin-Ni. The well-behaved transfer characteristics for the LFin-Ni-NH_3 are illustrated.

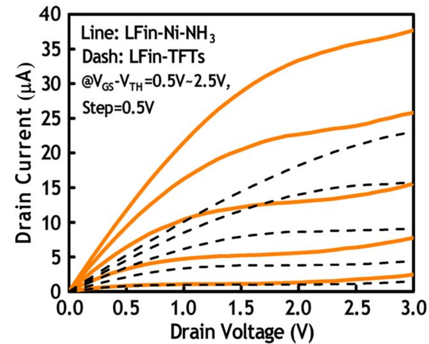

Fig. 5. Output characteristics of LFin-Ni-NH_3 and LFin-TFTs. The LFin-Ni-NH_3 devices exhibit higher driving currents.

the same devices with further NH_3 plasma treatments (called LFin-Ni-NH_3) were also constructed.

III. Result and Discussion

The scanning electron microscope (SEM) and cross-sectional transmission electron microscope (TEM) images of gate-stacked L-fin channels are shown in Fig. 2. The L-fin channels are surrounded by TEOS gate oxide and poly-Si gate resulting in multiple-gated LFin-TFTs. The height and thickness of the L-fin channels are about 200 and 45 nm, respectively. In this work, we measured the electric characteristics of LFin-TFTs with a channel length of 0.35 μm ($N_{\mathrm{Fin}} = 2$; effective channel width $\sim 0.3 \times 2 = 0.6$ μm). We fabricated the TEOS spacer as small as possible to approach the ideal fin. When the height of L-fin is great enough, the spacer variation can be improved by a smaller spacer size. The 3-D L-fin channels were fabricated without use of advanced lithographic tools by simple and low-cost processes. Fig. 3 shows the transfer characteristics of LFin-TFTs and LFin-Ni. The LFin-TFTs without hydrogen-related plasma treatments exhibit low $V_{\mathrm{TH}} \sim 0.26$ V and good SS $\sim$ 190 mV/dec due to the multiple-gated structure. On the other hand, the ON-state currents and transconductance (Gm) of LFin-Ni are higher than those of LFin-TFTs due to the reduction in S/D parasitic resistance [11], while the SS of the LFin-Ni is steeper. Furthermore, the small drain-induced barrier lowering (DIBL) of LFin-Ni during device operation can be attributed to the multiple-gated L-fin channel structure, which offers good gate controllability.

Fig. 4 shows the transfer characteristics of LFin-Ni-NH_3 and LFin-Ni. The characteristics of LFin-Ni-NH_3 are further improved by NH_3 plasma treatment, including SS, $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ($I_{\mathrm{OFF}} < 10^{-12}$ at $V_D = 1$ V), and DIBL. Those improvements can be attributed to the hydrogen passivation of the defect states, the nitrogen pileup at SiO_2/poly-Si interface, and the strong Si–N bond formation that terminates the dangling bonds in the grains and at the grain boundaries in the poly-Si channels [12]. The LFin-TFTs have a multiple-gated L-fin channel structure similar to single-crystal FinFETs, but additional hydrogen-related plasma treatments are required to improve the characteristics of the 45-nm-thick poly-Si L-fin channel. Nevertheless, the hydrogen-related plasma treatments are unnecessary in our previous work with sub-10-nm Si nanowire (NW) channel [13]. The characteristics of nanoscaled NW devices with different plasma treatment times are identical. We argue that the thickness and size of the poly-Si channels are the key points for future nanoscaled poly-Si TFTs.

TABLE I
COMPARISON OF IMPORTANT PARAMETERS OF THE L-FIN DEVICES IN THIS RESEARCH WITH HIGH-PERFORMANCE TFTS INVESTIGATED IN OTHER RESEARCH STUDIES

	LFin	LFin-Ni	LFin-Ni-NH_3
V_{TH} (V)	~0.26	0.16	0.036
S.S. (mV/dec)	190	148	132
I_{ON}/I_{OFF} (V_{DD}=1V)	>10^6	8.6x10^6	>10^7
DIBL (mV/V)	99	47	20

	This Work	[14]	[15]	[16]	[17]
Structure	Fin-like	High-k MG	Nanowire	Nanowire	DSSB
Channel	SPC	SPC	SLS	SPC	SPC
Gate Stack	Poly-Si / SiO_2	TaN / $HfSiO_X$	Poly-Si/ SiO_2	Poly-Si / SiO_2	Poly-Si / HfO_2
W/L (μm/μm)	0.6/0.35	150/0.3	0.13/1	0.035/0.03	0.02/0.09
V_{TH} (V)	0.036	0.75	0.6~0.76	0.97	1.162
EOT (nm)	10	2.8	25	25	T_{HfO2} =20
S.S. (mV/dec)	132	193	209	224	113
DIBL (mV/V)	20	80	20	895	254
I_{ON}/I_{OFF} (V_{DD})	>10^7 (1V)	>10^6 (1V)	~10^8 (3.5V)	>10^7 (1V)	>10^7 (1V)

The output characteristics of LFin-Ni-NH_3 and LFin-TFTs are compared in Fig. 5. After Ni salicidation and NH_3 plasma treatment, the improvement of saturation currents ($\sim$ 37.7 μA) over the LFin-TFTs ($\sim$ 23 μA) is about 63% at $V_G - V_{\mathrm{TH}} =$ 2.5 V and $V_D = 3$ V. The LFin-Ni-NH_3 devices exhibit higher driving currents than the LFin-TFTs due to their extra Ni-salicidation and NH_3 plasma treatment processes. In addition, we show the extracted parameters of the LFin-TFTs, LFin-Ni, and LFin-Ni-NH_3 at the top part of Table I. We also present a comparison of several important parameters of the LFin-Ni-NH_3 with high-performance TFTs investigated in other research studies [14]–[17] at the bottom part of Table I. Compared to planar TFTs with high-κ gate dielectric, as shown in Table I [14], [17], the LFin-Ni-NH_3 devices show a lower V_{TH}, a lower SS, and improved DIBL with thicker equivalent oxide thickness. The highly improved performances of the LFin-Ni-NH_3 can be attributed to the employment of a double-gate structure which provides higher gate controllability. Compared to the TFTs with a NW structure [15], [16], the LFin-Ni-NH_3devices have good SS and comparable DIBL, using a simpler process.

IV. CONCLUSION

High-performance poly-Si TFTs with novel L-fin channel structure have been constructed and investigated in this research. Compared with FinFETs, the LFin-TFT processes are simpler and have lower cost. The S/D parasitic resistance can be reduced by the Ni salicidation. Additional NH_3 plasma treatment was adopted to effectively passivate the defects and interface states in LFin-TFTs. The well-behaved electric characteristics (low off-leakage currents, good SS, improved DIBL, and high $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$) simultaneously achieved in the LFin-TFTs are the result of the multiple-gated L-fin channel structure. These high-performance LFin-TFTs appear to be promising for future applications in SOP and 3-D IC.

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