Impacts of the Underlying Insulating Layers on the MILC Growth Length and Electrical Characteristics

Chia-Chun Liao, Min-Chen Lin, Shao-Xuan Liu, and Tien-Sheng Chao

***Abstract*—This letter investigates the impacts of proximity layers on metal-induced lateral crystallization (MILC). The underlying insulating layers not only affect the MILC growth length but also influence the electrical characteristics. Based on the comparison among the underlying insulating layers, SiN is unsuitable to be an underlying insulating layer because of concerns regarding the crystallization condition. This letter proposes three reasonable mechanisms, including the gettering of Ni, intrinsic stress, and the involvement of hydrogen to enhance the understanding of the impacts of proximity layers.**

***Index Terms*—Metal-induced lateral crystallization (MILC), strain, thin-film transistors (TFTs).**

I. Introduction

METAL-INDUCED lateral crystallization (MILC) has been studied as a lower temperature alternative to solid-phase crystallization (SPC) of amorphous silicon or amorphous SiGe because of its high-quality poly-Si layer with higher carrier mobility, larger grain size, and lower defect density [1].

Although MILC has been a subject of numerous studies, its detailed mechanism still provokes many questions, including metal sources, temperature, and dopant species [1], [2]. Wong *et al.* reported that the underlying insulating materials influence the MILC growth length [3], [4]. Although this study proposed a reasonable mechanism (Ni gettering occurs at the interface between a-Si and the buffered layer), Wong *et al.* found that this mechanism does not suffice to bridge the MILC growth length with the dopant species involved, implying the involvement of another mechanism [4].

In contrast, FinFETs, nanowires, and double-gated TFTs have drawn considerable attention for a number of applications [5]–[7]. With the advantage of these structures, MILC poly-Si can achieve enhanced performance. Basically, the fabrication flow of these novel structures requires SiN, thermally grown oxide, or TEOS oxide to serve as the proximity layer, such as the hard mask, the underlying insulating layer, or the spacer before MILC [5]–[8]. Thus, clarifying the influences of these proximity layers on crystallization in addition to the advantages of the structures of poly-Si TFTs becomes critical.

This letter presents three commonly used layers for clarifying the effects of proximity layers on MILC length and electrical characteristics of p-channel TFTs. To avoid other mechanisms involved in carrier transportation (e.g., different mechanisms of scattering and charge trapping based on different gate oxides or spacers) that are not the scope of this letter, only different underlying insulating layers are studied for clarifying the influence of the proximity layer.

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II. Experimental Procedure

Fabrication of the underlying insulating layers (proximity layers) was started by capping a 500-nm-thick thermal oxide layer or the TEOS oxide layer on 6-in silicon wafers. A number of wafers with thermal oxides, namely, inserted SiN, were deposited as 150-nm SiN by low-pressure chemical vapor deposition (LPCVD) as a stacked double layer for investigating the impact of the SiN proximity layer. Then, a 50-nm-thick a-Si thin film was deposited by LPCVD on all wafers. A 5-nm-thick Ni thin film was selectively deposited using an electron gun evaporator on an a-Si film using the lift-off process. The wafers were heat treated at 550 °C in a N_2 ambient for 24 h to laterally crystallize the channel region where the nickel thin film was not deposited. All unreacted Ni was subsequently removed in a H_2SO_4 solution. A 500-nm-thick plasma-enhanced chemical vapor deposition (PECVD) oxide was deposited at 300 °C for device isolation. The oxide was then patterned and etched to define the active region of the device. The source and drain regions were implanted with BF_2 (15 keV at 5×10^{15} cm^{-2}) and activated at 600 °C for 24-h annealing in a N_2 ambient. A 30-nm-thick oxide was deposited at 300 °C by PECVD as the gate oxide. After patterning of contact holes, aluminum was deposited by PVD and patterned as the probe pads to complete the TFT devices.

The devices were annealed at 350 °C for 1 h. Other than postannealing, no other hydrogenation process was performed for investigating the intrinsic behavior of the devices.

III. Results and Discussion

Ni-induced MIC of a-Si occurs through a three-step process: silicide formation, breakup of the silicide layer into small nodules, and transport of the silicide nodules through the a-Si film. At the edge of a Ni-covered region, a certain number of the breakaway $NiSi_2$ nodules move laterally into the a-Si region not originally covered by Ni. As the nodules move laterally,

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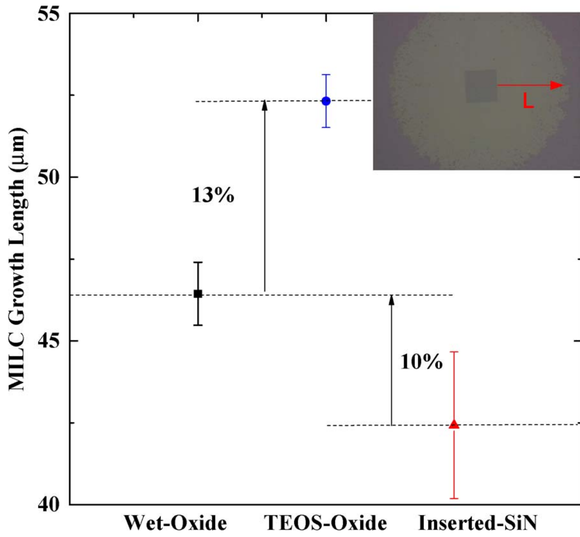

Fig. 1. Dependence of MILC growth length on proximity layers.

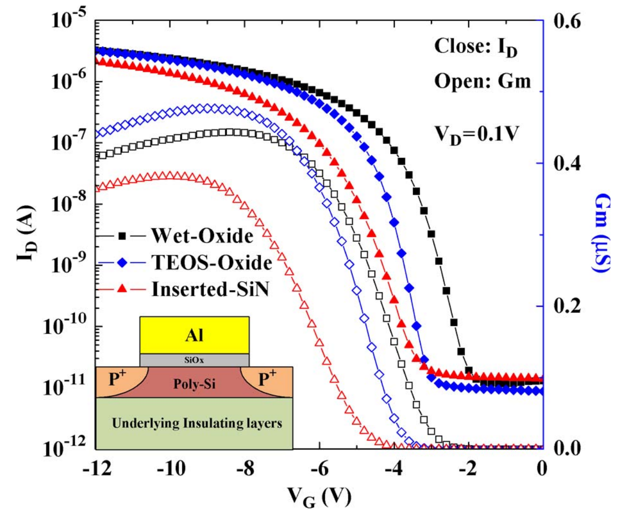

Fig. 2 Transfer characteristics I_D–V_G of p-channel TFTs with different underlying insulating layers.

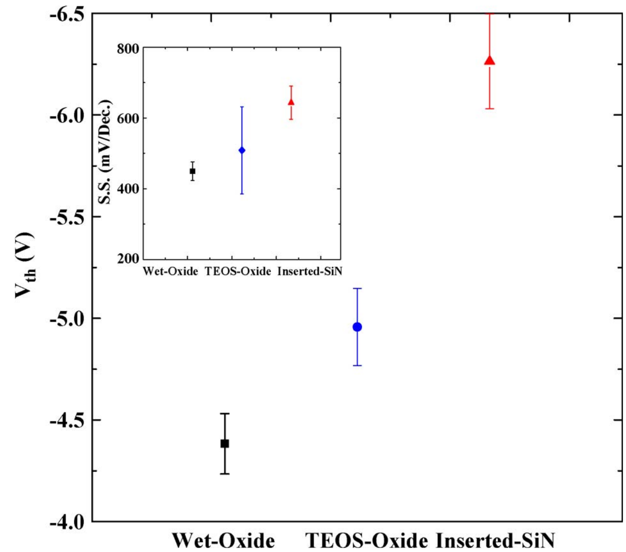

Fig. 3. Variation of threshold voltage as a function of channel width for $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$. The inset shows the variation of subthreshold swing as a function of channel width for $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$.

any a-Si along the path of the moving nodules is crystallized during the MILC process [9]. According to this theory, the growth model of MILC does not reveal the dependence of MILC growth length on the proximity layer.

Fig. 1 shows the relation between MILC growth length and different underlying insulating layers. The region crystallized by MILC was identified with optical microscopy, as shown in the inset. Using TEOS oxide achieves the fastest growth length (~52.5 μm), and using inserted SiN exhibits the slowest growth length (~42 μm). Three possible mechanisms could be responsible for the dependence of MILC growth length on the underlying insulating layers. The first mechanism proposed by Wong *et al.* is that Ni gettering occurs at the interface between a-Si and the buffered layer, meaning that the different interface between a-Si and the buffered layer would generate different gettering sites of Ni [4]. The second mechanism is the effect of stress on lateral growth behavior during MILC. Tensile stress enhances the breakage of Si–Si bonding and increases the number of absorbing Si atoms at the front of the $NiSi_2$/a-Si interface. This tensile stress also generates more vacancies in the $NiSi_2$ precipitates, and these vacancies raise the diffusion rate of Ni atoms through $NiSi_2$. Consequently, the tensile stress enhances MILC growth length, whereas the compressive stress retards it [10]. Thus, the stress of the underlying insulating layer is reasonable to affect MILC growth length. This stress may originate from the different coefficients of thermal expansion between a-Si and the proximity layer, the different lattice constants of various films, and intrinsic stress caused by film shrinkage, although the realistic stress interaction is difficult to gauge [11]. We believe that the higher compressive stress (-312 MPa) of the wet oxide could explain the lower MILC growth length compared to the growth length of the TEOS oxide (-52 MPa). The third possible cause is the outdiffusion of the released hydrogen from the underlying insulating layer, such as SiN, because the MILC growth length of the H_2-doped sample was retarded [2]. The higher H content signifies a film with less dangling bonds in amorphous Si, leading to a lower MILC growth length. We believe that the released hydrogen from SiN would counteract the effects of tensile stress (1.2 GPa), resulting in the slowest growth length.

Fig. 2 shows the I_D–V_G curves of a p-channel TFT and shows that using different underlying insulating materials results in a substantial impact on the electrical characteristics because of the different crystallization conditions and channel/bottom oxide interface. Fig. 3 shows the threshold voltage and subthreshold swing. The threshold voltage (V_{th}) is defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100$ nA at $V_{\text{DS}} = 0.1$ V. Figs. 4 and 5 show the field-effect mobility and output characteristics (the I_D–V_D curve). The deep states that originate from the dangling bonds in grain boundaries influence the threshold voltage and subthreshold swing, whereas the tail states that originate from intragrain defects affect field-effect mobility [12]. Kim *et al.* proposed that a higher MILC growth rate may generate lower trap density in the poly-Si channel [2]. However, they did not

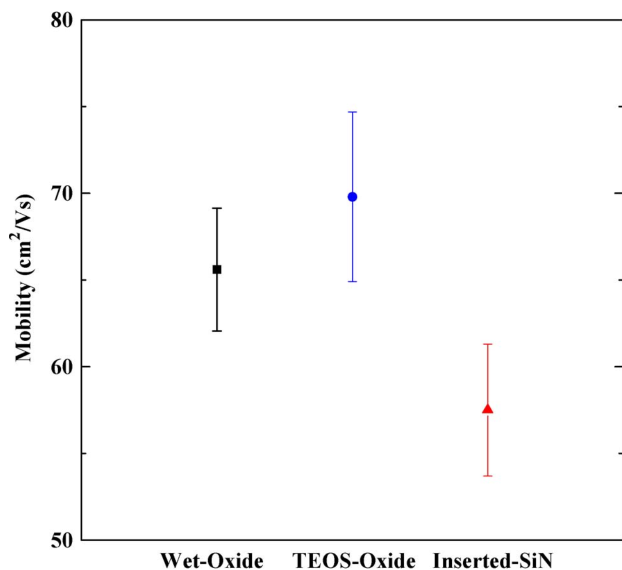

Fig. 4 Variation of mobility as a function of channel width for $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$.

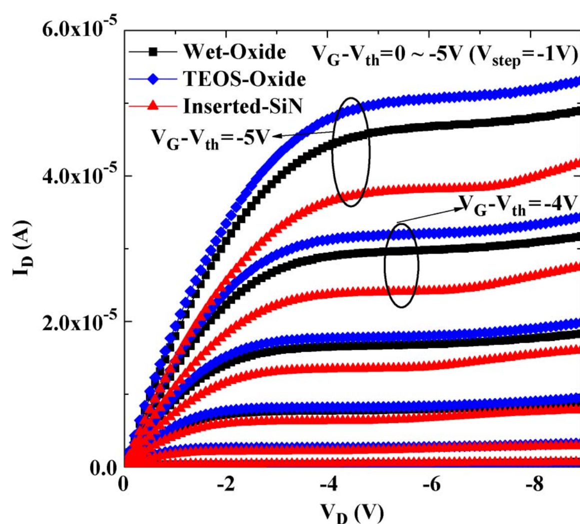

Fig. 5 Output characteristics (the I_D–V_D curve) of n-channel TFTs with $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$ for all samples.

catalogue the types of defects or verify this theory with any electrical characteristics of transistors. The inserted SiN sample exhibits the lowest mobility, the worst output characteristics, and the highest threshold voltage, correlating well with the slowest MILC growth length. In contrast, the TEOS oxide sample exhibits superior mobility, although with a slightly higher threshold voltage and subthreshold swing, compared to the wet oxide sample. Therefore, the underlying insulating layers affect not only the MILC growth length but also the electrical characteristics.

IV. Conclusion

This letter has clarified the effects of underlying insulating layers on MILC growth length and electrical characteristics. Three possible mechanisms can be used to explain the dependence of MILC growth length on the proximity layer. In addition, other than the difference in MILC growth length, the underlying insulating layers affect threshold voltage and mobility. Based on the comparison among underlying insulating layers, using SiN not only retards MILC growth length the most but also exhibits the worst threshold voltage and mobility. Therefore, we believe that the three probable mechanisms, which can be affected by the dopant, annealing, and different fabrication processes, can provide guidance for further examinations on the effects of the proximity layer.

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