Quadrature current-reused divide-by-3 semi-dynamic frequency divider with active balun

C.-Y. Lin, P.-Z. Rao, Y.-K. Lin and S.-J. Chung

A divide-by-3 semi-dynamic frequency divider (SDFD) with active balun is presented using the current-reused technique. The proposed SDFD is composed of a Gilbert cell mixer, one stage of static divider and an active balun. The LO switching stage of the Gilbert cell mixer is also the current source of the static frequency divider to construct the current-reused architecture. At the incident power of 0 dBm, this frequency divider operates at the maximum bandwidth of 1100 MHz from 21.5 to 22.6 GHz. The power consumption of the divider is 12 mW at a 1.5 V supply voltage.

Introduction: With the growing requirement of high data communication capabilities, the 60 GHz UWB system is being developed for new consumer applications. The proposed divide-by-3 frequency divider is employed to be divider 2 at the second stage of the frequency divider, as shown in Fig. 1*a*. In general, the divide-by-2 static frequency divider is the most often used architecture in the design. However, the divide-by-3 frequency divider can simplify PLL design with more flexibility. The divide-by-3 frequency divider has been well studied [1, 2]. Based on the Miller divider, the circuit diagram of SDFD is composed of a mixer, N stages of CML static frequency divider and a feedback path to the mixer [3]. The output frequency of the SDFD can be written as

$$f_o = \frac{f_{\text{in}}}{2^N \pm 1} \tag{1}$$

where f_{in} is the input frequency, and the frequencies that are generated by the signs of plus and minus will be coexistent when a double-sideband (DSB) mixer is adopted in the loop. The division ratio of the SDFD is equal to $2^N \pm 1$, and the signs of plus or minus in the equation can be decided by choosing the down or up conversion of the mixer. As shown in Fig. 1*b*, the proposed frequency divider based on the Miller divider utilises a Gilbert mixer together with a divide-by-2 current mode logic (CML) static divider to implement a divide-by-3 function.

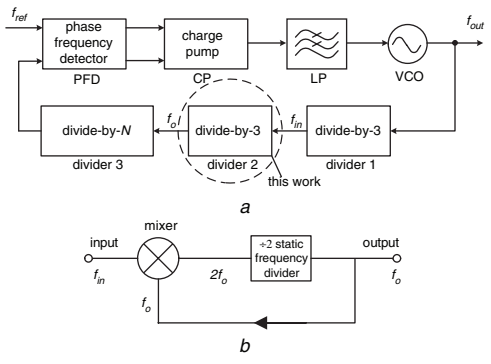

Fig. 1 *60 GHz UWB PLL with proposed devide-by-3 SDFD, and divide-by-3 semi-dynamic frequency divider*

a 60 GHz UWB PLL with proposed devide-by-3 SDFD
b Divide-by-3 semi-dynamic frequency divider

Traditionally, the LC network baluns and the microstrip line transformers are lossy and expansive for larger physical size, which limit the practicability of the passive baluns in the radio frequency integrated circuit (RFIC) designs. Furthermore, an RC polyphase filter is employed to accomplish quadrature input in the SDFD [2], but this method has drawbacks on peak phase error and peak amplitude attenuation when the RC polyphase filter is adopted. Conversely, the active baluns with compact size may have the characteristics of more acceptable gain imbalance and phase imbalance [4].

Circuit design: The completed circuit schematic of the SDFD is shown in Fig. 2. The SDFD comprises an active balun and a static frequency divider with an active cascode mixer. First, the large area consumption passive balun is replaced with the compact-size common-gate (CG) and common-source (CS) active balun in integrated circuit designs. The differential output signals, which characterise balanced amplitude and phase on the operated frequency, would be generated under a single-end input. Secondly, the adopted static frequency divider consists of sampling pairs and latching pairs (M_1–M_8) with an inductive load to convert the current to voltage signals, and the current sources are controlled by the MOSFETs M_9–M_{12}, which are also the LO switching stages of the cascode mixer. Moreover, from (1), the division ratio is equal to 2 ± 1 ($N = 1$); the CML divider is designed to be able to divide the mixed frequency less than f_{in} to ensure that the CML divider also has an additional function of a lowpass filter. Thirdly, the cascode mixer is based on a Gilbert cell, which is made up of an LO switching stage (M_9–M_{12}) and an RF transconductor stage (M_{13}–M_{14}). The transistors M_9–M_{12} are reused by the Gilbert mixer and the static frequency divider with the same path of DC current, which not only decreases the power consumption, but also makes the circuitry more compact and, further, the output signals of the static divider are connected to LO switching stage of the Gilbert mixer. Finally, the mixed signal from the mixer is fed into the static frequency divider at points p_1–p_4, and then the quadrature outputs of the divide-by-3 SDFD are produced at the nodes I^+, I^-, Q^+ and Q^-, respectively.

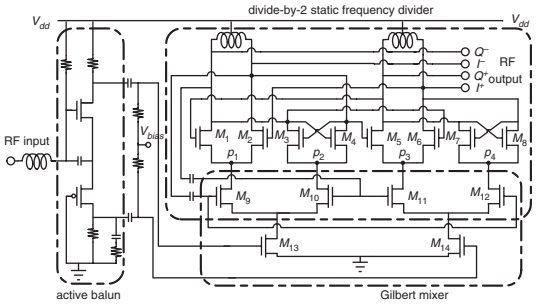

Fig. 2 *Schematic diagram of proposed semi-dynamic frequency divider*

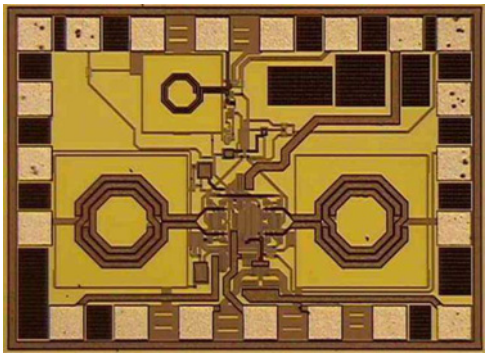

Fig. 3 *Photograph of fabricated frequency divider, chip size 1.1 × 0.8 mm²*

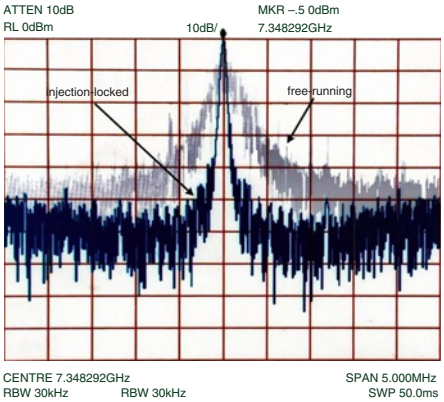

Fig. 4 *Measured output spectrum of SDFD at 22.05 GHz input*

Experimental results: The die photograph of the proposed SDFD is shown in Fig. 3 with a chip size of 1.1 × 0.8 mm². At a 1.5 V supply voltage, the total power consumption is 12 mW without taking that

consumed by the output buffers into consideration. Under free-running conditions, the SDFD oscillates at frequency of about 7.35 GHz. Fig. 4 shows the overlapped measurement result of the frequency spectrum of the free-running and the injection-locked SDFD. The injection-locked behaviour will be observed as long as the input signal f_{in} is applied at the triple frequency of f_o. The input sensitivity was measured using an external injection source applied to the input port of the active balun. The sensitivity of the divide-by-3 SDFD is shown in Fig. 5. The locking range will be increased as the input power level increases. With an injection power of 0 dBm, maximum bandwidth of 1100 MHz from 21.5 to 22.6 GHz was obtained.

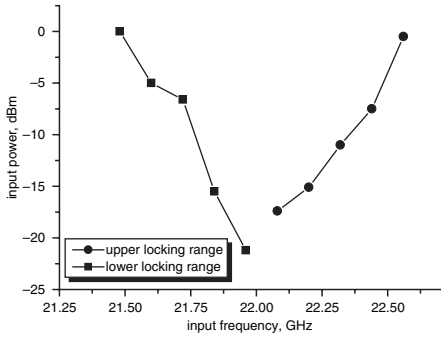

Fig. 5 *Measured input power against input frequency of SDFD*

Conclusion: The proposed SDFD with active balun was designed and fabricated using the TSMC 0.18 μm CMOS process. With active balun and current-reused technique, the proposed quadrature divide-by-3 SDFD has advantages on chip size and DC power consumption at the same operating frequency.

Acknowledgment: The authors thank the Chip Implementation Center (CIC) of the National Science Council, Taiwan, for their technical support.

8 September 2011
doi: 10.1049/el.2011.2606
One or more of the Figures in this Letter are available in colour online.

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