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Two-bit/four-level Pr_2O_3 trapping layer for silicon-oxide-nitride-oxide-silicon-type flash memory

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This study proposes and demonstrates a silicon-oxide-nitride-oxide-silicon (SONOS)-type memory device based on a high-*k* dielectric praseodymium oxide (Pr_2O_3) trapping layer. In the proposed design, channel hot electron injection programming and band-to-band hot-hole injection erasing allow highly efficient two-bit and four-level device operation. The proposed design also has a total memory window of 5 V, a ten-year V_t retention window larger than 0.8 V between adjacent levels, and enough memory window for 10^5 programming/erasing cycles of endurance. The proposed SONOS-type Pr_2O_3 trapping layer flash memory exhibits large memory windows, high program/erase speed, good endurance, and good disturbance characteristics. © *2012 American Vacuum Society*. [DOI: 10.1116/1.3668101]

I. INTRODUCTION

Conventional floating gate (FG) memory devices encounter problems with scaling down because they use a thick tunneling oxide to guarantee a long charge retention time for continuous charge storage.[1] Upon scaling the tunneling oxide thickness down, the FG easily loses charge due to defect generation caused by program/erase cycles or direct current tunneling.[2] According to the *International Technology Roadmap for Semiconductors* (ITRS), there are critical limitations for aggressively scaling down conventional nonvolatile floating gate memories below the 50 nm node.[3] A silicon-oxide-nitride-oxide-silicon (SONOS) structure for charging devices has recently become attractive because it does not have a planar scaling problem for floating gate isolation and shows great potential for achieving high program/erase speed, low programming voltage, and low power performance.[4] However, issues such as erase saturation and vertical stored charge migration remain a problem for SONOS memory.[5,6] Many recent studies present different types of high-*k* trapping layers as potential candidates for replacing Si_3N_4 to provide charge storage in nonvolatile memory.[6–10] Based on discrete storage nodes, SONOS-type flash memory has great potential to achieve high program/erase speed, low programming voltage, low power performance, a large memory window, excellent retention, and good endurance.

Rare earth oxides such as Pr_2O_3 are attractive candidates for trapping layers in memory devices due to their thermodynamic stability, high dielectric constant, proper conduction, valence band offset with silicon, low lattice mismatch with silicon, and excellent electrical properties.[11–14] High trapping state densities can improve the charge-trapping efficiency and, ultimately, achieve a larger operation window. This makes it possible to further reduce the operation voltage and potentially improve memory device scaling.

The experiment in this study fabricated a high performance nonvolatile memory with a high-*k* material praseodymium oxide (Pr_2O_3) charge-trapping layer. The proposed design has good characteristics in terms of a considerably large memory window, high speed program/erase, good endurance, and good disturbance for two-bit and four-level device operation.

II. EXPERIMENT

Figure 1 schematically depicts the device structure and process flow of the proposed flash memory. The fabrication process of the praseodymium oxide memory devices began with a local oxidation of silicon (LOCOS)[15] isolation process on *p*-type, 5 – 10 Ω cm, (100) 150 mm silicon substrates. First, a 3-nm-thick tunnel oxide was thermally grown at 1000 °C in a vertical furnace system. A praseodymium oxide layer was then deposited by the E-gun method[16] with praseodymium oxide targets. The samples then went through rapid thermal annealing (RTA) treatment in N_2O ambient at 900 °C for 1 min. A blocking oxide approximately 10-nm-thick was then deposited by high-density plasma chemical vapor deposition (HDPCVD)[17] followed by a 1 min, 900 °C N_2 densification process. A 200-nm-thick poly-Si layer was then deposited by low pressure chemical vapor deposition (LPCVD)[18] to serve as the gate electrode. The gate electrode was patterned and the source/drain (S/D) and gate were doped with self-aligned phosphorous ion implantation at a dosage and energy of 5×10^{15} ions/cm^{-2} and 20 KeV, respectively. The substrate contact was

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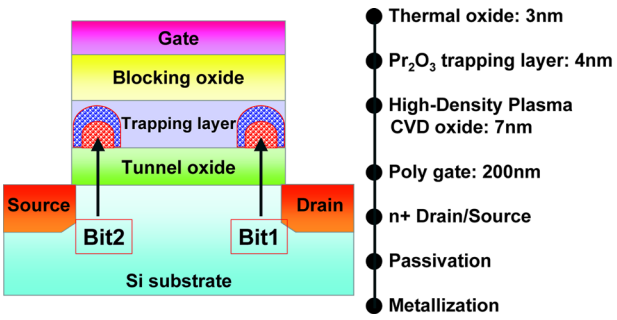

FIG. 1. (Color online) Pr_2O_3 flash memory cross-section cell structure and process flow of the proposed flash memory cell.

patterned and the sub-contact was implanted with BF_2 at a dosage and energy of 5×10^{15} ions/cm^{-2} and 40 KeV, respectively. After these implantations, the dopants were activated at 950 °C for 20 s. Standard complementary metal oxide semiconductor (CMOS) procedures were subsequently completed to fabricate praseodymium oxide high-*k* memory devices.

III. RESULTS AND DISCUSSION

The proposed Pr_2O_3 trapping layer flash memory employs channel hot-electron injection and band-to-band hot-hole injection for programming and erasing, respectively.[19] All devices described in this paper had dimensions of L/W = 2/2 μm. Figure 2 shows the program characteristics as a function of pulse width for different operation conditions. Both source and substrate terminals were biased at 0 V. The "V_t shift" is defined as the threshold voltage change of a device between the programmed and the erased states. With $V_d = V_g = 10$ V, relatively high speed (10 μs) programming performance can be achieved with a memory window of approximately 2.5 V. Figure 3 plots the erase characteristics as a function of various operation voltages. The devices were programmed with a 3 V memory window and erased. Excellent erase speeds of various V_g (from −5 to −7 V) and $V_d = 9$ V were obtained. More importantly, there was no significant over-erase issue. This is because band-to-band hot hole erasing decreases the vertical electric field by

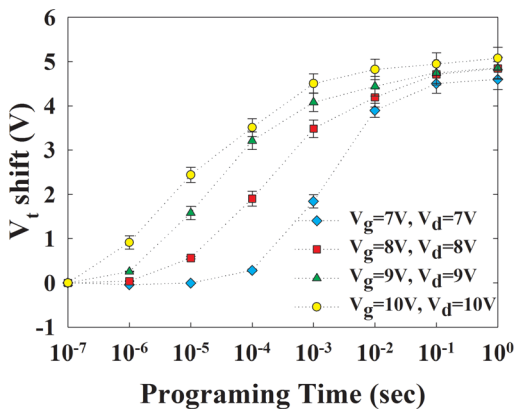

FIG. 2. (Color online) Program characteristics of the memory devices with different programming conditions.

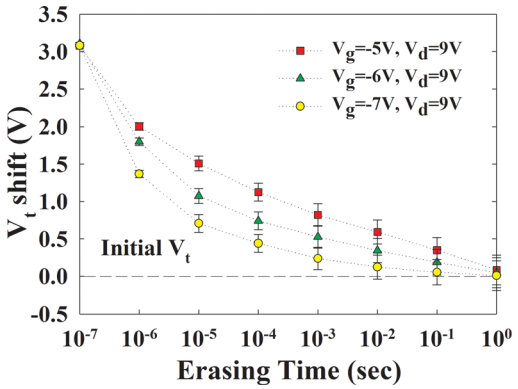

FIG. 3. (Color online) Erase characteristics of the memory devices with different erasing voltages.

decreasing trapped electrons in the trapping layer, and significantly reduces the hole injection into the trapping layer. Based on the discrete charge storage of the Pr_2O_3 trapping layer, the proper bias scheme can feasibly achieve 2-bit operation.[20] Forward and reverse reads can detect the information stored in the programmed Bit 1 and Bit 2, respectively. This means that it is possible to program Bit 1 and read the information using a reverse read scheme.[21]

Figure 4 shows the four-level threshold voltage (V_{th}) distribution of multilevel programming wherein a sharp V_{th} distribution can achieve reliable operation. The V_{th} distribution reveals that the proposed Pr_2O_3 trapping layer is uniform. The V_{th} distribution between adjacent bits still has a memory window larger than 1 V to detect the information. This demonstrates the feasibility of performing four-level operation with the proposed Pr_2O_3 trapping layer memory through a reverse read scheme in a single cell. Moreover, the V_{th} distribution range becomes fatter and less sharp. This is due to increased programming voltage, longer time, and broader channel hot electron distribution range. Thus, 4-level operation adopts a low voltage for sharp V_{th} distribution, but requires a memory window larger than 0.8 V to detect the information. Figure 5 illustrates the retention characteristics for four-level operation at room temperature. These results show that the retention time of the memory with a Pr_2O_3 trapping layer can be up to 10^4 s for 15% and

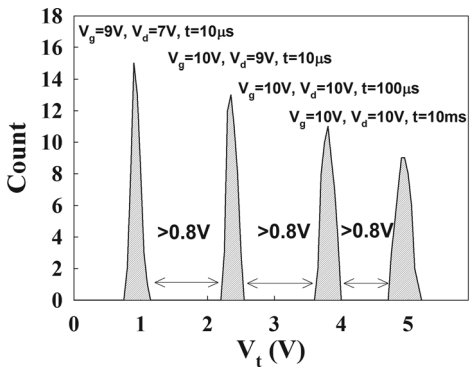

FIG. 4. Four-level threshold voltage (V_{th}) distribution of multilevel programming: The V_{th} distribution between adjacent bits still has a memory window larger than 0.8 V to detect the information.

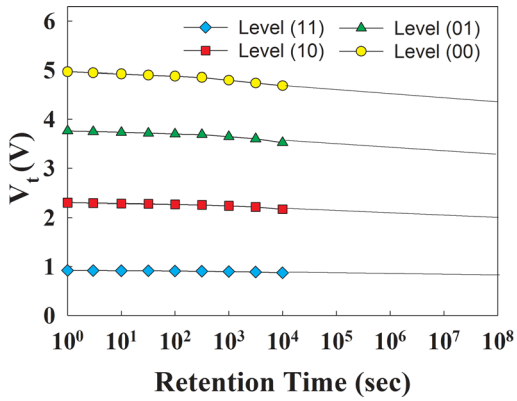

FIG. 5. (Color online) Four-level retention characteristics of Pr_2O_3 memory devices at T = 25 °C: The level-to-level memory window still has a memory window larger than 0.8 V up to 10^8 s.

10^8 s for 35% charge loss at room temperature. The memory window for level-to-level still has a memory window larger than 0.8 V and can detect information for up to 10^8 s.

Figure 6 shows the endurance characteristics for four-level operation after 10^4 P/E cycles. Slight memory window narrowing is apparent, and the individual threshold voltage shifts in the program and erase states become visible after 10^3 cycles.

This indicates the formation of operation-induced trapped electrons[22] in the tunneling oxide or a mismatch between the localized spatial distributions for injected electron and holes using channel hot-electron programming and band-to-band hot-hole erasing. The uncompensated electron resulting from residual charges in the Pr_2O_3 trapping layer subsequently causes the V_t to increase gradually over the P/E cycling. Even the four-level operation has a sufficient memory window (>0.8 V) to detect information up to 10^4 P/E cycles.

Figure 7 shows the programming drain disturbance of the proposed Pr_2O_3 flash memory. Three different drain voltages (V_d = 5, 7, and 9 V) were applied to the programming drain disturbance measurements at room temperature. Results show that a sufficient programming drain disturbance margin exists ($\Delta V_t < 0.5$ V) after programming at a value for V_d of 9 V at room temperature. Figure 8 shows the gate

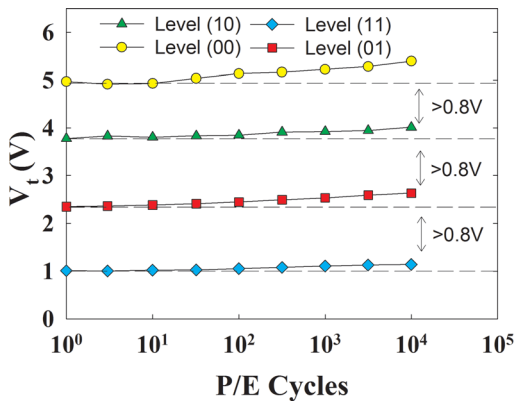

FIG. 6. (Color online) Four-level endurance characteristics of the Pr_2O_3 memory devices: A sufficient memory window (>0.8 V) can obtained and we can detect the information up to 10^4 P/E cycles.

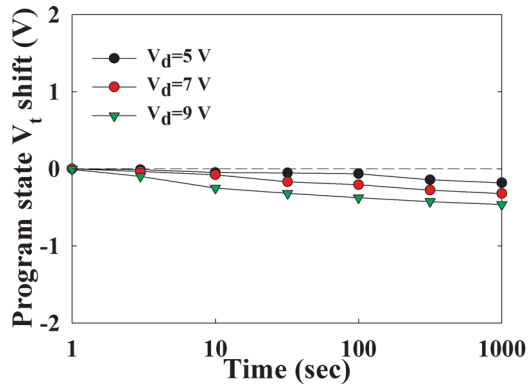

FIG. 7. (Color online) Drain disturbance characteristics of the Pr_2O_3 memory cells: A sufficient programming drain disturbance margin exists ($\Delta V_t < 0.5$ V) after programming at a value of V_d of 9 V at room temperature.

disturbance characteristics in the erasing state. For cells sharing a common word-line, gate disturbance may occur when one of the cells is being programmed. A threshold voltage shift of 0.2 V occurred under the following conditions: $V_g = 10$ V, $V_s = V_d = V_{sub} = 0$ V, and stress for 1000 s. Because of the small voltage drop at the tunnel oxide due to thicker block oxide, the proposed memory exhibits good gate disturbance characteristics with a tunnel oxide 3 nm thick. Figure 9 demonstrates the erase-state threshold voltage instability induced by read disturbance in a localized Pr_2O_3 trapping storage flash memory cell under different operation conditions. The read-disturb effect is the result of two factors: the word-line and the bit-line. The word-line voltage during reading may increase room temperature (RT) drift in the neighboring bit and a relatively large read bit-line voltage may cause unwanted channel hot-electron injection. This subsequently results in a significant threshold voltage shift in the neighboring bit. The measurements in this study applied gate and drain biases and placed the source at ground. Results demonstrate that almost no read disturbance occurred in the proposed Pr_2O_3 flash memory under low-voltage reading ($V_g = 4$ V; $V_d = 2$ V). Even for a larger memory window, there is almost no read disturbance (ca. 0.1 V) after operation at $V_d = 4$ V after 1000 s at 25 °C.

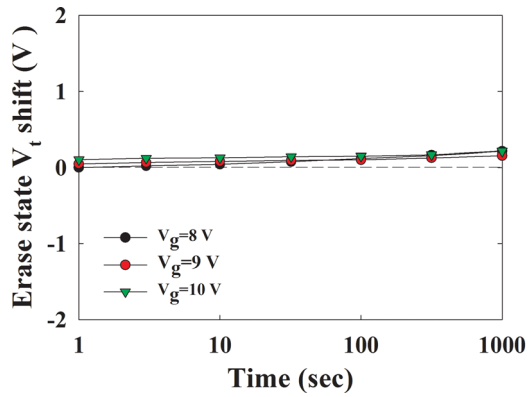

FIG. 8. (Color online) Gate disturbance characteristics of Pr_2O_3 memory devices: A threshold voltage shift of 0.2 V occurred after stressing at $V_g = 10$ V and $V_s = V_d = V_{sub} = 0$ V for 1000 s.

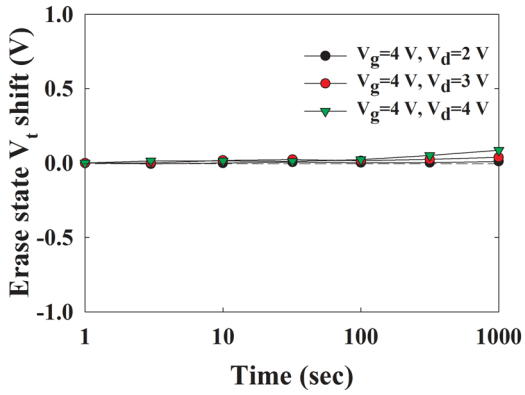

FIG. 9. (Color online) Read disturbance characteristics of the Pr_2O_3 flash memory: A slight V_t shift occurred for $V_d < 4$ V, after 1000 s at 25 °C.

IV. CONCLUSION

This study investigates the effect of memory on the performance of a Pr_2O_3 SONOS-type flash memory device. The proposed design has good characteristics in terms of large memory windows, high speed program/erase, excellent endurance, and good retention for two-bit/four level operation. Hence, Pr_2O_3 may be a candidate material for the trapping layers of a SONOS-type memory device.

ACKNOWLEDGMENT

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