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# The Strained-SiGe Relaxation Induced Underlying Si Defects Following the Millisecond Annealing for the 32 nm PMOSFETs

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The formation of the induced defects in the underlying Si substrate from the interaction of the partly relaxed source/drain strained-SiGe layer and subsequent millisecond annealing (MSA) have been systematically explored. It could be found that implantation in the shallower region of the strained-SiGe layer did not form defects in the underlying Si because the remaining strained-SiGe layer was sufficiently thick to resist wafer bending in response to the MSA thermal stress. However, deeper medium-level implantation indeed destroyed the part of the pseudomorphic strained-SiGe and the remaining strained-SiGe was too thin to withstand a significantly compressive stress induced by MSA surface heating and larger coefficient of thermal expansion (CTE) for SiGe than it for Si. Then brittle silicon substrate suffered a great tensile stress to generate numerous defects into plastic deformation. During MSA cooling, the over-bending of the surface SiGe layer contracted more than Si substrate and further results in highly tensile bending. Consequently, high defect density in the underlying Si results in high junction leakage and wafer bending leads to photolithographic limitation. A new approach for modifying the implantation conditions was developed to achieve a relaxation-less strained-SiGe layer and defect-free underlying Si substrate for the 32 nm PMOSFETs.
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Strain engineering and material innovation have been critical to improve the performance of CMOS devices over the past few years. For instance, selective epitaxially SiGe is used in source/drain regions to introduce uniaxially compressive stress into PMOSFETs, substantially enhancing the carrier mobility and the drive current, which increase is very difficult to be achieved by the conventional Si technology.[1–4] Source/drain strained-SiGe with low resistivity, formed using a well controlled doping concentration and by minimizing the short channel effect associated with a shallow doping profile, is important in CMOS device scaling. Recently, millisecond annealing (MSA, flash annealing or laser annealing),[5–7] which promotes dopant activation but causes less dopant diffusion at high annealing temperature, has emerged as an alternative approach for high-performance CMOS devices. The combination of strained-SiGe in the source/drain regions as channel stressors and MSA process is a candidate method for improving the performance of devices based on the 32 nm technology. However, the relaxation of the strained-SiGe layer due to the large thermal stress that is induced by MSA may make such a combination challenging.[8–11]

This study elucidates high defect density that results from the combination of strained-SiGe and subsequent MSA processes. Under certain implantation conditions, the MSA process induced defects in the underlying Si and degraded device performance. The phenomenon of defect formation by the MSA treatment is therefore modeled and discussed, and the effective integration of strained-SiGe and MSA process for fabricating 32 nm PMOSFETs is proposed.

## Experimental

A series of PMOSFETs with SiON gate oxide (Equivalent Oxide Thickness, EOT = 12A and Gate length, Lg = 32 nm) were fabricated using source/drain strained-$Si_{1-x}Ge_x$ (x nearly∼0.35) and in-situ Boron doping with a 100 nm-thick layer on 300 mm (001) Si wafers. The pocket implant was conducted in SiGe pattern wafers by implantation using Arsenic (As), at energy of approximately 50 keV and a dose of 3E13 $cm^{-2}$ to suppress the short channel effect (SCE). Spike rapid thermal annealing (RTA) around 1000°C was carried out to recover the damage induced by implantation and to activate the dopants. Laser MSA annealing at around 1200°C for 500 µs then performing to enhance dopant activation, was as plotted in Fig. 1. For another process sequence of implantation followed by SiGe deposition was explored as well, as shown in Fig. 1. The subsequent formation of nickel silicide on SiGe, the deposition of a contact etching stop layer (CESL) and metallization were conducted for the standard process. Then, the performance of the PMOSFETs was evaluated. For comparison, PMOSFETs without a source/drain SiGe structure were also fabricated by a similar process sequence.

## Results and Discussion

As shown in Fig. 2, PMOSFETs with implanted SiGe devices that had undergone RTA and MSA processes exhibited higher junction leakage about four orders of magnitude than that of those without implanted SiGe or millisecond anneal device, implying that the high junction leakage was caused by the combination of the implanted SiGe and millisecond annealing. The severe crystal defects observed in the cross-sectional TEM (XTEM) of Fig. 3a, which led to the significant junction leakage, were identified in the SiGe devices followed the MSA process. However, the TEM selective area diffraction demonstrates that the implanted strained-SiGe layer and the underlying Si substrate remained single crystalline. Surprisingly, the defects were

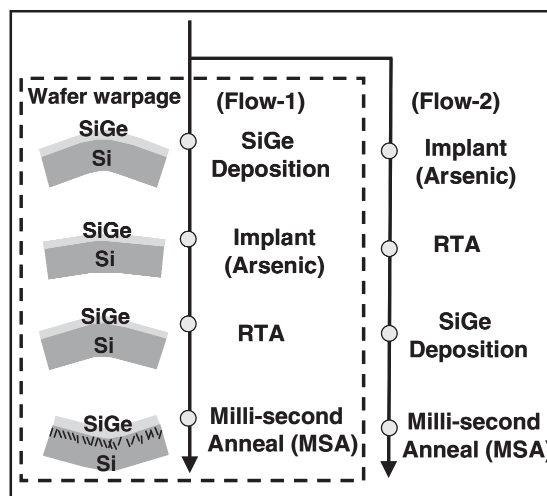


**Figure 1.** The Process flow of the source/drain SiGe followed by implantation or implantation followed by the S/D SiGe, both of sequences are conducted with MSA process.

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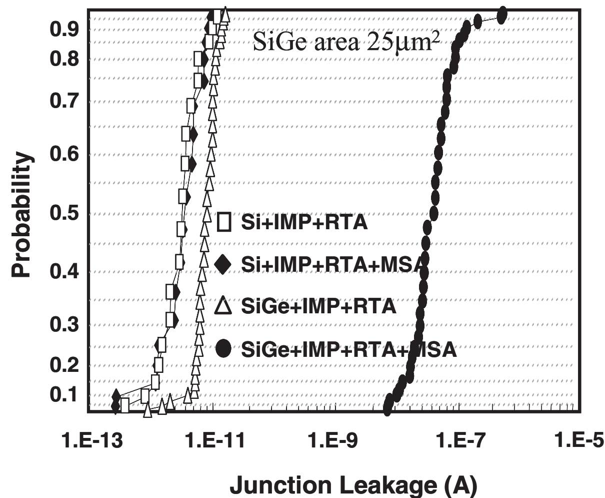
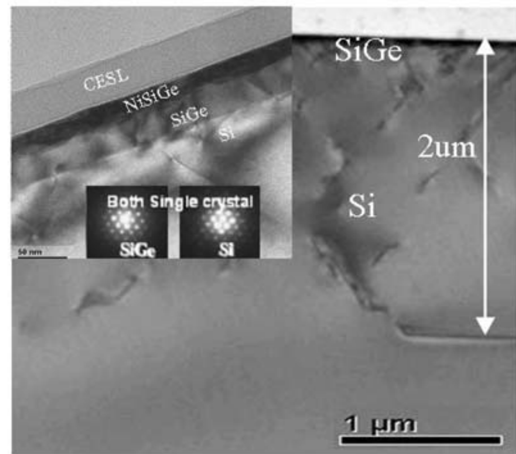
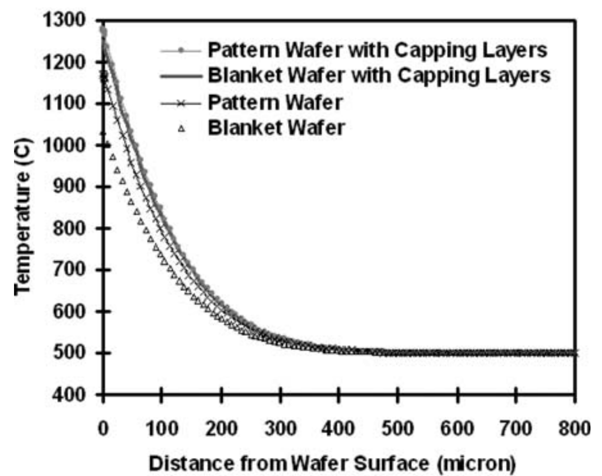



**Figure 2.** The implanted SiGe PMOSFETs device with RTA and MSA processes exhibits higher junction leakage than that of those without implanted SiGe or millisecond anneal device.




(a)




(b)

**Figure 3.** (a) The TEM of the implanted SiGe wafer with the RTA and MSA process shows high defect density in the relaxed SiGe layer as well as in the underlying Si substrate. (b) Simulated MSA wafer temperature profile and exhibited large temperature gradient close wafer surface.

observed not only in the SiGe layer but also in the underlying Si substrate to a depth of 2 μm. Since MSA employed pulsed surface heating with millisecond peak widths at temperatures below the melting point 1418°C of Si at the surface of the wafer (Fig. 3b),[12,13] the very large thermal stress associated with the huge thermal gradient caused dramatic wafer bending would generate many defects in the strained-SiGe layer and the underlying Si substrate. Hence, the formation of defects in the SiGe and Si substrate by the enormous thermal stress that was produced by millisecond annealing was further established. In comparison, applying a small thermal gradient treatment to the implanted SiGe wafer did not produce these defects in the underlying Si.

To investigate the relationship between the formation of defects in the underlying Si substrate and the combination of implanted SiGe and MSA process on the pattern wafer, identical processing conditions were applied to blanket Si (001) wafers and the corresponding optically measured wafer bow height, which revealed the degree of wafer warpage,[14,15] was as plotted in Fig. 4. The strong correlation between wafer bow height and density of defects observed in the Si substrate was well established. From Fig. 4, the 100 nm-thick strained-$Si_{1-x}Ge_x$ (x nearly 0.35) introduced a compressive film stress with wafer concave downward, then the subsequent medium implantation projection range (Rp) using Arsenic (As), at an energy of approximately 50 keV and a dose of 3E13 $cm^{-2}$ to make species to reach medium position of the strained-SiGe layer, damaged the upper portion of the strained-SiGe layer, and partially relaxed stress in the strained-SiGe, reducing wafer warpage. Following spike RTA, the implant-damaged strained-SiGe layer was repaired, but not completely. The subsequent MSA caused significant wafer warpage and plastic deformation from its initial compressive to its final high tensile state. Then, defects in the underlying Si substrate were observed as shown in the TEM image. Meanwhile, large wafer warpage up to 150 μm in tensile state impacted critical lithography stage, such as contact-hole lithography. For comparison, a strained-SiGe sample directly underwent the MSA process, exhibiting no change in bow height, while its underlying Si was defect-free and did not have warpage-induced lithographic limitation. This result implies that some relaxation of strain SiGe caused by implantation considerably changes the bow height and causes the formation of defects in the underlying Si for strained-SiGe that undergoes MSA.

To eliminate the relaxation of strain SiGe by post-SiGe medium implantation range Rp of n-type species, As, implantation conditions are modified to prevent strain relaxation, defect formation and warpage-induced lithographic limitation. Accordingly, a lighter atom, phosphorus (P), with energy of around 30 KeV and a dose of 4e13 $cm^{-2}$ was

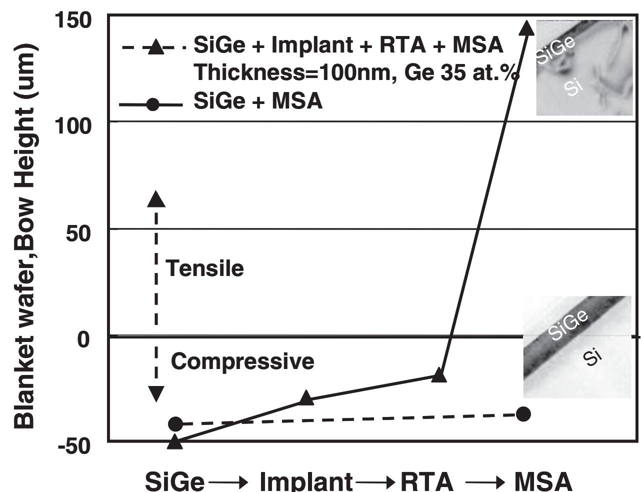



**Figure 4.** Change in bow height of strained-SiGe wafer associated with following implantation, RTA and subsequent MSA, which caused large change in bow height of SiGe wafer. A fully strained-SiGe sample directly underwent MSA, exhibited no change in bow height and had a defect-free underlying Si.

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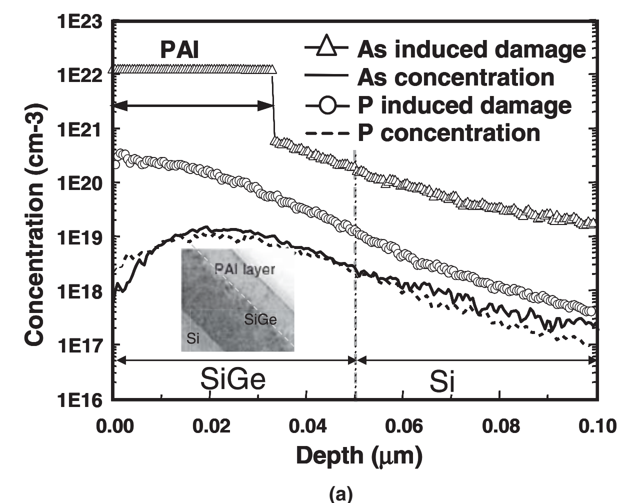
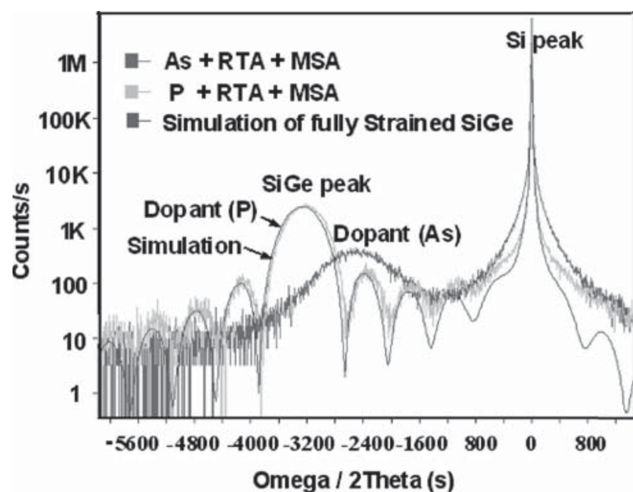
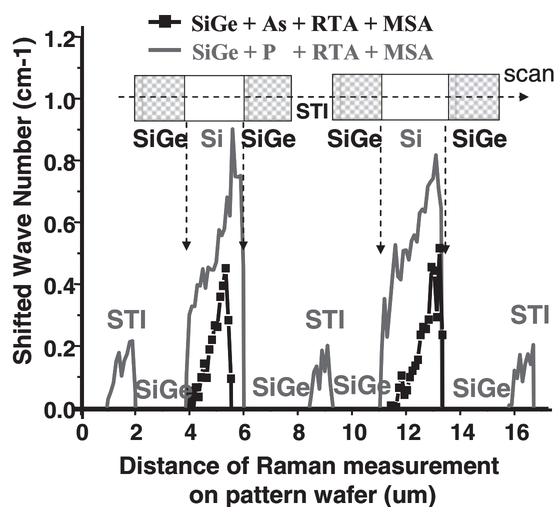



(a)

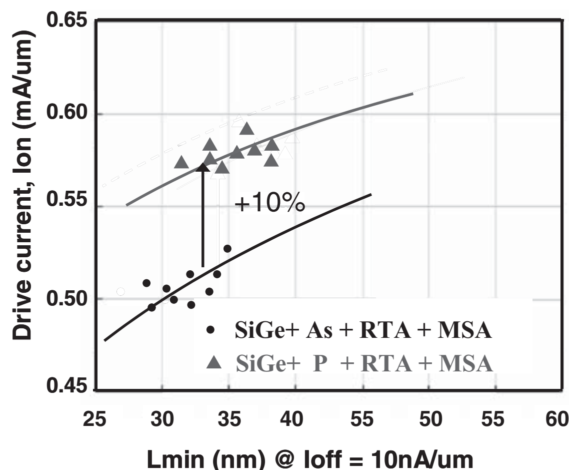



(b)

**Figure 5.** (a) Simulated that implant species arsenic (As) and phosphorus (P) at the comparable implant energy and concentration caused different degrees of damage in the strained SiGe layer (b) The relaxation of strained-SiGe is a function of dopant impurities, determined from the XRD rocking curve.




(a)




(b)

**Figure 6.** (a) Raman measurements (wave number shifts) indicated the relaxation of strained-SiGe is associated with post implanted species, As and P, and their effects on the Si channel stress in Si; (b) Drive current, Ion-Lmin was affected by the implanted As and P induced damage effect in the strained-SiGe layer, which causes various degrees of strain relaxation upon the RTA and MSA.

used to give the same medium implantation range Rp of As, and minimize the SCE properties. In the inset of Fig. 5a TEM image indicates that a medium implantation Rp of the species, As, was employed into strained-SiGe layer and led to a clear pre-amorphous implant (PAI) layer in the SiGe layer as well as feeding to simulation result by the kinetic Monte Carlo (kMC) model. The degree of the As induced implantation damage in SiGe was defined during simulation that Si atoms had moved one-third of the way from original position toward vicinity.[16–18] Since As atoms are large, the damaged layer of pre-amorphorized implantation resulted in the large relaxation of strain SiGe and severely affected the pseudomorphic SiGe. The following RTA process was unable to recover relaxed strained-SiGe, which was indicated from the broadening XRD rocking curve of SiGe in Fig. 5b. Therefore, subsequent MSA produces defects in the underlying Si substrate, as revealed by the XRD rocking curve of the broadening Si peak in Fig. 5b. Nevertheless, phosphorus, which has a small atomic size as compared to As, implanted at a concentration close to that of the As atoms, did not cause PAI in the strained-SiGe layer, as shown in Fig. 5a. Therefore, the subsequent spike RTA process enabled the non-PAI SiGe to be almost fully recovered as strained-SiGe, and the following MSA did not cause defects in the underlying Si, as revealed by the tight SiGe profile and shaper Si peak in the XRD rocking curve of phosphorus. Figure 5b also presents results of a simulation of fully strained-SiGe samples as a reference. The figure reveals that the strained-SiGe was almost fully recovered. Hence, well-controlled implantation in the source/drain SiGe is required to prevent strain relaxation and defect formation.

Properly selecting implanted species to form almost fully strained-SiGe enables Si channel stress to be increased to further boost the device drive current. In Fig. 6a, the Raman measurements reveal the relaxation of strained-SiGe by various implanted species on the Si channel stress of the Si substrate. Post-SiGe arsenic implantation caused large strained-SiGe relaxation, reducing the effective stress in the Si channel below that associated with SiGe relaxation by phosphorus. The 10% higher drive current (Id,sat) gain of PFET devices versus Lmin (minimum gate length) associated with post-SiGe phosphorus than that associated with arsenic in Fig. 6b, was consistent with Raman measurements. Figure 7 plots the relationship of the dopant species and the junction leakage in PMOSFET devices. Upon RTA and MSA thermal treatment, post-SiGe phosphorus implantation can result in an almost fully strained-SiGe layer and does not form defects in the underlying Si substrate. Minimized the leakage current to a

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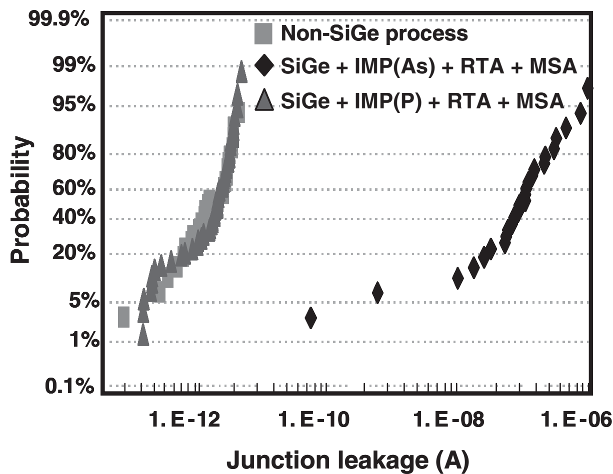


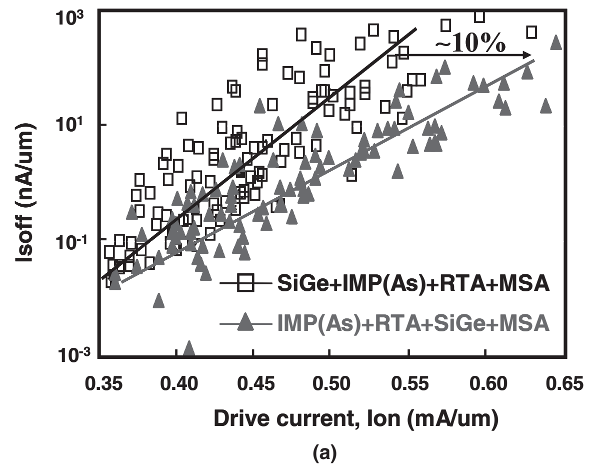

**Figure 7.** Improvement in the P+/n well junction leakage by the post-SiGe implantation of species, P, reduces the relaxation of strained-SiGe and yields a defect-free underlying Si substrate upon RTA+MSA.

level comparable to those of PMOSFET devices are fabricated using a non-SiGe process.

On the other hand, changing the sequence of the implantation species, As, from post-SiGe implantation process to Pre-SiGe implantation process, as revealed Flow-2 in Fig. 1, enables a less relaxed strained-SiGe to be achieved, increasing the drive current gain. Figures 8a and 8b present the device performance of PMOSFETs and junction leakage current of pre-SiGe implantation sequence. As implantation and RTA process prior to strained-SiGe layer were conducted to present a low level of strain relaxation. MSA did not affect low degree of strained-SiGe relaxation and did not form defects in the underlying Si substrate. Then, PMOSFET devices had an Id,sat gain of around 11% due to the low degree of strained-SiGe relaxation and a significantly improved junction leakage than that of those post-SiGe implantation process.

## Mechanism and Model

To understand the formation of defects in the underlying Si during the MSA of implanted strained-SiGe, three implantation conditions - low energy (15 keV) of shallower implantation Rp, medium energy (50 keV) of medium implantation Rp and high energy (70 keV) of deep implantation Rp, made implanted species, As, reach the surface, medium and bottom of the 100 nm-thick strained-SiGe blanket wafer, respectively. The three samples with different implantation conditions were followed by RTA and MSA, causing 11%, 51% and 75% relaxation of strained-SiGe. High-resolution X-ray diffraction reciprocal space maps (HR XRD RSMs)[19] were obtained to characterize the relaxation of strain SiGe and the defects in the underlying Si, as shown in Fig. 9. For the case of 11% relaxation of strained-SiGe, the MSA did not significantly degrade the lightly relaxed strained-SiGe and did not produce defects in the underlying Si substrate, presented in the TEM image, and as revealed by results of the tight XRD RSM patterns of the Si. In Fig. 9b, the medium implantation Rp, RTA process and subsequent MSA caused a 51% strained-SiGe relaxation, which was consistent with a weak SiGe diffraction peak in RSM pattern. MSA of such remarkably relaxed strained-SiGe formed many defects in the underlying Si, as shown in the TEM image, corresponding to the broadening of the Si RSM pattern in the most {111} direction by the defects. Finally, in Fig. 9c, a more deeply implanted Rp, the RTA process and subsequent MSA caused an almost 75% relaxation of strained-SiGe, and produced numerous dislocations in SiGe, which result is related to the very weak SiGe diffraction RSM pattern. MSA applying to a high relaxation of strained-SiGe wafers does not form defects in the underlying Si, as presented in the TEM image, indicat-



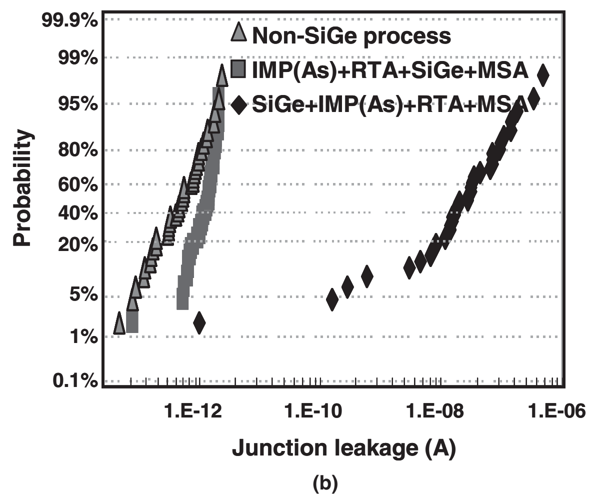




**Figure 8.** (a) Improvement of Ion-Ioff by the change in sequence of SiGe and implantation. Implantation prior to SiGe deposition exhibited less strain relaxation and a higher channel stress; (b) upon MSA, implantation following the SiGe process sequence results in low strain relaxation and few defects in the underlying Si, and consequently improved junction leakage.

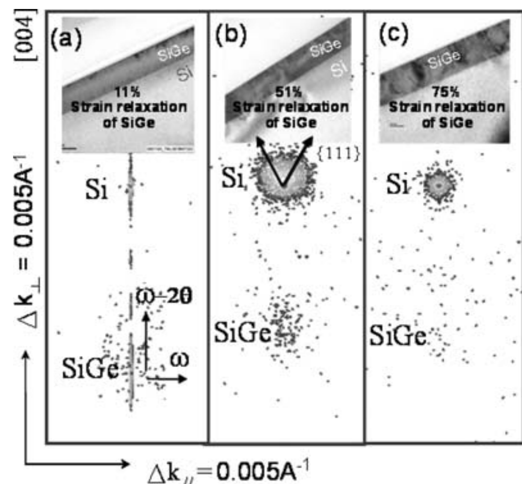



**Figure 9.** High-resolution X-ray diffraction reciprocal space maps (HR XRD RSMs) and TEM of strained-SiGe and underlying Si following implantation under various energy and RTA and MSA, which are associated with various strained-SiGe relaxation (a) No defect formation for 11% relaxation of strain SiGe. (b) Defect formation in the underlying Si for 51% strained-SiGe relaxation. (c) 75% relaxation shows the almost completely relaxed strained-SiGe with weak diffraction peak, and defect-free in the underlying Si.

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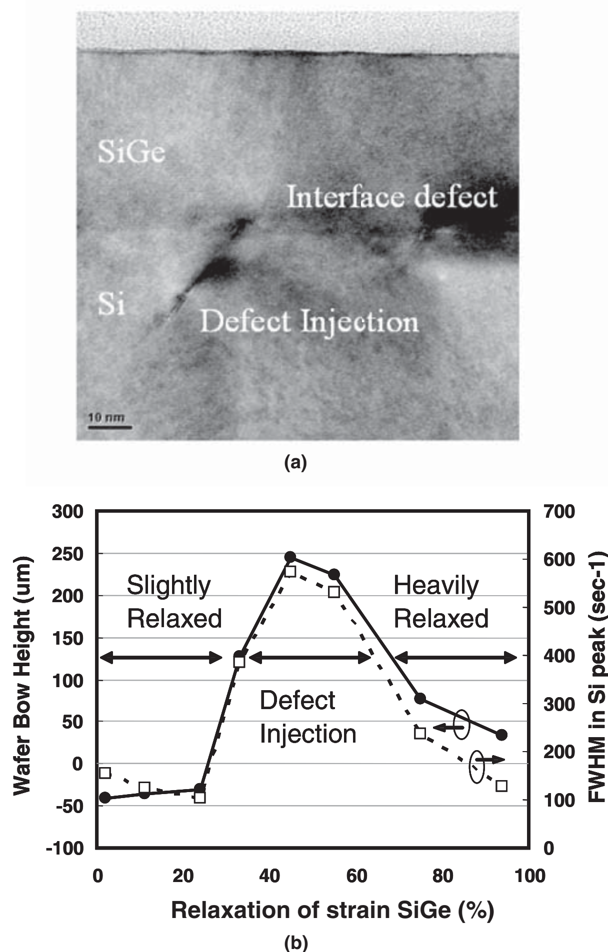


**Figure 10.** (a) Upon MSA, relaxed strained-SiGe caused injection of defects into underlying Si (b) Correlation between relaxation of strain SiGe and injection of defects, determined from wafer bow height and full width at half maximum (FWHM) of Si XRD peak.

ing a slightly broadened Si RSM pattern, owing to the clarity of the Si substrate.

Hence, the degree of strained-SiGe relaxation determines whether defects are formed in the underlying Si substrate under millisecond annealing. Figure 10a the TEM image reveals that upon MSA, the formation of defects or their injection into underlying Si was observed because strained-SiGe underwent moderately medium strain relaxation. Neither excessively low nor excessively high strained-SiGe relaxation was associated with any defect injection into the underlying Si. Therefore, Fig. 10b plots a correlation between the relaxation of strain SiGe and the injection of defects, obtained from the bow height of the SiGe wafer and the corresponding full width at half maximum (FWHM) of the Si XRD peak, respectively.[20] In designing a high performance of CMOS devices with strained-SiGe and MSA, pseudomorphic relaxation of strain SiGe of less than 11% must be maintained to ensure favorable channel stress to boost the drive current and an absence of defect formation in the Si to ensure a low junction leakage current.

The stress of the strained-SiGe layer on the Si substrate can be calculated using Stoney's well-known equation, which assumes uniform biaxial film stress:[21]

$$\sigma_{SG} = \frac{E_S}{6(1-\nu_S)}\frac{d_s^2}{d_f}k, \quad [1]$$

where $E_S$ and $\nu_S$ denote the Young's modulus and Poisson ratio of the substrate; $d_s$ is the thickness of the Si substrate; $d_f$ is the thickness of the strained-SiGe layer, and k is the wafer curvature.

When MSA was performed using pulsed surface heating with a millisecond peak width at a temperature of around 1200°C at the surface of the Si wafer without SiGe layer, as shown in Fig. 3b, the very high thermal stress caused by the huge thermal gradient induced very large wafer bending, which can be expressed as,[22]

$$\sigma_{MSA} = \frac{E_{S,T}}{1-\nu_S}\alpha\Delta T, \quad [2]$$

where α is the thermal expansion coefficient; $E_{S,T}$ is Young's modulus at the MSA temperature, and ΔT is the effective temperature difference between the surface of the wafer and the position of zero temperature gradient, where $\partial T/\partial x = 0$. Since the MSA chamber was thermally insulated, the decrease in the temperature across the Si substrate is given by,[23]

$$T = T_f + A_1 \exp\left(\frac{-x}{x_c}\right), \quad [3]$$

where $T_f$ is the temperature at zero temperature gradient across the wafer. The experimental MSA temperature profile across the surface of the wafer was fitted using parameters $T_f$, $A_1$, and $x_c$ set to 490°C, 814°C and 106 μm. Therefore, the effective temperature difference due to the thermal gradient is represented by

$$\Delta T = \frac{a}{x_T}\left[\int_0^{x_T}\left(T_f + A_1 \exp\left(\frac{-x}{x_c}\right)\right)dx - x_T T_f\right], \quad [4]$$

where $x_T = 396$ μm, and a = 0.4 to fit the experimental data in Fig. 3b. Accordingly, the magnitude of the MSA thermal stress across Si wafer surface was,

$$\sigma_{MSA} = \frac{E_{S,T}}{1-\nu_S}\alpha\frac{a}{x_T}\left[\int_0^{x_T}\left(T_f + A_1 \exp\left(\frac{-x}{x_c}\right)\right)dx - x_T T_f\right].$$

The MSA thermal tensile stress in this experiment at approximately 1200°C for 500 μs was thus around 0.6 GPa. The thermal stress caused by MSA pulse heat in the Si surface region, $d_f$, is given by Stoney's equation,

$$\sigma_{Si} = \frac{E_{S,T}}{6(1-\nu_S)}\frac{d_s^2}{d_f}k, \quad [5]$$

The bow height (B) that is induced by stress is,

$$B = \frac{r^2 k}{2}, \quad [6]$$

where r denotes radius of the wafer, and k is the curvature of the wafer. Substituting Eq. 5 into Eq. 6 yields the k value, and the bow height of Si wafer following the MSA process is given by

$$B \approx d_f\left(\frac{r}{d_s}\right)^2 \alpha\Delta T\frac{E_{S,T}}{E_S}. \quad [7]$$

Given the experimental parameters, the change in the bow height of the pure Si wafer without SiGe layer during the MSA process was small, at around few 10 μm.

The bow height, however, changed significantly around 150 μm when the relaxation of the strained-SiGe was introduced into the MSA process. When both of the film stress and the thermal stress have been determined, the wafers bow height of the strained-SiGe and MSA was as presented in Fig. 10b. It was modeled using the Gaussian function to obtain an empirical fomula to illustrate the bow height change of the SiGe wafer by the compressive stress of the strained-SiGe layer and tensile stress of the MSA, as follows.

$$B = y_0 + \frac{A}{f_{in}\sqrt{2\pi}}\exp\left\{-2\left[\frac{b(1-R)\sigma_{SG} - \sigma_{MSA}}{f_{in}}\right]^2\right\}, \quad [8]$$

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where $y_0$, A, and b are constants; R is the relaxation of strained-SiGe and $f_{in}$ is the interaction factor,

$$f_{in} = m\sigma_{SG} + n\sigma_{MSA},$$

where m and n are also fitting constants. According to Eq. 8, the bow height reached its maximum when b(1-R)$\sigma_{SG}$ was close to $\sigma_{MSA}$. Therefore, the bow height depended on both the magnitude of the strained-SiGe film stress and the MSA thermal stress. Shallow implant Rp in the surface region caused only an 11% relaxation of the strained-SiGe layer, and the compressive film stress was sufficiently high to resist wafer bending associated with MSA thermal tensile stress. Hence, the bow height was negative as compressive as that of the initial strained-SiGe film. When implantation is performed using medium projection range Rp to induce 51% relaxation of the strained-SiGe, the film stress, $\sigma_{SG}$, was reduced by a factor (1-R) showing lower shear yielding stress for deformation during MSA thermal stress,[24,25] and was then too small to resist the MSA tensile stress and the relaxed strained-SiGe wafer buckled in the maximum tensile state. This phenomenon is described by a second moment of inertia,[26] which demonstrates that a suddenly large deformation or over-bending occurred when the applied force exceeded a critical stress or over shear stress for yielding. At the experimental condition, while strained-SiGe relaxation is over around 20%, large SiGe wafer bending occurred under applying MSA tensile stress corresponding to the concept of the second moment of inertia. When deep implantation of Rp destroyed most of the strained-SiGe layer at close to 75% relaxation, the yield-point of relaxed strained-SiGe was further reduced to cause much bending under MSA process. However, the 75% relaxation of strained SiGe was formed with lots of interfacial misfit dislocations and low-density of coherent bonding with Si substrate. The highly relaxed strained-SiGe film is then expanded and contracted along with the externally thermal stress and would not cause any residual strain to the underlying Si substrate during the MSA thermal cycle.

A model of MSA temperature ramp-up and cool down acting on a medium-level of relaxed strained-SiGe to caused defect formation in the underlying Si and wafer bending was therefore proposed. In Fig. 11a, by using micro-second camera and comparing wafer shape with the ellipsometer wafer bow height to investigate real-time wafer bending during MSA heating and cooling on the medium relaxed SiGe wafer. The wafer showed a little compressive bending after SiGe deposition at initial stage. At the next stage the coefficient of thermal expansion is greater for SiGe than for Si such that the SiGe layer expanded more than the silicon substrate during MSA surface heating. The expansion induced a compressive stress exceeding the lower yielding stress of the relaxed strained-SiGe caused a further compressive bending. Thus, brittle silicon substrate suffered a great tensile stress to generate lots of defects into plastic deformation. During MSA cooling at the final stage, the over-bending of the surface SiGe layer contracted more than silicon substrate to become highly tensile bending. Fig. 11b schematically plots the mechanism of the MSA effects on the various implanted strained-SiGe wafers. When the damaged amorphous layer (α layer) was near the SiGe surface, corresponding to shallow implantation Rp, the remained thick and good crystalline strained-SiGe with high yielding stress of deformation can resist the compressive and tensile stress to over-bending during MSA heating and cooling cycle. Once the damaged PAI reached to a medium Rp, the remarkably relaxed strained-SiGe with relatively lower yielding stress of deformation followed with RTA would led to a too-thin strained-SiGe to withstand the large thermal stress during MSA. Meanwhile, the underlying Si substrate encountered a tremendous tensile stress and resulted in defects in the underlying Si along {111} lowest energy slip planes. Furthermore, high-energy implant with a deep Rp to the SiGe/Si interface would form a significantly relaxed SiGe with numerous interfacial misfit dislocations and low-density of coherent bonding with Si substrate. The highly relaxed strained-SiGe film is then expanded and contracted along with the externally thermal stress and would not cause any residual strain to the underlying Si substrate during the MSA thermal cycle.

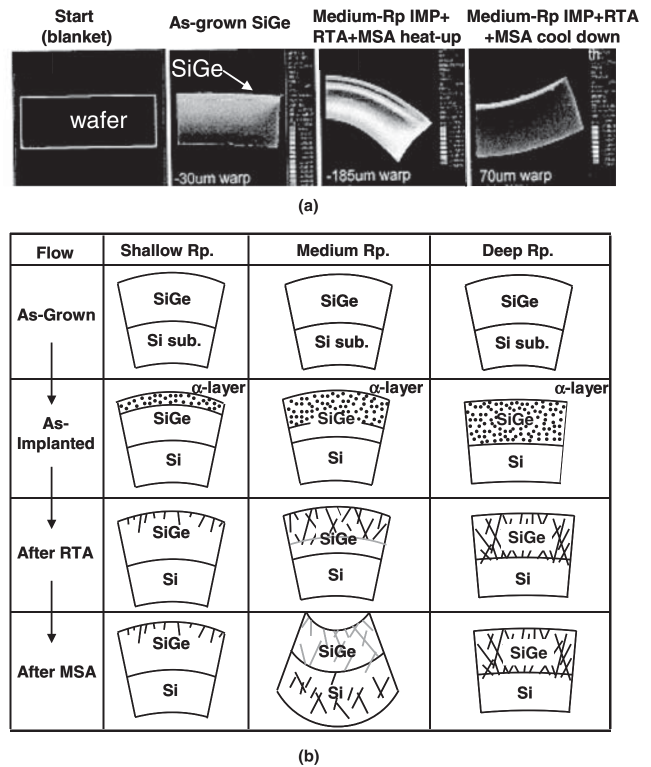


**Figure 11.** (a) Real-time micro-second camera image of change in wafer bow height associated with SiGe deposition and the following MSA temperature ramp-up and cool down. (b) Schematic plot of various implantations Rp to thickness of SiGe layer, change in wafer bow height and resultant injection of defects in underlying Si substrate.

## Conclusions

The degree of strained-SiGe relaxation importantly affected the channel stress and the formation of defects in the underlying Si substrate as well as wafer bending when MSA was applied to the S/D strained-SiGe in 32 nm PMOSFET devices. Low-energy As implantation to cause shallower Rp in the strained-SiGe surface induced low-level 11% of relaxation and did not generate defects in the underlying Si, because the remaining strained-SiGe was sufficiently thick to resist wafer bending by the tensile stress associated with MSA thermal treatment. However, moderate relaxation 51% of the strained-SiGe by medium-energy As implantation revealed the partly relaxed SiGe with lower shear stress of yielding deformation was unable to withstand the significantly compressive stress of the surface expansion to form defects in the underlying Si substrate during MSA heating and more surface contraction of high CTE of SiGe to cause over-bending in the tensile state during MSA cooling. In addition, the 75% relaxation of the SiGe layer by high-energy implantation would for lots of interfacial misfit dislocations and low-density of coherent bonding with Si substrate. The highly relaxed strained-SiGe film is then deformed freely along with the externally thermal stress direction and would not cause any residual strain to the underlying Si substrate during the MSA thermal cycle. Therefore, proper implantation conditions were chosen to provide a relaxation-less strained-SiGe and boost the channel stress, achieving a 10% current gain. The defect-free underlying Si in millisecond-annealed 32 nm PMOSFETs devices exhibits a decrease in the junction leakage current by four orders of magnitude.

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