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Oxygen-Adsorption-Induced Anomalous Capacitance Degradation in Amorphous Indium-Gallium-Zinc-Oxide Thin-Film-Transistors under Hot-Carrier Stress

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This paper investigates anomalous capacitance-voltage (*C-V*) degradation in amorphous indium-gallium-zinc-oxide (*a*-IGZO) thin-film-transistors (TFTs) under hot carrier stress. In vacuum hot carrier stress, both the gate-to-drain capacitance (C_{GD}) and the gate-to-source capacitance (C_{GS}) curves exhibited positive shifts due to electron trapping in the gate dielectric. In addition, an observed increase in capacitance value at a lower gate voltage in the C_{GD} measurement only can be ascribed to interface state creation. However, when the hot carrier stress was performed in an oxygen-rich environment, the C_{GD}-V_G curve showed a significantly positive shift due to the electric-field-induced oxygen adsorption near the drain terminal. The degradation in the C_{GS}-V_G curve is due not only to the positive shift, but also the anomalous two step turn-on behavior. This phenomenon can be ascribed to the electron trapping in the gate dielectric and electric-field-induced oxygen adsorption on the channel layer, especially in the area adjacent to the drain terminal. The electron trapping increased the source energy barrier, with the electric-field-induced oxygen adsorption further raising the energy-band near the drain, resulting in a two-step turn-on behavior in the C_{GS}-V_G curve.

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Amorphous indium-gallium-zinc-oxide (*a*-IGZO) thin-film-transistors (TFTs) have attracted much attention for use in active matrix liquid crystal displays (AMLCD) and active matrix organic light emitting diode (AMOLED) applications due to their high mobility, high transparency, and capability to realize integrated circuits over a large area on the same glass as the display.[1–5] Compared to conventional *a*-Si TFTs, *a*-IGZO TFTs have better device performance with the same advantages of a low manufacturing cost and a process flow compatible with conventional *a*-Si TFTs.[6,7]

Device stability is an important issue in real applications. It is reported that the stability of *a*-IGZO TFTs suffers from several factors, such as the adsorption of water/oxygen molecules,[8,9] the temperature effect,[10] the illumination effect, and the influence of operating bias.[11,12] During the normal working mode, one of the degradation mechanisms of *a*-IGZO TFTs is hot carrier stress. Previous research has reported that the hot carrier effect, resulting from the electrons near the drain region under the high electric field, causes the deterioration of drain current and field effect mobility.[13,14] Further, the environment surrounding the *a*-IGZO TFT also has a great impact on the electrical stability;[8–12] however, most studies have focused on the current-voltage (*I-V*) transfer characteristics to investigate the degradation mechanism after stress.[11,12] Because current transfer behaviors respond to the entire degradation region in the channels, the detailed region of deterioration in the channel after stress is somewhat difficult to examine. In this work, the effects of hot carrier stress are examined with *I-V* and capacitance voltage (*C-V*) measurements, which can further verify the damaged location and study the mechanism of hot carrier stress in *a*-IGZO TFTs. The depicted energy-band diagram of the *a*-IGZO TFTs along the channel length helps to identify the degradation location and mechanism.

Experimental

A schematic cross-section of the coplanar-type bottom-gate *a*-IGZO TFT examined here is depicted in Figure 1a. The patterned Ti/Al/Ti (50/200/50 nm) tri-layer structures were deposited by DC-sputtering as the gate electrode and then capped with 300-nm-thick plasma-enhanced chemical vapor deposition (PECVD)-derived silicon-oxide (SiO_2) gate dielectric. The source/drain electrodes were formed with DC-sputtered Ti/Al/Ti (50/200/50 nm) and then patterned in channel width/length dimensions (W/L) = 100 /11 μm. An active layer of 30-nm-thick *a*-IGZO film was deposited by a DC magnetron sputtering system at room temperature, using a target of In:Ga:Zn = 1: 1: 1 in atomic ratio. Finally, the devices were annealed in air at 330°C for two hours in an oven.[11]

DC voltages were applied to the devices to study electrical reliability. In order to execute hot carrier stress in *a*-IGZO TFTs, the applied gate bias must be larger than the threshold voltage and the drain bias must be high.[15] The stress condition was set at $V_D = 30$ V and $V_G = V_T + 10$ V while source terminal was grounded for 1000 sec. The applied biases of the drain, gate, and source terminals are illustrated in Figure 1. Variations in the electrical characteristics were monitored from the drain current-gate voltage (I_{DS}-V_G) and the capacitance-voltage (*C-V*) transfer characteristics. The electrical characteristics were measured in vacuum and in 760 torr oxygen ambience, respectively. The *I-V* curves and *C-V* curves were measured by an Agilent B1500 semiconductor parameter analyzer. Here, the normalized drain current (NI_{DS}) is defined as drain current/(width/length), i.e., I_{DS}/(W/L). In the *C-V* measurements, the gate-to-source capacitance (C_{GS}) and the gate-to-drain capacitance (C_{GD}) were measured at a frequency of 100 K Hz. For the C_{GS}-V_G measurement, capacitance-measurement-high (CMH) was applied to the gate electrode and capacitance-measurement-low (CML) was connected to source electrode with a floated drain. In contrast, the C_{GD}-V_G was measured with a floated source.

Results and Discussion

Figure 2 shows the NI_{DS}-V_G transfer characteristic curves of an *a*-IGZO TFT with 1 V drain voltage at initial and after 1000 sec of hot carrier stress in a vacuum environment. It can be seen that the device exhibits a slight degradation under hot carrier stress, where V_T increases with the evolution of stress time. The positive shift of

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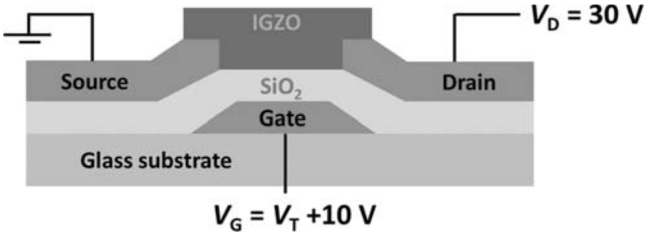

Figure 1. Schematic cross section of an *a*-IGZO TFT under hot carrier stress conditions.

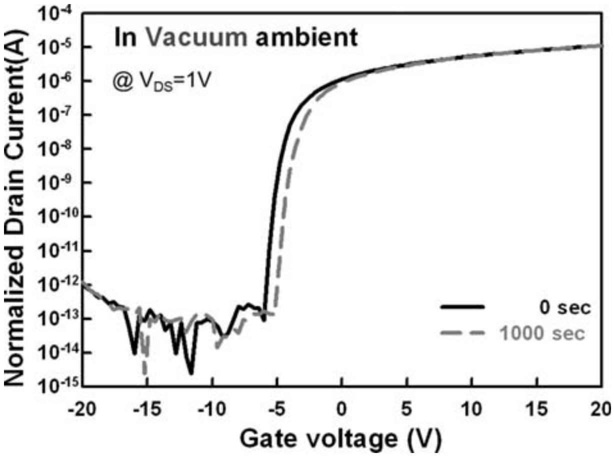

Figure 2. Normalized I_D-V_G transfer characteristics curves of *a*-IGZO TFTs with 1 V drain voltage under initial and after hot carrier stress in vacuum ambient.

the transfer characteristics may be ascribed to the electron trapping at the interface between the channel and gate dielectric or the defect creation within the *a*-IGZO channel material. The negligible variance of the subthreshold swing before and after hot carrier stress (SS_{before} = 0.396 V/dec, SS_{after} = 0.401 V/dec) indicates that the negative charge trapping at the channel/gate dielectric interface is the major origin of the positive threshold voltage shift.[11]

To further understand this phenomenon, the C_{GD}-V_G and the C_{GS}-V_G transfer characteristics before and after 1000 sec of hot carrier stress in a vacuum environment were measured in Figures 3a and 3b. Compared to that before hot carrier stress, the stressed C_{GD}-V_G curve exhibited two main changes; namely, the parallel shift in the positive direction and an increase in the capacitance value for the gate voltage just below the flatband voltage (V_{FB}). A previous study reported that the increase in the C_{GD} value during the lower gate voltage comes from the interface states near the drain region,[13] suggesting that a large drain voltage accelerates the electrons to move from the source terminal to the drain terminal and produce numerous traps in the *a*-IGZO film adjacent to the drain electrode by impact ionization. It can be observed from Figure 3b that the C_{GS}-V_G curve parallel shifts in the positive direction after hot carrier stress in vacuum ambient, which is consistent with the I_{DS}-V_G result in Figure 2. Hence, the creation of interface traps near the drain terminal and the electron trapping in the gate dielectric appeared after the hot carrier stress was conducted in the vacuum environment.

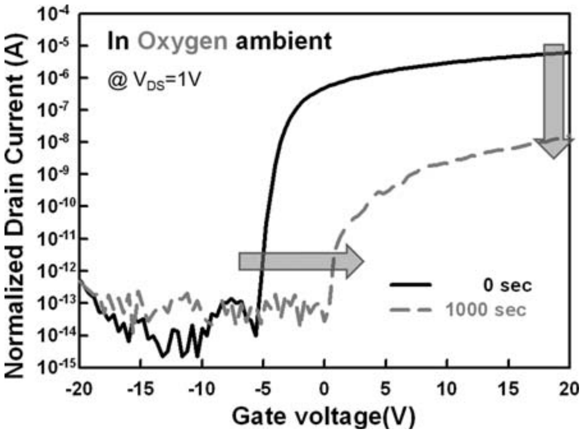

Figure 4. Normalized I_D-V_G transfer characteristics curves of *a*-IGZO TFTs with 1 V drain voltage under initial and after hot carrier stress in oxygen environment.

Early investigations have shown that the adsorption/desorption reaction of ambient oxygen molecules on the amorphous oxide surface has a great impact on the electrical characteristics of amorphous metal oxide TFTs, where the excess electron accumulation in the conducting channel region will be captured by the oxygen species from the ambient atmosphere, which then generates the negatively charged species (O_2^-) in the back-channel of amorphous oxide TFTs.[8,9] In order to further understand the influence of oxygen on electrical characteristics of *a*-IGZO TFTs, the hot carrier stress was also performed in a 760 torr oxygen-rich ambient environment.

Figure 4 shows the NI_{DS}-V_G transfer characteristics of an *a*-IGZO TFT with 1 *V* drain voltage before and after stress for 1000 sec in an oxygen-rich environment. As can be clearly seen, the device exhibits pronounced degradation after the same hot carrier stress condition, where V_T shifts to the positive direction and on-current is seriously degraded. It is well known that the oxygen molecules in the surrounding atmosphere will adsorb on the *a*-IGZO film by capturing electrons from the conduction band and exist in the form of O_2^-(ad).[16] Due to the charge transfer between the oxygen molecules and *a*-IGZO film, a reduction of the free carriers occurs, which results in the

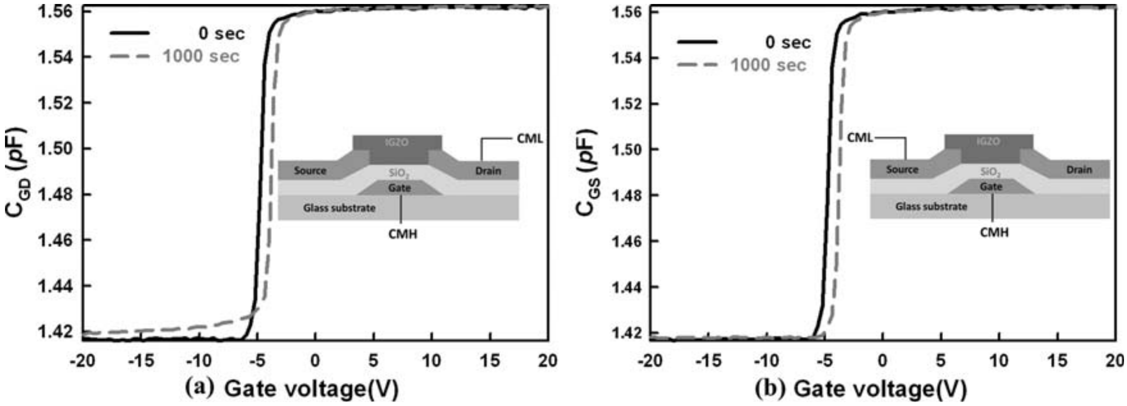

Figure 3. (a) C_{GD}-V_G and (b) C_{GS}-V_G transfer characteristics under initial and after hot carrier stress in vacuum ambient. The insets show their respective measurement methods.

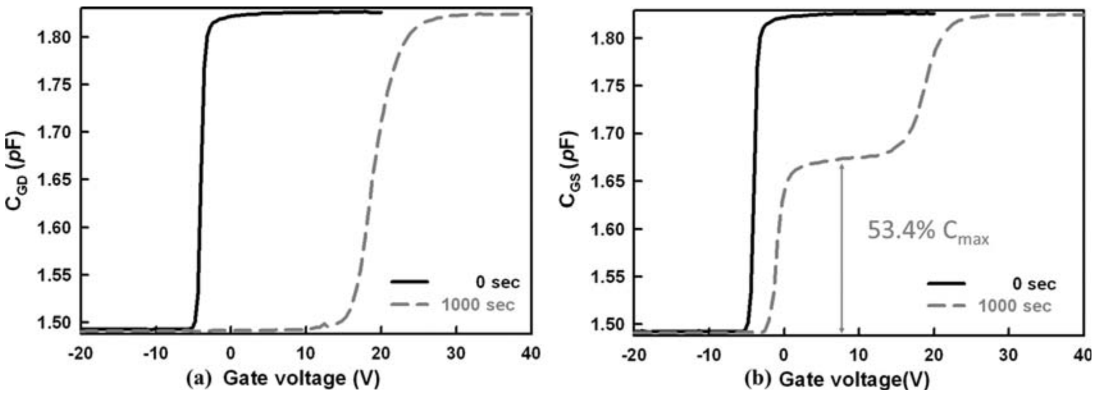

Figure 5. (a) C_{GD}-V_G and (b) C_{GS}-V_G transfer characteristics under initial and after hot carrier stress in oxygen environment.

increase of V_T. The interaction between the back-channel and surrounding atmosphere can be described as the following chemical reaction:

$$O_2\,(g) + e^- \rightarrow O_2^-(ad),\ K = [O_2^-]_{(ad)}/P_{O2}[n]$$

where K, $[O_2^-]_{(ad)}$, P_{O2}, and $[n]$ represent the chemical equilibrium constant, the concentration of the adsorbed oxygen molecules on *a*-IGZO film, the oxygen partial pressure, and the density of the electrons in the channel, respectively. Previous research identified the phenomenon of electric-field-induced oxygen adsorption on the *a*-IGZO surface under positive gate bias,[17] where an increase in the density of generated free electrons $[n]$ resulted in a positive V_T shift in the electrical characteristics of *a*-IGZO TFTs since the chemical equilibrium constant K does not vary at a fixed temperature. In addition, as positive bias is applied to the drain electrode, the adjacent active area of the drain terminal may attract more oxygen molecules absorbing on the *a*-IGZO surface, causing a significant reduction in the on-current. Therefore, the severe deterioration of electrical characteristics for *a*-IGZO TFTs after 1000 sec of hot carrier stress conducted in an oxygen-rich environment may be ascribed to the electric-field-induced oxygen adsorption on the back-channel layer and the adjacent channel area of the drain electrode, which leads to a positive threshold voltage shift and a noticeable reduction of on-current.

To further confirm the degradation mechanism, the C_{GD}-V_G and C_{GS}-V_G transfer characteristics under initial and after 1000 sec of stress in an oxygen-rich environment were measured, and are shown in Figures 5a and 5b, respectively. Figure 5a clearly shows a significant positive shift of about 20 V in the C_{GD}-V_G curve, while the increase in the capacitance value with the gate voltage below the V_{FB} is eliminated, which may be suppressed by the oxygen passivation from the surrounding oxygen atmosphere. The oxygen adsorption in the surrounding atmosphere affects the characteristics via the charge transfer between the *a*-IGZO film and the oxygen molecules.[16] The absorbing oxygen molecules on the back-channel lead to the reduction of free carriers in the active layer of the *a*-IGZO TFT. When hot carrier stress is performed, the generated electrons near the drain terminal become influenced by a large positive electric field, causing the electrons to transport from the pinch-off region to the drain terminal, as depicted in Figure 6a. These electrons move in possibly random directions due to the drain-side energy-band lowering and are further captured by the surrounding oxygen molecules, resulting in a greater electric-field-induced oxygen adsorption on the *a*-IGZO film near the drain terminal. Hence, the origin of the positive shift of the C_{GD}-V_G curve is the oxygen adsorption which captures the electrons and reduces the electron concentration. Nevertheless, the shift value of the threshold voltage obtained from the I_{DS}-V_G result does not correspond to the result acquired from the C_{GD}-V_G curve. Furthermore, the C_{GS}-V_G exhibited the anomalous behavior of a two-step turn-on after hot carrier stress, as shown in Figure 5b. The flatband voltage of the first-step of the C_{GS}-V_G curve is consistent with the threshold voltage of the I_{DS}-V_G curve, while the second-step behavior is similar to the C_{GD}-V_G curve. Therefore, the main reasons for the two-step turn-on behavior might be the contributions of electron trapping and oxygen adsorption near the source and drain terminals, respectively.

The solid line in Fig. 6b shows the energy-band diagram of the *a*-IGZO TFT along the channel length without oxygen adsorption on the *a*-IGZO surface under the flatband condition. As discussed above, the hot carrier stress causes the electron trapping in the whole oxide layer, further raising the source barrier. In addition, the oxygen adsorption on the *a*-IGZO surface, especially near the drain terminal, leads to a reduction of the electron concentration, also causing the Fermi-level to be lowered, indicating that the drain barrier is further raised. The dashed blue line in Figure 6b represents the modulated energy-band diagram after the lowering of Fermi-level induced by the electron trapping and the oxygen adsorption, especially adjacent to the

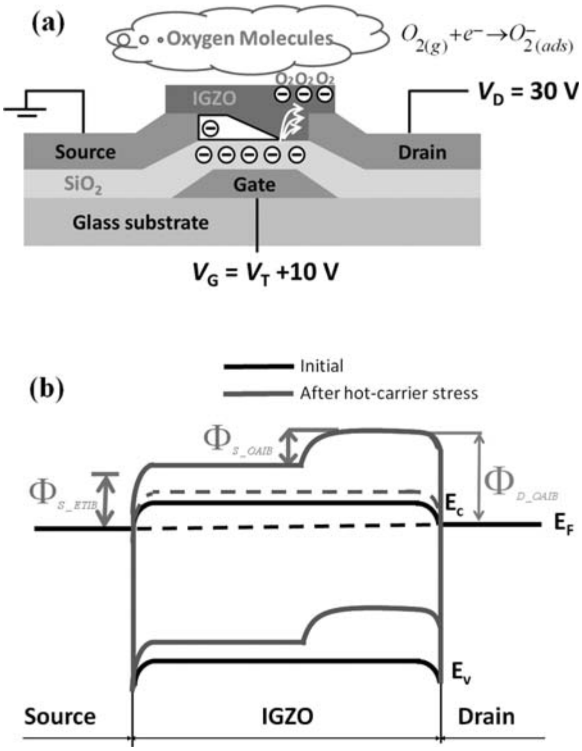

Figure 6. (a) Schematic diagram of electron transport behavior and electron adsorbing reaction under hot carrier stress in oxygen environment for an *a*-IGZO TFT. (b) The energy-band diagram under initial (solid line) and after hot carrier stress (dashed blue line) in oxygen environment.

drain terminal. The captured electrons raise the energy-band upward and further induce additional energy barriers at the source and drain terminals, where the barrier of the drain side is higher than the source side due to the additional applied drain voltage.

In the C_{GD}-V_G measurement, the detected electrons originated from the drain terminal because the source terminal was floated, and these electrons further faced a large drain barrier originating from the oxygen-adsorption-induced-barrier (Φ_{D_OAIB}), as shown in Figure 6b. The free electrons provided from the drain terminal should overcome the Φ_{D_OAIB} when the gate terminal is swept to the positive voltage, which results in carrier injection into the whole channel and the device turn-on phenomenon. Accordingly, the V_T of an *a*-IGZO TFT, obtained from the C_{GD}-V_G curve, was delayed to about 20 V when compared with the I_{DS}-V_G curve, because of the higher barrier height (Φ_{D_OAIB}) near the drain terminal. This implies that only one of the turn-on behavior steps is observed in the C_{GD}-V_G curve, as seen in Figure 5a. In contrast, the C_{GS}-V_G curve exhibited a two-step turn-on behavior in Figure 5b and the turn-on threshold voltage in the first-step was consistent with the V_T extracted from the NI_{DS}-V_G result in Figure 4. This intriguing phenomenon can be explained by the modulated energy-band diagram (the dashed blue line) in Figure 6b. In the C_{GS}-V_G measurement, electrons were only provided from the source terminal, and experienced different source barriers, those of the electron-trapping-induced-barrier (Φ_{S_ETIB}) and the oxygen-adsorption-induced-barrier (Φ_{S_OAIB}). At a lower gate voltage, these free electrons easily surmount the Φ_{S_ETIB}, and start to move into the channel. However, due to a great quantity of the electric-field-induced oxygen adsorption near the drain terminal, the energy band raises upward even further, and causes the second source barrier (Φ_{S_OAIB}). The Φ_{S_OAIB} impedes the fluid motion of free electrons to the drain side during the C_{GS}-V_G measurement. As a result, a larger gate bias is needed to suppress theΦ_{S_OAIB}.

Based on the previous energy-band explanation, we speculate that the *a*-IGZO TFT should display a two-step turn-on behavior. This speculation is consistent with the result shown in Figure 5b, where the first step of the turn-on behavior occurred at a gate voltage of about 0 V, the second step occurring at about 20 V. Accordingly, the source barriers (Φ_{S_ETIB} andΦ_{S_OAIB}) produced by the electron trapping and electric-field-induced oxygen adsorption will be lowered with an increasing applied gate voltage. Then the electrons provided by the source terminal can flow from the source side to the drain side freely. Therefore, the result of the C_{GS}-V_G measurement further confirms that the hot carrier stress conducted in oxygen-rich ambient causes the oxygen molecules to adsorb on the *a*-IGZO film near the drain terminal.

Furthermore, the length of the electric-field-induced oxygen adsorbing on an a-IZGO film surface can be estimated from the C_{GS}-V_G measurement if the channel width is constant after the hot carrier stress. As seen in Figure 5b, the maximum capacitance value of the first stage is 53.4% of the measured maximum capacitance, where the origin of the capacitance is the electron trapping and the natural capacitance of the silicon oxide.[18] The remaining capacitance is needed to surmount the oxygen adsorption-induced barrier near the drain terminal. Hence, the drain electric-field-induced oxygen adsorbing length can be calculated as 5.1 μm, as plotted in Figure 7.

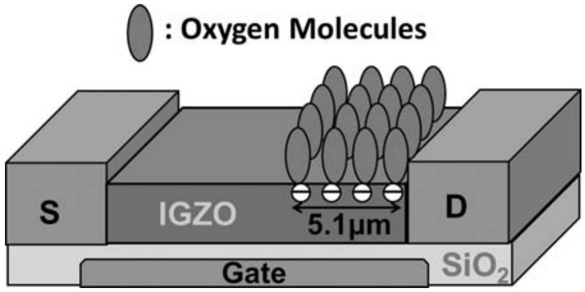

Figure 7. Schematic diagram of estimated oxygen adsorbing length induced by large drain voltage after the hot carrier stress in oxygen environment.

Conclusions

This work investigates the environment-dependent degradation of *a*-IGZO TFTs under hot carrier stress using the *I-V* and *C-V* measurements, which can verify the degradation location in the *a*-IGZO channel. When hot carrier stress was conducted in vacuum ambient, the current and capacitance transfer curves exhibited positive shifts due to electron trapping along the whole gate dielectric. An increase in capacitance value at lower gate voltage obtained from the C_{GD} measurement is due to the interface state creation. We also observed that after hot carrier stress, the threshold voltage shifts caused by electron trapping in the gate dielectric layer in an oxygen-rich environment were more serious than in a vacuum environment, regardless of the *I-V* and *C-V* results. In addition, an anomalous two-step turn-on behavior appeared in the C_{GS}-V_G curve, due to a large amount of oxygen adsorption at the drain terminal. A schematic energy-band diagram model was proposed to explain the anomalous *C-V* behavior, and proposed that the raising of the source/drain barrier originates from the electron trapping in the whole gate dielectric, with the oxygen adsorption further raising the energy-band, especially at the drain terminal. Accordingly, the carriers generated from the source terminal face two barriers, Φ_{S_ETIB} andΦ_{S_OAIB}, resulting in a two-step turn-on behavior in the C_{GS}-V_G curve. Nevertheless, the electrons provided by drain terminal face only a large barrier Φ_D such that the C_{GD}-V_G curve exhibits a one-step turn-on behavior and larger turn-on voltage. These findings provide important information for further studies in ambient environments and of electrical stability of *a*-IGZO TFTs, where the electron trapping in the gate dielectric and drain electric-field-induced oxygen adsorption are the primary issues in the hot carrier stress operation.

Acknowledgments

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