Oxide Thinning and Structure Scaling Down Effect of Low-Temperature Poly-Si Thin-Film Transistors

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***Abstract*—In this paper, the gate oxide thickness, and the channel length and width of low-temperature poly-Si thin-film transistors (LTPS-TFTs) have been comprehensively studied. The scaling down of gate oxide thickness from 50 to 20 nm significantly improves the subthreshold swing (S.S.) of LTPS-TFTs from 1.797 V/decade to 0.780 V/decade and the threshold voltage $V_{\rm TH}$ from 10.87 V to 5.00 V. Moreover, the threshold voltage $V_{\rm TH}$ roll-off is also improved with the scaling down of gate oxide thickness due to gate capacitance density enhancement. The channel length scaling down also shows significant subthreshold swing S.S. improvement due to a decreasing of the channel grain boundary trap density N_t. However, the scaling down of channel length also increases the series resistance effect, resulting in the degradation of the field-effect mobility $\mu_{\rm FE}$. Therefore, the channel length dependence of field-effect mobility $\mu_{\rm FE}$ is slightly different with different channel width due to the competition of channel grain boundary trap density effect and series resistance effect.**

***Index Terms*—Gate oxide thickness, low-temperature poly-Si thin-film transistors (LTPS-TFTs), scaling down.**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been used for active-matrix liquid crystal displays (AMLCDs) on glass substrates as pixel and driving integrated circuits instead of amorphous silicon [1]–[8]. This is because the field-effect mobility $\mu_{\rm EF}$ in polycrystalline silicon is significantly higher (by two orders of magnitude) than that in amorphous silicon [6], so that CMOS devices with reasonably high drive currents can be achieved in polycrystalline silicon. Recently, the topic of system-on-panel (SOP) is attracting much attention. Therefore, high-performance TFTs with high driving current, low gate leakage current, low threshold voltage $V_{\rm TH}$ and subthreshold swing S.S. are required urgently for high-speed display driving circuits [9], [10]. Increasing the gate capacitance density is a direct and simple method of improving the performance and specifically the driving current of LTPS-TFTs. Therefore, a comprehensive study of the effect of reducing gate oxide thickness in LTPS-TFTs is important for further development. Here, we investigate the gate oxide thickness scaling impacts of LTPS-TFTs with different channel length L_g and width W on the electrical behavior of threshold voltage $V_{\rm TH}$, field-effect mobility $\mu_{\rm FE}$, and subthreshold swing S.S.

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II. Experimental Procedure

The fabrication of devices was started by depositing an undoped amorphous Si (α-Si) layer 55-nm at 550 °C in a low-pressure chemical vapor deposition (LPCVD) system on Si wafers capped with a 500-nm thick thermal oxide layer. Then, the α-Si layer was recrystallized by a solid-phase-crystallization (SPC) process in furnace at 600 °C for 24 h in a N_2 ambient. After the crystallization of the channel film, the active region was patterned by dry etching. Then, three thicknesses of gate oxide 20, 32, and 50 nm were deposited by plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C. 250-nm *in situ* N^+ doped α-Si is deposited by LPCVD at 550 °C as the gate electrode. After gate stack patterning, the gate and source/drain regions are implanted with phosphorus (15 keV at 5×10^{15} cm^{-2}) and activated at 600 °C for 24 h annealing in a N_2 ambient. A 500-nm PECVD oxide is deposited for the passivation layer. After the patterning of contact holes, aluminum was deposited by thermal evaporation system and patterned as the probe pads to complete the TFT devices. The grain size of the polycrystalline Si channel is about 250–300 nm [9]. Generally, LTPS-TFT with SPC process has many grain boundaries within the poly-Si channel, resulting in many electrical traps exist. These traps would capture carriers to create potential barriers, resulting in poor subthreshold swing S.S., higher threshold voltage $V_{\rm TH}$, lower field-effect mobility $\mu_{\rm FE}$ and poor performance. Therefore, hydrogenation process is usually used to passivate these traps to improve the electrical behavior of LTPS-TFTs [11]. In order to study the intrinsic electrical property of LTPS-TFTs, there is no any defect passivation process in our fabrication of LTPS-TFTs.

The threshold voltage $V_{\rm TH}$ is defined as V_G at which I_D reaches 100 nA $\times$ (W/L_g) and $V_D = 1$ V. The field-effect mobility $\mu_{\rm FE}$ is extracted from the maximum transconductance G_m.

III. Results and Discussion

Fig. 1 shows the transfer curves (I_D–V_G) and field-effect mobility $\mu_{\rm FE}$ of LTPS-TFTs with different gate oxide thickness. The subthreshold swing S.S. is significantly improved from 1.797 V/decade to 0.780 V/decade when the gate oxide thickness is scaled from 50 to 20 nm. The subthreshold swing S.S. should be strongly related to the gate capacitance density $C_{\rm ox}$ and interface states $D_{\rm it}$ according to the Dimitriadis model [12]

$$\text{S.S.} = \left[\frac{qN_{\rm it}}{C_{\rm ox}} + 1\right]\frac{KT}{q}\ln 10. \tag{1}$$

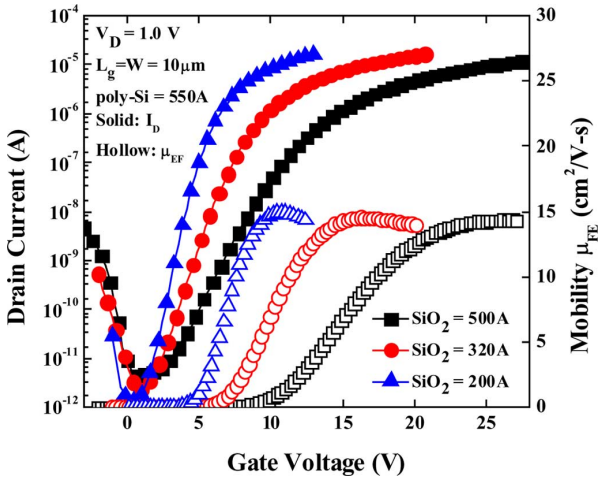

Fig. 1. Transfer curve (I_D–V_G) and field-effect mobility $\mu_{\rm FE}$ of LTPS-TFTs with three gate oxide thickness 50, 32, and 20 nm.

TABLE I
IMPORTANT DEVICE PARAMETERS OF LTPS-TFTS WITH DIFFERENT OXIDE THICKNESS $t_{\rm ox}$, 55-NM CHANNEL FILM THICKNESS, $W/L_g = 10\,\mu{\rm m}/10\,\mu{\rm m}$

t_{ox} (nm)	V_{TH} (V)	S.S. (V/dec.)	μ_{FE} (cm^2/V-s)	D_{it} (cm^{-2})
20	5.00	0.780	14.91	1.30×10^{13}
32	7.35	1.180	14.54	1.27×10^{13}
50	10.87	1.797	14.33	1.26×10^{13}

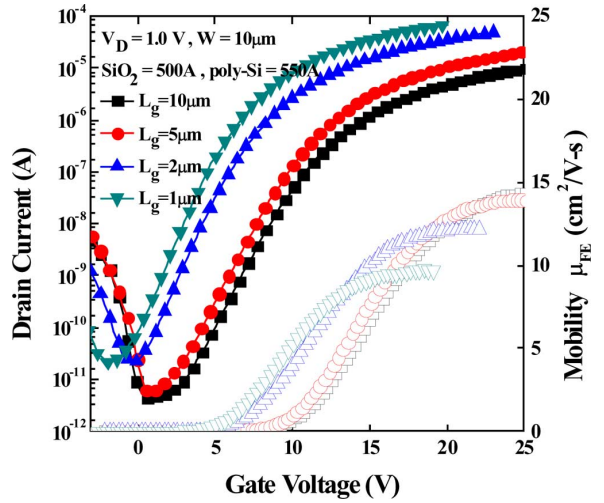

Fig. 2. Transfer curve (I_D–V_G) and field-effect mobility $\mu_{\rm FE}$ of LTPS-TFTs with 50-nm gate oxide thickness, channel width $W = 10\,\mu$m and four channel length $L_g = 10,\ 2,$ and $1\,\mu$m.

The extracted interface states $D_{\rm it}$ and other important parameters are listed in the Table I. It shows that the interface states $D_{\rm it}$ of LTPS-TFTs with different gate oxide thickness are the same, indicating the subthreshold swing S.S. improvement is completely attributed to the increase in the gate capacitance density $C_{\rm ox}$. It also indicates the oxide/Si interface quality of LTPS-TFTs with different gate oxide thickness is the same. In addition, the field-effect mobility $\mu_{\rm FE}$ of LTPS-TFTs with different gate oxide thickness are comparable, indicating the

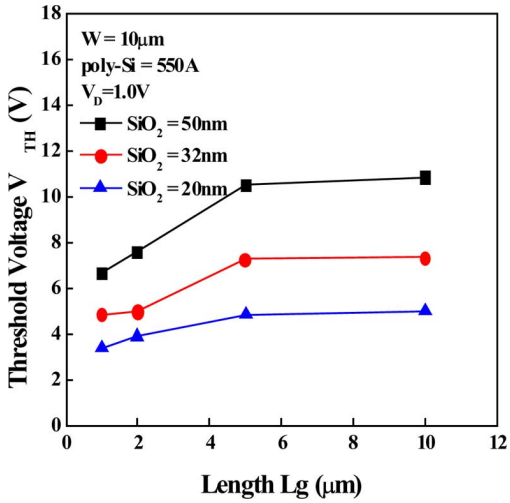

Fig. 3. Threshold voltage $V_{\rm TH}$ versus channel length L_g of LTPS-TFTs with three gate oxide thickness 50, 32, and 20 nm.

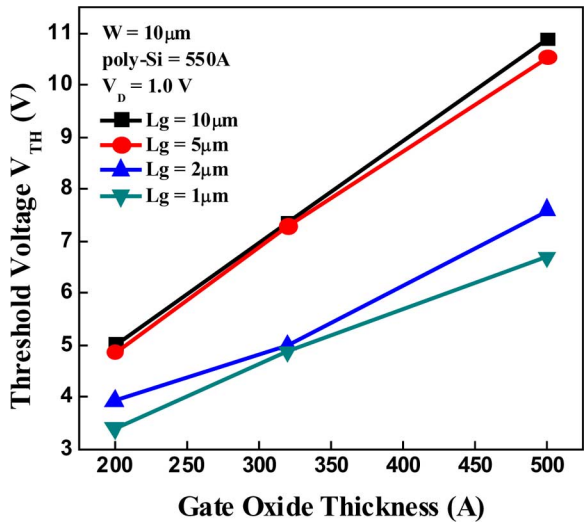

Fig. 4. Threshold voltage $V_{\rm TH}$ versus gate oxide thickness of LTPS-TFTs with four channel length $L_g = 10,\ 5,\ 2,$ and $1\,\mu$m.

field-effect mobility $\mu_{\rm FE}$ is less dependent on gate capacitance density $C_{\rm ox}$ if the oxide–Si interface and channel film quality is the same.

Fig. 2 shows the transfer curves of LTPS-TFTs with different channel length L_g. Significant threshold voltage $V_{\rm TH}$ roll-off is observed, as shown in Fig. 3, and reducing the gate oxide thickness from 50 to 20 nm enhances the control afforded by the gate, thereby improving the threshold voltage $V_{\rm TH}$ roll-off. Fig. 4 shows the gate oxide thickness dependence of threshold voltage $V_{\rm TH}$, indicating that the threshold voltage $V_{\rm TH}$ is almost linearly proportional to oxide thickness whether the channel length is long or short.

In addition to threshold voltage $V_{\rm TH}$ behavior, the channel lengthL_g dependence of field-effect mobility $\mu_{\rm FE}$ and subthreshold swing S.S. are also shown in Fig. 5. The reduction in subthreshold swing S.S. with decrease of the channel length L_g is due to the decreasing of channel grain boundary trap density N_t when the channel length L_g is decreasing, resulting in fewer surface interface states $D_{\rm it}$. The channel grain boundary trap

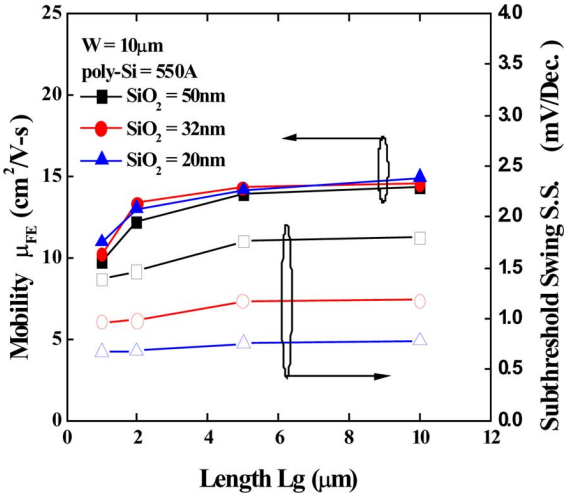

Fig. 5. Channel length L_g dependence of field-effect mobility $\mu_{\rm FE}$ and subthreshold swing S.S of LTPS-TFTs with channel width $W = 10$ μm and three gate oxide thickness 50, 32, and 20 nm.

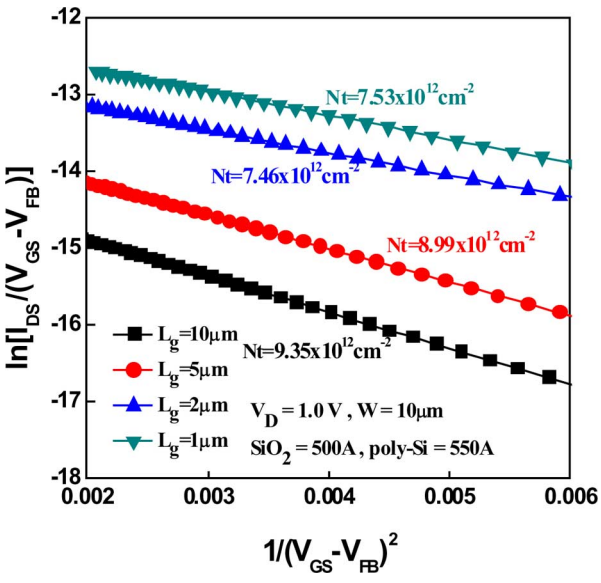

Fig. 6. Plot of $\ln[I_{\rm DS}/(V_{\rm GS}-V_{\rm FB})]$ versus $1/(V_{\rm GS}-V_{\rm FB})^2$ curves of LTPS-TFTs at $V_{\rm DS} = 1.0$ V and high $V_{\rm GS}$ with channel width $W = 10$ μm and four channel length $L_g = 10,\ 5,\ 2,$ and 1 μm.

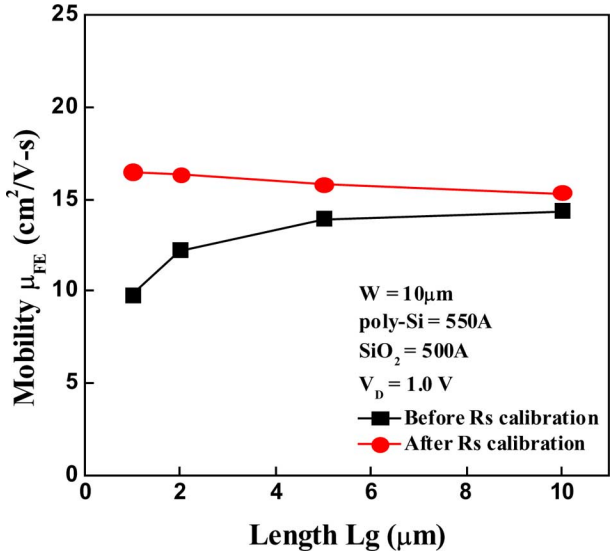

Fig. 7. Channel length L_g dependence of field-effect mobility $\mu_{\rm FE}$ of LTPS-TFTs with channel width $W = 10$ μm before and after series resistance R_s calibration.

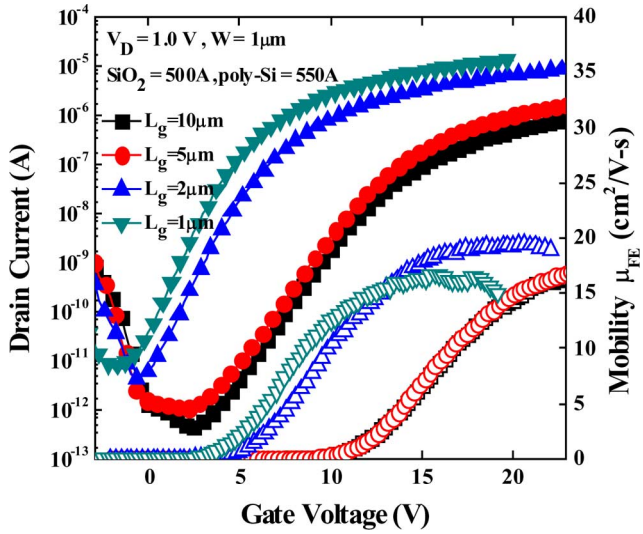

Fig. 8. Transfer curve (I_D–V_G) and field-effect mobility $\mu_{\rm FE}$ of LTPS-TFTs with 50 nm gate oxide thickness, channel width $W = 1$ μm and four channel length $L_g = 10,\ 5,\ 2,$ and 1 μm.

density N_t of LTPS-TFTs with different channel length L_g are extracted from the plot of $\ln\ [I_{\rm DS}/(V_{\rm GS} - V_{\rm FB})]$ versus $1/(V_{\rm GS} - V_{\rm FB})^2$ curves at $V_{\rm DS} = 1$ V and high $V_{\rm GS}$ [13], [14], as shown in Fig. 6. When the channel length L_g or width W is much larger than the grain size, the average grain boundary density is fairly constant, resulting in less device dimension dependence of electrical behavior of LTPS-TFTs. As the device dimension is reduced the number of grain boundaries in the channel becomes small, and therefore the varying number of grain boundaries between devices becomes significant, resulting in greater variation in device characteristics. Fig. 5 also shows that the field-effect mobility $\mu_{\rm FE}$ is reduced when the channel length L_g is decreased. With the reduction of channel length L_g, the grain boundary trap density N_t would decrease, and the series resistance R_s effect would be more serious [15], [16]. A reduced grain boundary density could improve the field-effect mobility $\mu_{\rm FE}$ and subthreshold swing S.S. due to a reduced trap density and less carrier scattering in the conduction channel. However, the series resistance R_s effect would lead to less drain voltage drop in the conduction channel, resulting in less drain current and lower field-effect mobility $\mu_{\rm FE}$. Therefore, the effect of the grain boundary trap density N_t decreasing and the series resistance effect are in competition when the channel length L_g is reduced. In the subthreshold region, a small drain current would not lead to a significant reduction in actual voltage across the channel due to the series resistance, and the grain boundary trap density N_t decrease effect could improve the subthreshold swing S.S. as the channel length L_g is reduced. However, for a high driving current, the series resistance R_s effect would significantly degrade the field-effect mobility $\mu_{\rm FE}$ as the scaling down of channel length L_g even the grain boundary trap density N_t

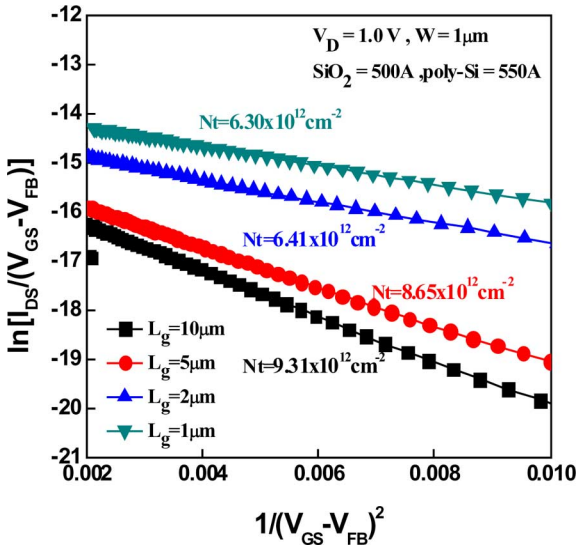

Fig. 9. Plot of $\ln[I_{\rm DS}/(V_{\rm GS}-V_{\rm FB})]$ versus $1/(V_{\rm GS}-V_{\rm FB})^2$ curves of LTPS-TFTs at $V_{\rm DS}=1.0$ V and high $V_{\rm GS}$ with channel width $W=1$ μm and four channel length $L_g=10,\ 5,\ 2,$ and 1 μm.

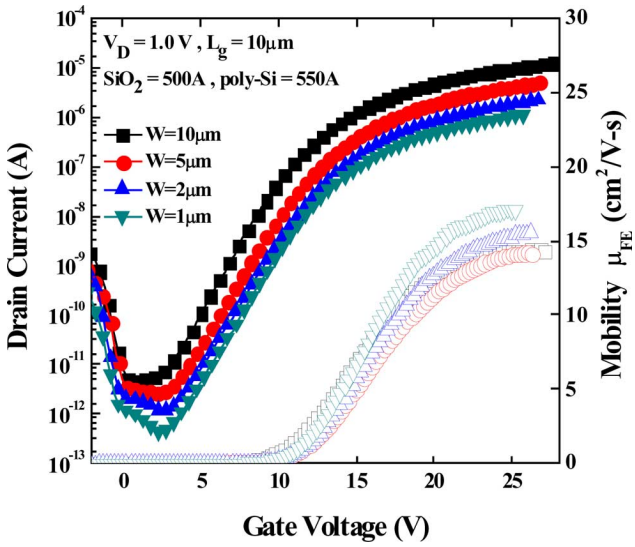

Fig. 11. Transfer curve (I_D-V_G) and field-effect mobility $\mu_{\rm FE}$ of LTPS-TFTs with 50-nm gate oxide thickness, channel length $L_g=10$ μm and four channel width $L_g=10,\ 5,\ 2,$ and 1 μm.

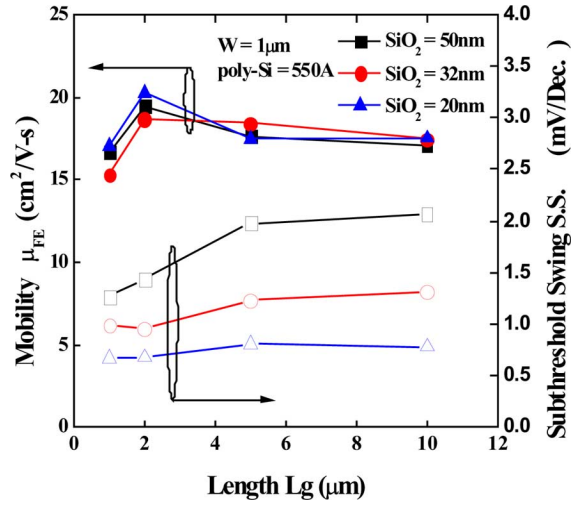

Fig. 10. Channel length L_g dependence of field-effect mobility $\mu_{\rm FE}$ and subthreshold swing S.S of LTPS-TFTs with channel width $W=1$ μm and three gate oxide thickness 50, 32, and 20 nm.

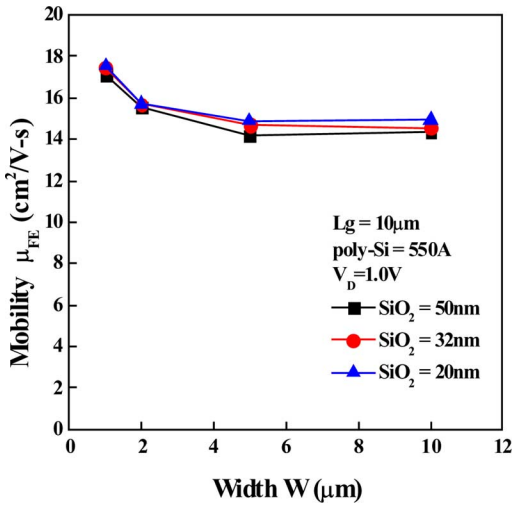

Fig. 12. Field-effect mobility $\mu_{\rm FE}$ versus channel width W of LTPS-TFTs with three gate oxide thickness 50, 32, and 20 nm.

decreased. In order to estimate the series resistance effect of LTPS-TFTs, the modified field-effect mobility $\mu'_{\rm FE}$ is defined as follows [17]:

$$I_D=\frac{W}{L}C_{\rm ox}\mu_{\rm eff}(V_g-V_{TH})V_D \tag{2}$$

$$I_D=\frac{W}{L}C_{\rm ox}\mu'_{\rm eff}(V_g-V_{TH})V'_D \tag{3}$$

$$V'_D=V_D-I_D\times R_s \tag{4}$$

$$\mu'_{\rm eff}=\mu_{\rm eff}\times\frac{V_D}{V_D-I_D\times R_s} \tag{5}$$

where V_D is the total applied voltage. The voltage drop should occur in the series resistance and conductive channel of TFTs. V'_D is thus the real applied voltage across the channel of TFTs. About 6.1 kΩ series resistance of device is extracted from drain current relation of gate voltage V_g and channel length L_g [17]. The modified field-effect mobility $\mu'_{\rm FE}$ with and without series resistance R_s calibration is shown in Fig. 7. It shows that the modified field-effect mobility $\mu'_{\rm FE}$ is increased with the reduction in channel length L_g, and the field-effect mobility $\mu_{\rm FE}$ without R_s calibration shows the 6.1 kΩ series resistance would result in series $\mu_{\rm FE}$ degradation. As for the narrower channel width $W=1$ μm, the transfer curves of LTPS-TFTs with different channel L_g are shown in Fig. 8. Comparing to wide channel width $W=10$ μm, the grain boundary trap density N_t decreasing effect is more significant as shown in Fig. 9, resulting in that the field-effect mobility $\mu_{\rm FE}$ exhibiting a slight increase first before it decreases with the reduction of channel length L_g, as shown in Fig. 10. Moreover, the subthreshold swing improvement ΔS.S. from channel length $L_g=10$ μm to 1 μm is also enhanced from $\Delta\text{S.S.}=0.4\,\text{V/decade}$ to 0.8 V/decade with the reduction of channel width from $W=10$ μm to 1 μm. Fig. 11 shows the transfer curves of LTPS-TFTs with different channel width. The channel width dependence of field-effect mobility $\mu_{\rm FE}$ is shown in Fig. 12. It shows that the field-effect mobility $\mu_{\rm FE}$ is independent of gate oxide thickness and increases with the reduction in the channel width. As mentioned above, the

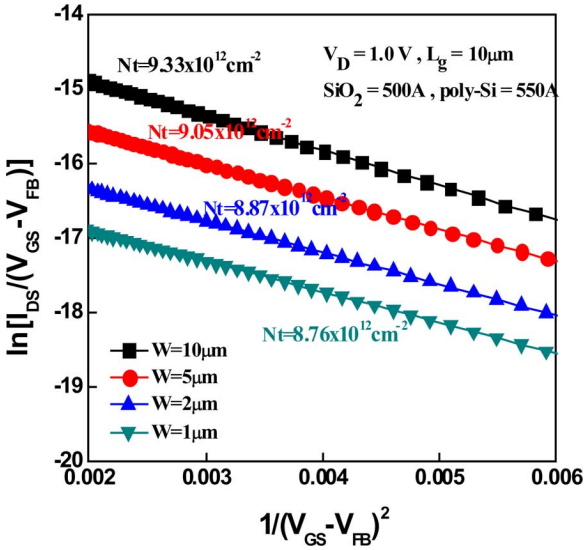

Fig. 13. Plot of $\ln[I_{\rm DS}/(V_{\rm GS}-V_{\rm FB})]$ versus $1/(V_{\rm GS}-V_{\rm FB})^2$ curves of LTPS-TFTs at $V_{\rm DS}=1.0$ V and high $V_{\rm GS}$ with channel length $L_g=10\ \mu$m and four channel width $L_g=10,\ 5,\ 2,$ and $1\ \mu$m.

channel width reduction can decrease the grain boundary trap density N_t in the channel film, as shown in Fig. 13, resulting in higher field-effect mobility $\mu_{\rm FE}$. Finally, the impacts of reducing gate oxide thickness, channel length L_g and width on LTPS-TFTs are all extracted simultaneously.

IV. Conclusion

A comprehensive study of scaling down effects of LTPS-TFTs with various gate oxide thicknesses, channel length L_g and width W are studied simultaneously. Gate oxide thickness strongly affects the electrical performance of LTPS-TFTs, including threshold voltage $V_{\rm TH}$, subthreshold swing S.S., channel length L_g dependence of field-effect mobility $\mu_{\rm FE}$ and subthreshold swing S.S. The thin gate oxide thickness of LTPS-TFTs results in the most stable and superior electrical behavior. In addition, the competition of channel grain boundary trap density effect and series resistance effect is also observed; the different channel width of LTPS-TFTs exhibit slightly different channel length dependence of field-effect mobility $\mu_{\rm FE}$.

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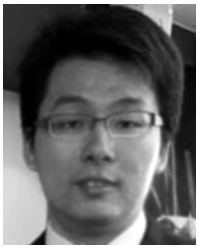

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