Low Frequency Noise in Nanoscale pMOSFETs with Strain Induced Mobility Enhancement and Dynamic Body Biases

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***Abstract* —Local strain effect on low frequency noise (LFN) of pMOSFETs with gate length down to 60 nm was investigated in this paper. Novel and interesting results were identified from the pMOSFETs adopting embedded SiGe (e-SiGe) in source/drain for uni-axial compressive stress. This local compressive strain can realize significant mobility enhancement and desired current boost in nanoscale pMOSFETs. However, the dramatic increase of LFN emerges as a penalty traded off with mobility enhancement. The escalated LFN may become a critical killer to analog and RF circuits. Forward body biases (FBB) can improve the effective mobility (μ_{eff}) and reduce LFN attributed to reduced normal field (E_{eff}). However, the benefit from FBB becomes insignificant in strained pMOSFETs with sub-100 nm gate length.**

***Index Terms*–Low frequency noise, strain, mobility, pMOSFET**

I. INTRODUCTION

Strain engineering has evolved as an indispensable technology in high speed CMOS platform at 65 nm node and beyond [1]. Both local and global strain engineering can realize an effective mobility enhancement and current boost. The gate speed improvement driven by the mobility and current indeed makes a contribution to f_T and f_{max}, the key parameters determining RF and analog circuits performance [2-3]. However, the potential impact from the strain on noise, particularly the low frequency noise (LFN) or namely flicker noise brings a critical challenge to both RF and analog circuits/systems design. Consequently, the strain engineering effect on noise becomes an important subject and attracts increasing research effort in recent years. Many literatures were published with a discussion on strain effect on LFN [4-6]. Unfortunately, there exist lot of debates in the experimental results and proposed mechanisms. Maeda *et al*. reported flicker noise increase in pMOSFETs under both compressive and tensile stress, namely bi-directional noise degradation [5]. Stress induced excess traps and dipoles were proposed as the possible cause responsible for flicker noise degradation. Ueno *et al*. published results just in contradiction to the previous one [6]. They claimed improved 1/f noise in pMOSFEs with e-SiGe for local compressive stress, and controverted Maeda's results as inclusive owing to side effects other than stress. Unfortunately, there remain couple of open questions deserving an extensive investigation, such as the excess noise introduced by Ge-implant for stress relaxation, the abnormally large LFN revealed in pMOS compared to nMOS with stress free liner, and number fluctuation model assumed for pMOSFETs.

Meanwhile, the lower supply voltage for matching device scaling and lower active power generally degrades the headroom for signal to noise margin (SNM) and raises more crucial demand on low noise design. Dynamic threshold voltage CMOS (DTMOS) technique is considered the most promising method to facilitate low power design in nanoscale CMOS platform, and dynamic body biases scheme is an effective way to realize DTMOS [7-8]. As a result, strain engineering cooperating with dynamic body biases is proposed as a viable approach in nanoscale CMOS for high speed, low power, and low noise design.

In this paper, pMOSFETs adopting e-SiGe S/D for uni-axial compressive strain were fabricated for mobility enhancement. A comprehensive characterization was carried out to investigate the local strain effect on mobility, current, short channel integrity, and most importantly LFN. Dynamic body biases scheme consisting of forward body bias (FBB), zero body bias (ZBB), and reverse body bias (RBB) was employed to explore the influence on LFN. Through the extensive characterization and theoretical analysis, the mechanism responsible for LFN in pMOSFETs can be extracted, and the results suggest that mobility fluctuation model plays a dominant role.

II. DEVICE FABRICATION AND CHARACTERIZATION

Strained pMOSFETs adopting e-SiGe in S/D for local compressive strain were fabricated in 65 nm process. The standard devices free from strain engineering, namely control pMOSFETs were fabricated simultaneously as the reference. Four-terminal device layout was implemented with 4 individual pads for 4 electrodes (G/D/S/B) to enable a freedom of body biases. The gate width (W) was fixed at 10μm while the gate lengths drawn on layout (L_{drawn}) varied in a wide range from 10 μm to 0.08 μm. An etching bias of 0.02 μm leads to physical gate length $L_g=L_{drawn}$-0.02 μm, i.e. the minimal L_g down to 0.06 μm (60 nm).

The drain current noise was measured by LFN system consisting of Agilent dynamic signal analyzer (DSA 35670) and low noise amplifier (LNA SR570). The measured noise

was represented as power spectral density (PSD) in frequency domain, denoted as S_{Id}. The LFN measurement generally covers a wide frequency range from 10 to 100 KHz.

III. RESULTS AND DISCUSSION

A. Local Strain Effect on Current and Mobility

Firstly, local strain effect on current drivability was investigated on 60 nm pMOSFETs. Fig. 1(a) and (b) present the measured drain current I_{DS} and transconductance G_m under varying V_{GS}. Note that gate overdrive $V_{GT}= V_{GS}–V_T$ was specified to replace V_{GS} for eliminating V_T offset due to strain engineering. The comparison between strained and control devices reveals a remarkable increase of both I_{DS} and G_m in the 60 nm devices, due to the uni-axial compressive strain. The improvement can reach around 80% increase in I_{DS} and maximum G_m. The experimental proves the local strain an effective technique for performance boost in nanoscale devices.

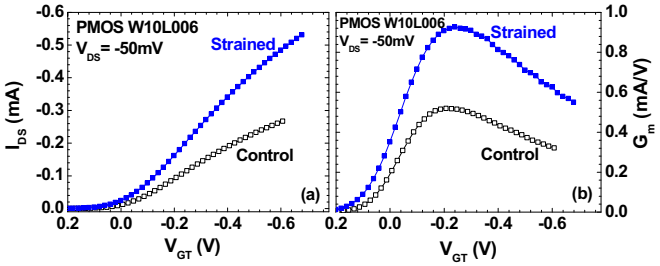

Fig. 1 (a) Drain current I_{DS} vs. V_{GT} (b) transconductance G_m vs. V_{GT} measured in linear region at V_{DS}=-50mV and varying V_{GS} (V_{GT}=V_{GS}-V_T) for control and strained pMOSFETs with L_g=60 nm.

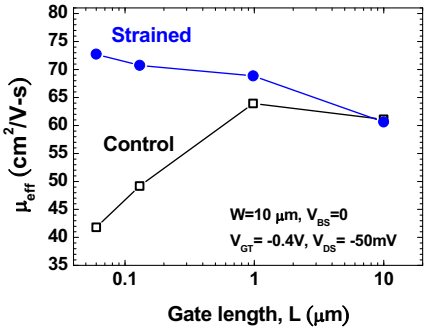

Fig. 2 The effective mobility μ_{eff} extracted from linear I-V characteristics for strained and control pMOSFETs over various gate lengths, L_g=10~0.06 μm.

Fig. 2 exhibits the effective mobility μ_{eff} extracted from linear I-V characteristics. Interestingly, the extracted μ_{eff} indicates a significant dependence on L_g for both strained and control pMOSFETs but going the opposite directions. For strained pMOS, the shorter L_g gains higher μ_{eff} whereas for control pMOS, the shorter L_g suffers degradation in μ_{eff}. As a result, the μ_{eff} enhancement realized by strained over control pMOSFETs can attain around 74%, which exactly contributes the improvement of I_{DS} and G_m. The μ_{eff} enhancement realized in strained pMOS with sufficiently short L_g manifests the local compressive strain effect from e-SiGe S/D. On the other hand, the dramatic μ_{eff} degradation with L_g reduction revealed in control pMOS suggests an aggravated impurity scattering due to halo implantation located near channel region in sufficiently short devices.

B. Local Strain Effect on V_T and Body Bias Sensitivity

Local strain effect on V_T and its sensitivity to body biases emerges as one major concern for the deployment of dynamic body biases. Fig. 3(a) shows the linear V_T measured over various L_g (10~0.06 μm). The control pMOS indicates a significant $|V_T|$ increase with L_g scaling, namely reverse short channel effect (RSCE) over the full range of L_g. Halo implantation introduced lateral non-uniform profile is the major cause responsible for RSCE. As for strained pMOS, RSCE is demonstrated in L_g scaling to 0.13 μm but followed with a V_T roll-off for L_g reduction to 60 nm. The occurrence of V_T roll-off in 60 nm device suggests that short channel effect (SCE) becomes strong and dominates RSCE. Strain induced bandgap narrowing (or valence band offset for holes) and S/D recess for e-SiGe are two potential factors for the worse SCE and V_T roll-off. Note that the V_T lowering in this uni-axially strained pMOS is relatively much smaller than those with bi-axial strain **[9]**. Fig. 3(b) presents V_T shift (ΔV_T) under FBB (V_{BS}=-0.6V) and RBB (V_{BS}=0.6V) over various L_g. The FBB enables a positive V_T shift toward lower $|V_T|$ whereas RBB leads to a negative V_T shift toward higher $|V_T|$. The comparison indicates that strained pMOSFETs have a smaller V_T shift under both FBB and RBB, particularly for L_g scaling to 60 nm. The results can be self-consistently explained with the causes proposed for V_T lowering identified from strained devices. The potential impact is the degraded sensitivity and V_T tunability under dynamic body biases.

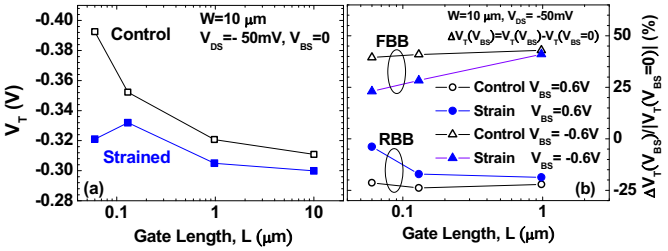

Fig. 3 (a) Linear V_T measured at V_{DS}=-50mV, V_{BS}=0 for strained and control pMOS (b) V_T shift due to $V_{BS,}$ normalized to $V_T(V_{BS}=0)$: $\Delta V_T(V_{BS})/V_T(V_{BS}=0)$,$\Delta V_T(V_{BS})=V_T(V_{BS})-V_T(V_{BS}=0)$ measured under FBB (V_{BS}=-0.6V) and RBB (V_{BS}=0.6V) for strained and control pMOS with L_g =1 ~0.06 μm.

C. Low Frequency Noise –Local Strain and Dynamic Body Biases Effect

Local compressive strain has been proven as an effective performance booster in nanoscale pMOS but its impact on LFN becomes a critical concern for analog and RF circuit design. To explore local strain and gate length scaling effect on LFN, S_{Id} in the strained devices with the shortest L_g and largest μ_{eff} enhancement was investigated. Fig.4 shows the LFN measured

from 60 nm pMOS and represented as S_{Id}/I_{DS}^2 in the frequency domain. Unfortunately, the strained pMOS reveal significantly higher S_{Id}/I_{DS}^2 than control pMOS over the full range of frequencies in 10 ~ 100 kHz.

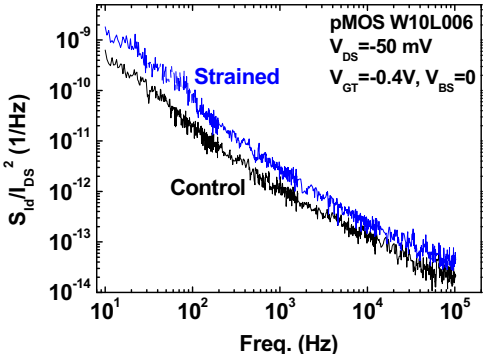

Fig. 4 The S_{Id} measured for 60 nm pMOS under V_{GT} =-0.4V and V_{BS}=0. The LFN is represented as S_{Id}/I_{DS}^2 for a fair comparison between strained and control devices with different I_{DS}.

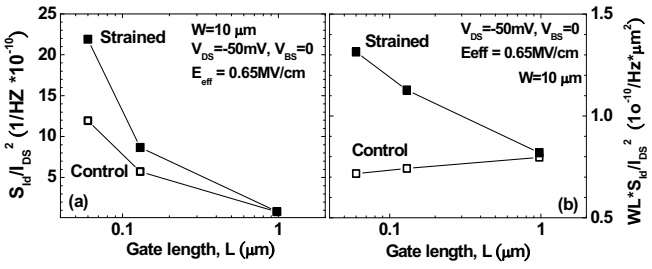

Fig. 5 The S_{Id} measured under a specified E_{eff} of 0.65MV/cm and normalized to $I_{DS}^2$for strained and control pMOSFETs with various L_g (0.98 ~0.06µm) (a) S_{Id}/I_{DS}^2 (b) S_{Id}/I_{DS}^2 xWL_g

Fig. 5(a) shows S_{Id} normalized to I_{DS}^2 under a specified E_{eff} (0.65MV/cm) for strained and control pMOS with various L_g (0.98~0.06 µm). For long devices with L_g=0.98 µm, LFN in terms of S_{Id}/I_{DS}^2 keeps nearly the same for strained and control pMOS. Unfortunately, the strained pMOS suffer obviously higher S_{Id}/I_{DS}^2 for shorter L_g. Fig. 5(b) presents S_{Id}/I_{DS}^2 multiplied with device gate dimensions WxL_g. Interestingly, opposite trends are demonstrated for strained and control devices in $S_{Id}/I_{DS}^2xWL_g$ against L_g scaling. Strained pMOS indicate an increasing trend versus L_g scaling whereas control pMOS reveal a decreasing function. This result cannot be explained by number fluctuation model and actually is in contradiction to what was published for nMOS **[10]**. Referring to Fig. 3(a), the dramatic RSCE revealed in control pMOS indicates a highly non-uniform channel doping profile due to halo implantation and suggests an aggravated impact on LFN based on the number fluctuation model **[10]**. However, the experimental for pMOS exhibits an opposite trend that is the control pMOS with apparently worse RSCE than strained pMOS have much lower LFN. Regarding other potential reasons responsible for the worse LFN in strained devices, like stress induced excess traps or dipoles **[5]**, they cannot be justified due to a contraction with the measured gate leakage currents J_g in which the strain pMOS presents a lower J_g than control pMOS (not shown). The mentioned argument motivates our interest in exploring an appropriate model for an accurate prediction of LFN in pMOS. Fig. 6 presents an analysis of LFN in terms of S_{Id}/I_{DS}^2 under varying $I_{DS}(V_{GT},V_{BS})$ for strained and control pMOS with L_g in 0.98 ~ 0.06 µm. The S_{Id}/I_{DS}^2 follows a function proportional to $1/I_{DS}$ over the whole range of bias conditions from low V_{GT} to high V_{GT}. The result indicates that mobility fluctuation model derived according to Hooge empirical formula and given by (1) or (2) is the dominant mechanism governing pMOS's LFN **[11]**.

$$\frac{S_{I_d}}{I_{DS}^2} = \frac{1}{f}\frac{qV_{DS}}{I_{DS}}\frac{\alpha_H \mu_{eff}}{L^2} \quad (1)$$

$$\frac{S_{I_d}}{I_{DS}^2} = \frac{q}{f}\frac{1}{WLC_{ox}} \times \frac{\alpha_H}{V_{GT}}, \; V_{GT} = (V_{GS} - V_T) \quad (2)$$

where

α_H : *the Hooge parameter*

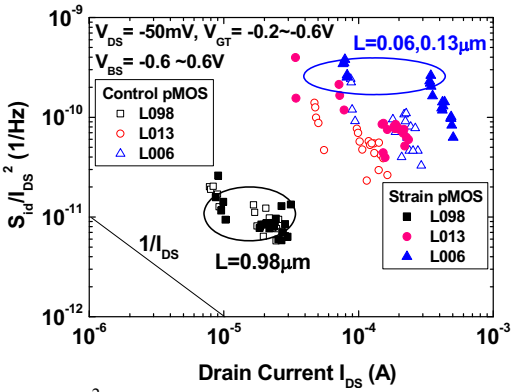

Fig. 6 The S_{Id}/I_{DS}^2 versus I_{DS}, measured under varying V_{GT} (V_{GT}= -0.2~ -0.6V) and body biases (V_{BS}=-0.6, 0, 0.6V) for strained and control PMOS with various L_g (0.98 ~0.06 µm).

Note that S_{Id}/I_{DS}^2 exhibits a dramatic increase with L_g scaling in both strained and control devices, and strained pMOS suffer much higher LFN in terms of S_{Id}/I_{DS}^2 for aggressively scaled dimensions at 0.13 µm and 0.06 µm. The mobility fluctuation model with an expression of (1) for varying I_{DS} or (2) for varying V_{GT} can predict the dramatic increase of S_{Id}/I_{DS}^2 with L scaling and more importantly help explore the origins responsible for the worse LFN in strained pMOS. The increase of effective mobility μ_{eff} or Hooge parameter α_H will lead to higher LFN in terms of S_{Id}/I_{DS}^2 under a specified I_{DS}. It explains why the strained pMOS with short L_g (0.13, 0.06 µm) indeed gain the benefit of higher μ_{eff} but pay the penalty of increased LFN, as shown in Fig. 5 and 6.

According to (2), the effective ways to suppressing LFN can be classified as the increase of device dimensions (W, L), the increase of V_{GT}, and the reduction of α_H. The local strain cooperating with body biases effect on the Hooge parameter α_H emerges as an interesting topic. Fig. 7 makes a comparison in α_H between strained and control pMOSFETs over various L_g, and exhibits a remarkable increase of α_H with L_g in strained devices but a decrease in control devices. It suggests the local strain will increase α_H and makes LFN worse. Note that the

larger α_H in strained pMOS may be due to accelerated phonon scattering in the strained lattice **[12]**. The enlarged difference in α_H with L_g scaling is the major factor responsible for the dramatic difference in LFN, i.e. S_{Id}/I_{DS}^2 between strained and control pMOS with L_g scaled to 60 nm (Figs.5 and 6**).**

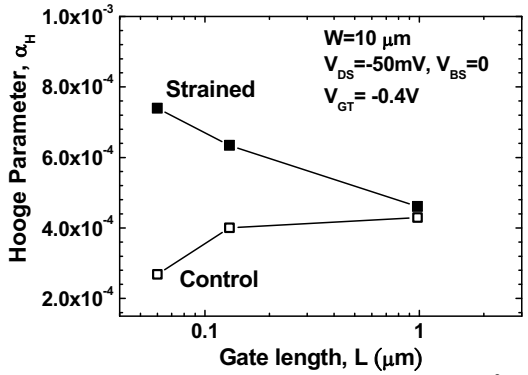

Fig. 7 The Hooge parameter α_H extracted from S_{Id}/I_{DS}^2 measured under V_{GT}=-0.4V and V_{BS}=0 for strained and control pMOS with various L_g (0.98 ~0.06 μm)

Dynamic body biases method proven in DTMOS platform for low power design is considered a potential solution for low noise. Fig. 8 displays dynamic body biases effect on LFN in terms of S_{id} variation under FBB (V_{BS}=-0.6V) as well as RBB (V_{BS}=0.6V) and normalized to the reference S_{id} at ZBB (V_{BS}=0), denoted as $\Delta S_{id}(V_{BS})/S_{id}(V_{BS}=0)$. For both strained and control pMOS, FBB can suppress S_{id} given with $\Delta S_{id}(V_{BS})< 0$, attributed to reduced normal effective field E_{eff}. On the other hand, RBB makes S_{id} worse with $\Delta S_{id}(V_{BS})> 0$. However, the dynamic body bias effect on LFN is degraded in strained pMOS with a smaller amount in $\Delta S_{id}(V_{BS})/S_{id}(V_{BS}=0)$, particularly worse for the shortest devices with L_g=60 nm. The significant V_T lowering and degraded body bias effect shown in Fig. 3 for strained devices explains the diminishing benefit from FBB on LFN.

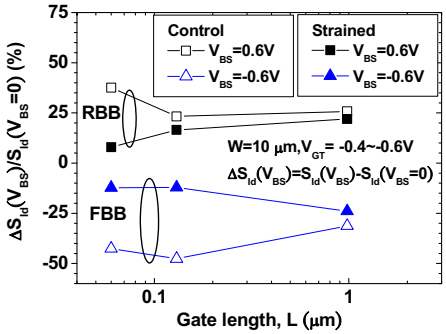

Fig. 8 The change of S_{id} under FBB (V_{BS}=-0.6V) as well as RBB (V_{BS}=0.6V) and normalized to the reference S_{id} at ZBB (V_{BS}=0), denoted as $\Delta S_{id}(V_{BS})/S_{id}(V_{BS}=0)$ measured for strained and control pMOS with various L_g (0.98 ~0.06 μm).

IV. Conclusion

Local compressive strain can realize hole mobility enhancement above 70% in 60 nm pMOSFETs. The remarkable increase in G_m and I_{DS} can boost gate speed and RF/analog circuit performance in terms of f_T and f_{max}. However, the local strain leads to worse LFN with much higher S_{Id}/I_{DS}^2 in nanoscale devices. The number fluctuation model widely used for nMOSFETs is no longer valid and cannot explain the local strain as well as scaling effects on LFN measured from pMOSFETs. Mobility fluctuation model can predict the novel LFN characteristics in the dependence on local strain, geometry scaling, and bias conditions. The increase of Hooge parameter α_H due to local strain is identified as the major factor responsible for worse LFN in strained pMOSFETs. FBB can help suppress LFN but the advantage provided by FBB is degraded in strained pMOSFETs with nanoscale gate lengths.

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