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Charge trapping induced frequency-dependence degradation in n-MOSFETs with high-k/metal gate stacks

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A R T I C L E I N F O

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A B S T R A C T

This letter investigates the reliability issues of $HfO_2/Ti_{1-x}N_x$ metal-oxide-semiconductor field effect transistor in terms of static and dynamic stress. The results indicate threshold voltage (V_{th}) instability under dynamic stress is more serious than that under static stress, owning to transient charge trapping within high-k dielectric. Capacitance–voltage techniques verified that electron trapping under dynamic stress was located in high-k dielectric near the source/drain (S/D) overlap region, rather than the overall dielectric. Furthermore, the V_{th} shift clearly increases with an increase in dynamic stress operation frequency. This phenomenon can be attributed to the fact that electrons injecting to the S/D overlap region have insufficient time to de-trap from high-k dielectric. We further investigated the impact of different $Ti_{1-x}N_x$ composition of metal-gate electrode on charge trapping characteristics, and observed that V_{th} shift decreases significantly with an increase in the ratio of nitride. This is because the nitride atoms diffusing from the metal gate fill up oxygen vacancies and reduce the concentration of traps in high-k dielectric.

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1. Introduction

The continuous scaling of metal-oxide semiconductor field electrical field transistors (MOSFETs) is driving conventional SiO_2-based dielectric to only a few atomic layers thick, leading to the excessive gate leakage current and reliability issues [1–3]. To meet the International Technology Roadmap for Semiconductors, Hf-based dielectrics have been heavily investigated as a replacement for SiO_2 gate insulator to reduce both tunneling gate leakage and power consumption in CMOS circuits [4,5]. However, charge trapping in high-k gate stacks remains a key reliability issue since it causes the threshold voltage (V_{th}) shift and drive current degradation [6–8]. This is believed to happen due to the filling of pre-existing traps in the high-k dielectric layer rather than trap creation over the device operation time [9–11]. However, these studies mainly focused on charge trapping characteristics under the static bias condition. There are a few studies investigating the impact of dynamic operation on V_{th} instability in Hf-based n-MOSFETs, noteworthy because in real circuits the devices are generally operated in the dynamic condition. Therefore, this work further investigates V_{th} instability of Hf-based n-MOSFETs under the dynamic bias operation. The static condition was also performed on the identical device for a comparison. It was found that the V_{th} shift under dynamic operation is more serious compared to that under static operation. Besides, the ΔV_{th} difference between dynamic and static stresses increases with an increase in dynamic operation frequency. Using C–V technology demonstrates that the charge trapping region under dynamic operation is mainly localized near the source/drain (S/D) overlap region, rather than throughout the overall high-k dielectric layer. In addition, we further investigated the impact of different $Ti_{1-x}N_x$ composition of metal-gate electrode on charge trapping characteristics under dynamic condition. It was also observed that V_{th} shift decreases significantly with an increase in the ratio of nitride. This is because nitride incorporation reduces the trap density in the bulk of Hf-based dielectric layer.

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2. Experiment

3The HfO_2 n-MOSFETs with $Ti_{1-x}N_x$ metal gate used in this study were fabricated using a conventional self-aligned transistor flow through the gate first process. For the gate first process devices, high quality thermal oxide with thickness of 10 Å was grown on a (100) Si substrate as an interfacial layer oxide layer. After standard cleaning procedures, 30 Å of HfO_2 films were sequentially deposited by atomic layer deposition. Next, 10 nm of $Ti_{1-x}N_x$ films were deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The S/D and poly-Si gate activation were performed at 1025 °C. The dimensions of the selected devices were 10 μm in both width and length to avoid contribution from the short-channel effect. The V_{th} and inversion equivalent oxide thickness of these devices are ~0.7 V and 18.1 Å, respectively.

The devices were stressed in the dynamic condition with 50% duty cycle. A pulse train with high-voltage of $0.5\ V + V_{th}$, low-voltage of 0 V, and rising/falling time of 10 ns was applied to the gate electrode. The frequencies are in the range of 10 Hz and 10 MHz. The static bias stress was also performed at $0.5\ V + V_{th}$ for comparison. The source, drain and substrate terminals were all grounded during stress. Variations in the V_{th} were monitored from the drain current-gate voltage (Id-Vg) and capacitance–voltage (C–V) transfer characteristics. In the C–V measurement, the gate-to-channel capacitance (Cgc) and the gate-to-body capacitance (Cgb) were measured at a frequency of 1 M Hz at room temperature. For the Cgc operation method, a capacitance measurement high (CMH) was applied to the gate electrode, and both S/D electrodes were connected to a capacitance measurement low (CML). For the Cgb operation method, the gate and body electrodes were connected to CMH and CML,

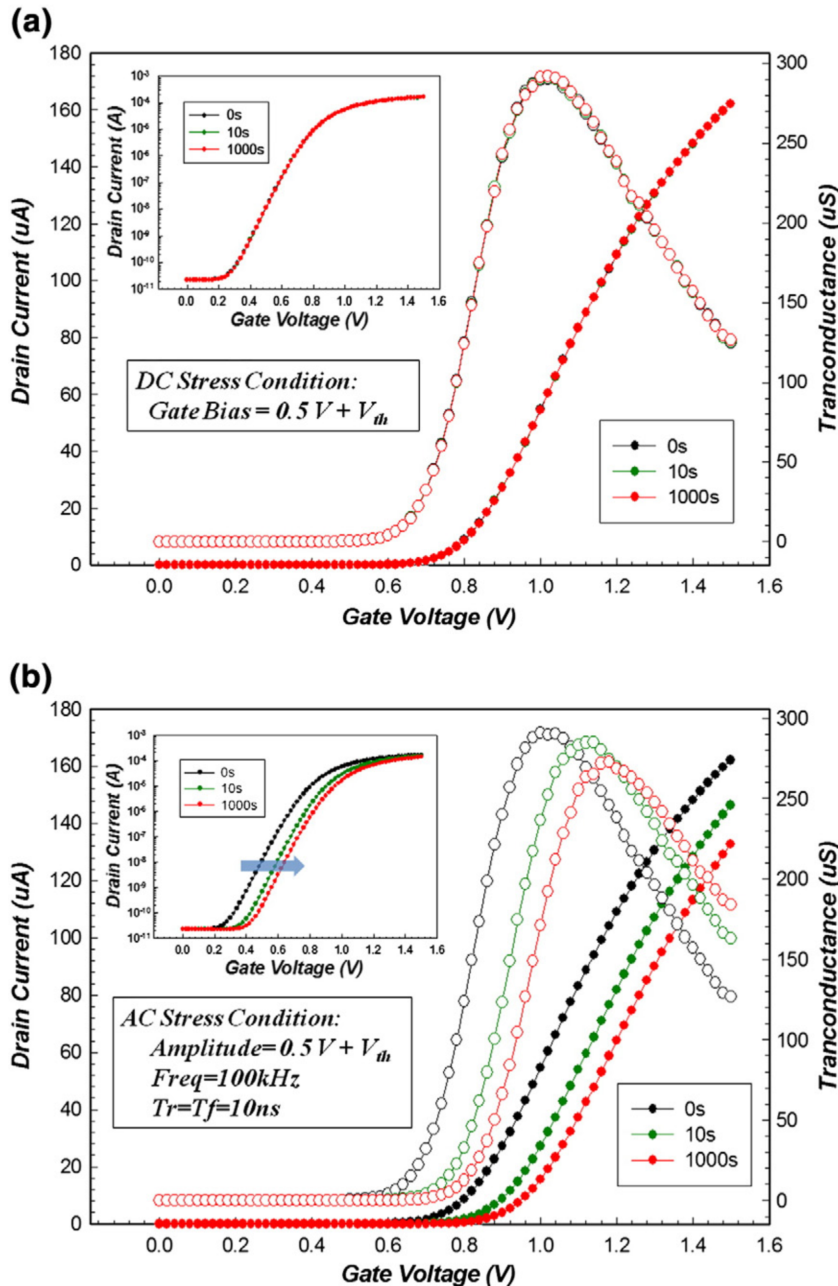


Fig. 1. Id-Vg and corresponding Gm-Vg transfer characteristic curves of high-k/metal gate MOSFETs as a function of stress time under (a) DC stress and (b) AC stress. The inset shows the bias-stress-induced shift of log (Id)-Vg curve. The sweep was done at Vd = 0.05 V for both curves.

respectively. All experimental curves were measured using an Agilient B1500 semiconductor parameter analyzer.

3. Results and discussion

Fig. 1(a) shows the Id-Vg, and corresponding Gm-Vg transfer characteristic curves with 50 mV drain voltage under initial and after static stress. Obviously, the device exhibits no degradation under the static positive gate bias of $0.5\,V + V_{th}$ over a period of 1000 s. This indicates no obvious charge trapping phenomenon can be observed in this stress condition. However, when dynamic stress was applied to the identical device, the transfer characteristic has significant degradation, as shown in Fig. 1(b). The V_{th} shifts to the positive direction and on-current is degraded after the stress. In addition, the transfer curves shift has not been accompanied by subthreshold swing degradation, meaning that there is no creation of extra interface states between the active region and dielectric layer. Therefore, most of the V_{th} shift can be attributed to the charge trapping within the high-k dielectric layer.

The results above support the conclusion that charge trapping in the dynamic condition is more serious than in the static condition. This phenomenon is inconsistent with the general realization that the dynamic bias causes less degradation due to its shorter effective stress time [12]. To further understand this phenomenon, the Cgb-Vg and Cgc-Vg transfer characteristics under initial and after dynamic stress are measured and shown in Fig. 2(a) and (b), respectively. It can be observed that the Cgc-Vg curves shift in the positive direction after dynamic stress, which is consistent with the Id-Vg result in Fig. 1(b). However, Fig. 2(b) shows that Cgb measured between the gate and the substrate terminals has no significant change before and after stresses. No variation in flat band voltage suggests that in the dynamic condition, electrons cannot be really captured in throughout the overall high-k dielectric layer. Therefore, the ΔV_{th} in Figs. 1(b) and 2(a) can be mainly attributed to the electrons trapped near the S/D overlap region. Fig. 3 illustrates that the captured electrons raise the band energy upward and induce additional energy barriers near the S/D overlap. Both barrier heights resist the electrons supplied from the S/D, leading to the positive shift in the Cgc-Vg measurement. However, the local electrons trapped near the S/D overlap region have no influence on the charge variation across the overall high-k dielectric layer during the Cgb-Vg measurement. Therefore, the flat band voltage in the Cgb-Vg curves has no significant change before and after stresses.

The frequency dependence of the electron trapped near the S/D overlap region was also evaluated. Fig. 4 shows the ΔV_{th} as function of the stress time for DC stress and AC stresses in the frequency range of 10 Hz to 10 MHz. It can be seen that the magnitudes of V_{th} shift under several AC stresses are significantly higher than that of continuous DC stress. Besides, the ΔV_{th} has an increase with dynamic stress operation frequency. Furthermore, the linear relationship between ΔV_{th} and stress frequency is also obtained and shown in the inset of Fig. 4. Due to the fact that these AC stresses were all done with 50% duty cycle, this suggests that under the dynamic stress, the amount of electron trapped near the S/D overlap region has a high dependence with the stress frequency, rather than the effective equivalent stress time. Based on these results, we proposed the reasonable explanation why the electrons can be captured only near the S/D overlap during dynamic stress.

The previous proposed charge trapping model [13,14] suggests that in the period of on-state stress, a small portion of electrons can be captured instantly in the shallow traps of the high-k dielectric, as shown in the Fig. 5(a). Then, at off state, the built-in electronic field established by work function difference between metal gate and p-substrate drives these trapped electrons to migrate toward the gate electrode by Poole–Frenkel emission [7]. This same electrical field direction during on-state and off-state continuously drives these elections, captured in shallow traps, toward the gate electrode. Therefore, few electrons can be captured in the deep traps of high-k dielectric above the channel region. This is also the reason why the charge trapping phenomenon cannot be observed in the constant electrical field under static bias stress. When we consider the S/D overlap region, the on-state bias results in the electrons still being captured in the shallow traps of the high-k dielectric, as shown in Fig. 5(b). In the off-state stress, however, due to the positive value of work function difference between TiN and N + S/D, a contrary direction of electrical field exists and prompts the trapped electrons to migrate toward the N + S/D. The different electrical field directions

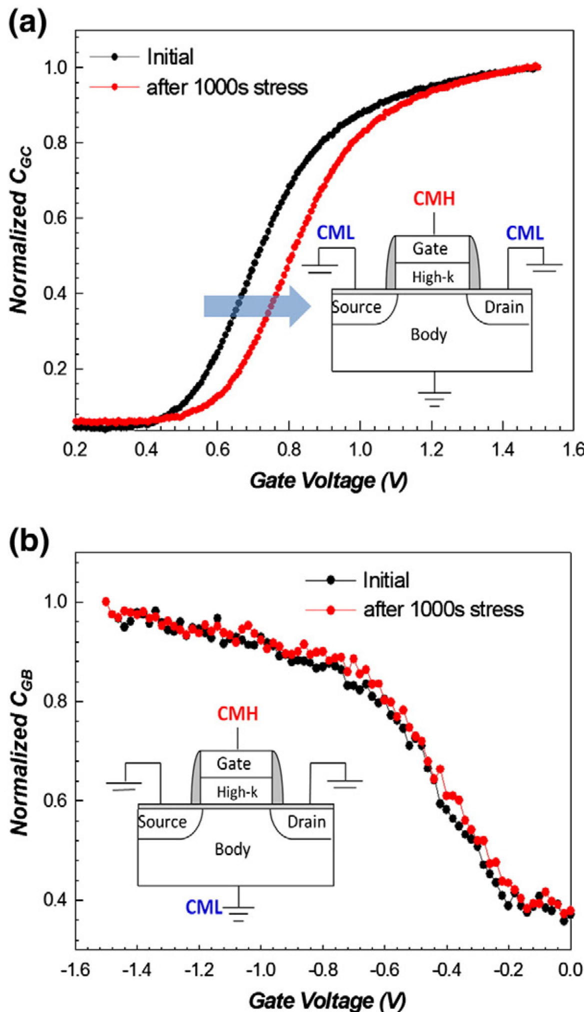


Fig. 2. (a) Normalized Cgc-Vg and (b) Normalized Cgb-Vg transfer characteristics under initial and after dynamic stress. The inset shows their respective measurement method.

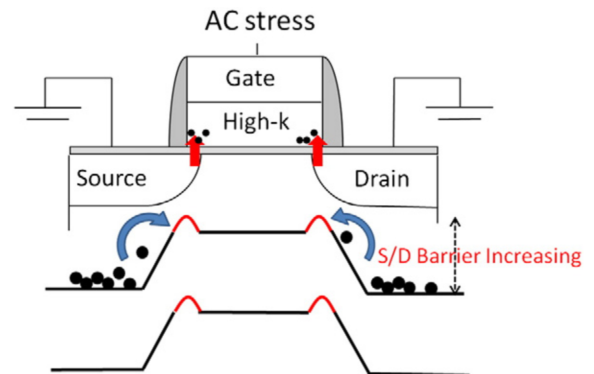


Fig. 3. Schematic diagram of the high-k/metal gate MOSFET and its energy-band diagram after dynamic stress.

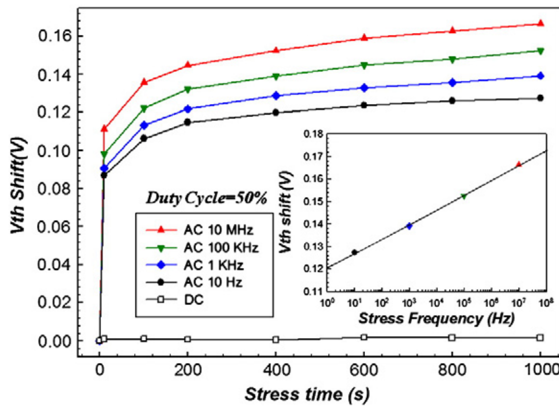
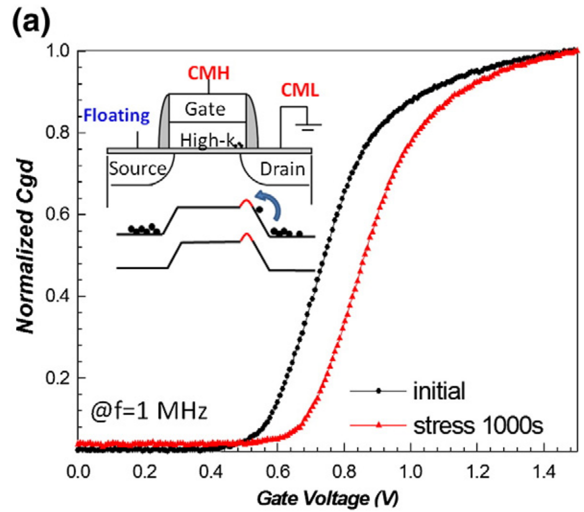


Fig. 4. ΔV_{th} versus stress time under static and dynamic stress with different frequencies, $V_{stress} = 0.5\,V + V_{th}$. The inset displays the linear relationship between stress frequency and ΔV_{th} after 1000 s stress.

between on and off states does not allow these electrons in the shallow traps have sufficient time to escape from the high-k dielectric. This increases the possibility of electron capture in the deep traps of high-k dielectric. Besides, the higher frequency of dynamic stress leads to more increase in V_{th} shift, as shown in the Fig. 3. This can be attributed to the fact that higher frequency supplies less time for electrons trapped in the shallow defects to de-trap from the high-k dielectric. Consequently, in the dynamic condition, the charge trapping phenomenon occurs obviously near the S/D overlap region and becomes more serious with the increase in dynamic stress frequency.

To further confirm this phenomenon, the dynamic stress condition was imposed upon an identical device, with the exception of a floating source terminal. The Cgd-Vg and Cgs-Vg curves before and after stress are shown in Fig. 6(a) and (b), respectively. After the stress, the Cgd-Vg curves have a similar shift to those in Fig. 2(a) due to the energy barrier induced by trapped electrons in the drain overlap region, as shown in the inset of Fig. 6(a). However, Fig. 6(b) shows no significant change in the Cgs-Vg curves under this stress condition. This evidence indicates that there is no additional energy barrier near the source overlap region, due to the fact that the dynamic bias cannot be applied across the overlap region between the gate and floating source terminals. This result further verifies that charge trapping in the overlap region is an effect of variation of electrical field.



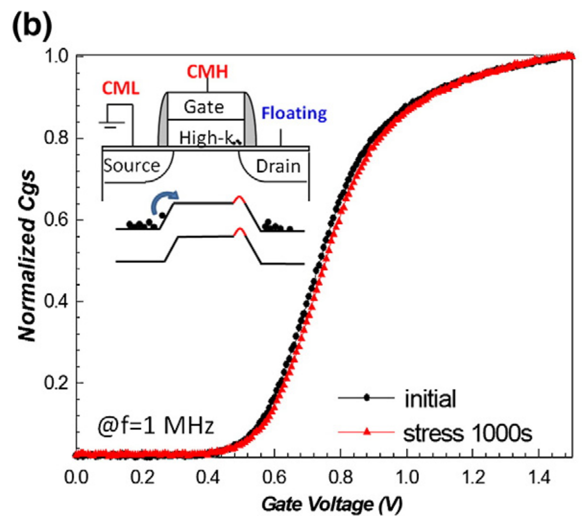


Fig. 6. (a) Cgd-Vg and (b) Cgs-Vg transfer characteristics under initial and after dynamic stress. The inset shows their respective measurement method and illustrates the energy-band diagram after dynamic stress for a device with a floating source.

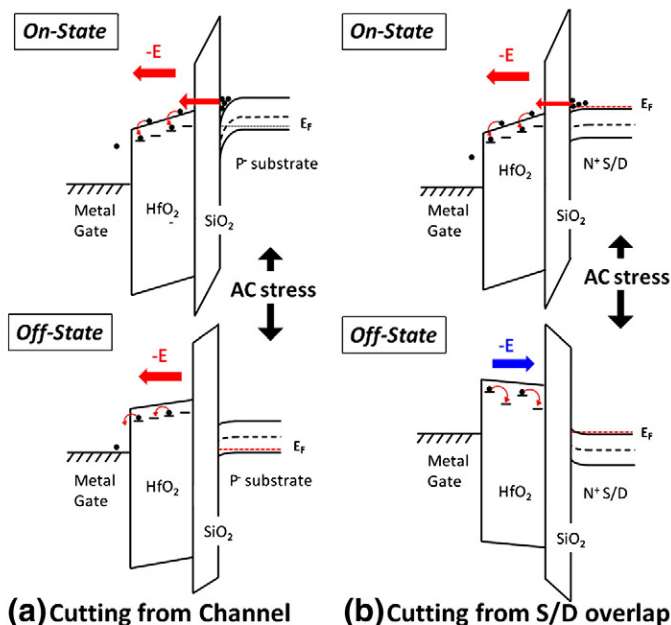


Fig. 5. Variation of energy-band diagram cutting from (a) channel region and (b) S/D overlap region during dynamic stress.

This charge trapping characteristics induced by dynamic condition was also investigated as function of the nitride concentration in the TiN metal gate. Fig. 7 shows ΔV_{th} as function of the stress time with different $Ti_{1-x}N_x$ composition of metal-gate electrode under dynamic condition. It can be seen that the magnitude of ΔV_{th} has a decrease with an increase in the ratio of nitride. This phenomenon indicates that higher nitride concentration of TiN metal gate results in the less electrons trapping in the high-k dielectric layer near the S/D overlap region. This is because the nitride atoms diffusing from the metal gate can fill up oxygen vacancies and reduce the concentration of traps in high-k dielectric. This result is in agreement with reports that nitrogen anneals oxygen vacancies that act as electron trap centers [15].

4. Conclusion

In this paper, we observed that the V_{th} instability induced by charge trapping under dynamic stress was more serious than under static stress. C–V techniques verified that electron trapping under AC stress is located in the high-k dielectric near the S/D overlap region rather than throughout the overall dielectric. Besides, the amount of electrons trapped in the S/D overlap region has a high dependence of dynamic frequency. These results can be attributed to the different

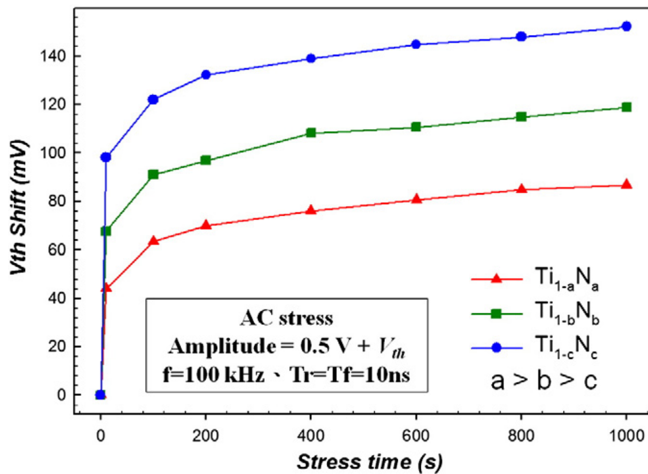


Fig. 7. ΔV_{th} versus stress time under dynamic stress for the devices with different nitride ratio of TiN metal gate.

electrical field direction in the S/D overlap region during dynamic stress. This trapping phenomenon was further verified by applying identical stress conditions to a device with floating source. In addition, the different $Ti_{1-x}N_x$ composition of metal-gate electrode also affects this charge trapping characteristic. It was observed that V_{th} shift decreases significantly with an increase in the ratio of nitride. This is because nitride incorporation in the metal gate can diffuse and fill up oxygen vacancies, reducing the trap density in the bulk of HfO_2 dielectric layer. Therefore, the dynamic stress induces less electron trapping in the high-k dielectric near the S/D overlap region. These results imply that in real circuit operation, the main charge trapping issue is induced by the electrons trapped in high-k near the S/D overlap region. Choosing an appropriate material as a metal gate is an important role to solve the V_{th} instability in the MOSFETs with high-k/metal gate stacks.

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