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Enhanced data retention characteristic on SOHOS-type nonvolatile flash memory with CF_4-plasma-induced deep electron trap level

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The improved data retention characteristics of Polysilicon-oxide-hafnium oxide-oxide-silicon (SOHOS) type nonvolatile memory were obtained by post-HfO_2 trapping layer deposition tetrafluoromethane (CF_4) plasma treatment. The memory characteristics such as program/erase speed, retention and endurance were studied comprehensively. That fluorine atoms incorporated into Hf-based high-k material eliminate shallow trap defect level effectively and remain deeper trap level. Although the shallow traps of the HfOF trapping layer SOHOS memory have passivated, it doesn't deteriorate the program/erase speed obviously and retention characteristic was then improved because of deeper electron storage level. The results clearly indicate CF_4 plasma treatment-induced deep electron storage level is a feasible technology for future SOHOS-type nonvolatile flash memory application.

Introduction

Since the first floating gate nonvolatile flash memory was invented in 1967 [1], it has taken possession of almost nonvolatile memory market. Nevertheless, owing to the application of system-on-chip (SOC), a continuously scaling of the gate dielectrics for complementary metal-oxide-semiconductor (CMOS), tunnel oxide and inter-poly dielectrics (IPDs) for electrically erasable programmable read-only memory (EEPROM) and stacked-gate flash memory is needed to obtain high density and low operation voltage. Scaling down of the tunnel oxide thickness in a flash is essential to reduce the cell size and the program/erase voltage. However, a thinner tunnel oxide (below 7-8 nm) results in reliability degradation and starts to leak due to the stress-induced leakage current (SILC) resulting from repeated program/erase operations [2] and the possible disturb effect. After stress-induced leakage path generation in the tunnel oxide, the storage charge in the floating gate loses easily to exhibit false data information. Recently, polysilicon-oxide-nitride-oxide-silicon (SONOS)-type nonvolatile memories (NVMs) have attracted much attention as one of the most promising candidate to replace the conventional floating gate flash memory for the industry moves to 32 nm and beyond [3]-[5]. High permittivity constant dielectric have been proposed to further instead of trapping layer (HfO_2) or blocking oxide (Al_2O_3) to improve program speed or charge retention characteristics. However, hafnium oxide (HfO_2) is expected to a promising candidate for charge trapping and longer retention time owing to sufficient trap density and deep trap energy level [6], [7].

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For continuing scaling, the high permittivity dielectric constant material were proposed to replace conventional thermal dry oxide (SiO_2) or oxynitride (SiON) to avoid direct tunneling gate leakage current owing to larger physical thickness at the same equivalent oxide thickness [8]-[10]. However, reliability issue such as negative/positive bias temperature instability (N/PBTI) or charge to breakdown (Q_{BD}) is a main obstacle of high-κ material integrated into MOSFET. Consequently, fluorine passivation technology has been proposed and successfully demonstrated on ULSI MOEFET device fabrication for improving dielectric reliability [11]-[14]. Fluorine incorporation is effective to terminate bulk defect such as oxygen vacancy within high-k gate dielectric, which is helpful to reduce gate leakage current, larger carrier mobility, less charge trapping and result in deeper trap energy level as well [15], [16]. Even so, the characteristics of fluorine passivation effect on SOHOS-type nonvolatile memory are seldom investigated yet. In this paper, the impact of fluorine passivation by post-HfO_2 trapping layer deposition CF_4 plasma treatment of SOHOS-type nonvolatile flash memory has been studied for first time.

Experimental details

The n-channel SOHOS-type NVMs with gate stacks hafnium oxide (HfO_2) trapping layer were fabricated on 6-inch p-type (100) Czochralski (CZ) silicon wafer with 1-10 Ω-cm resistivity. After the standard RCA cleaning with a hydrofluoric (HF) acid-last process, the 3-nm tunneling oxide were grown at 900°C in oxygen (O_2) ambient by APCVD. The 5-nm HfO_2 trapping layer was deposited by the AIXTRON metal organic chemical vapor deposition (MOCVD) system at 500°C. After HfO_2 trapping layer deposition, CF_4 plasma was used to treat HfO_2 trapping layer in plasma-enhanced chemical vapor deposition (PECVD) system(denoted as HfOF in the following). The RF power, chamber pressure, flow rate and process time of CF_4 plasma were 50 watt, 90m torr, 30 sccm and 30 sec, respectively. Furthermore, without CF_4 plasma treatment serves as reference sample (denoted as HfO_2 in the following). A 10-nm blocking oxide was deposited by LPCVD TEOS (Si ($OC_2H_5)_4$) at 700°C, followed by poly-Si gate 200 nm deposition by LPCVD system using silane (SiH_4) gas at 620°C.

After gate electrode patterning by the I-line lithography stepper and subsequently phosphorous implantation at 25 keV, 5×10^{15} cm^{-2}, dopants were then activated at 950°C for 30 s in N_2 ambient. Finally, contact holes etching and Al metallization were performed using standard CMOS fabrication process, followed by forming gas annealing in N_2/H_2 ambient at 400°C for 30 min to reduce interfacial trap density.

The electrical properties and reliability characteristics of were measured using Hewlett-Packard 4156C semiconductor parameter analyzer and Hewlett-Packard 81110A pulse generator. Furthermore, the content and distribution of the fluorine atom was measured by secondary-ion mass spectroscopy (SIMS). The binding energy of the hafnium and fluorine atom was extracted from the X-ray photoelectron spectrometer (XPS).

Results and discussion

Fig. 1 shows the SIMS depth profile of the SOHOS gate stacked nonvolatile memory with post-HfO_2 trapping layer deposition CF_4 plasma treatment. The result obviously indicates that fluorine is effectively incorporated into the trapping layer (HfO_2) of SOHOS gate stack by CF_4 plasma treatment and during subsequently high temperature processes, which is helpful to passivate the bulk HfO_2 defect such as oxygen vacancies to form Hf-F bonds, and result in deep electron trap level[15], [16]. Moreover, the fluorine

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can further pile up at the interface between the blocking oxide/trapping layer (SiO_2/HfO_2), which also reveals that the CF_4 plasma treatment process exhibits high probability to terminate the interface dangling bonds between blocking oxide/trapping layer to generate robust bonds to against the program erase cycles stress.

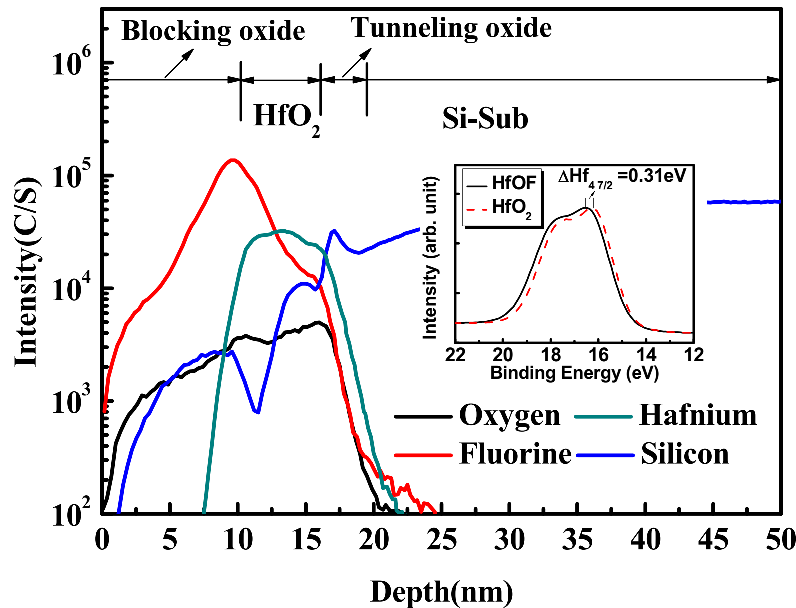

Fig. 1. SIMS depth profile of the SOHOS-type nonvolatile flash memory with post- HfO_2 trapping layer deposition CF_4 plasma treatment. XPS analysis of the Hf_{4f} electronic spectra is also shown in inset.

XPS spectra of the Hf_{4f} signal for the HfO_2 trapping layer with and without CF_4 plasma treatment is shown in inset. The detected binding energy was calibrated by C_{1s} signal at 284.5 eV. Compared with HfO_2 SOHOS NVM, the HfOF SOHOS NVM process obviously increases the binding energy larger roughly 0.31 eV for the $Hf_{4f7/2}$ signal. The binding energy of the $Hf_{4f7/2}$ signal increases from 16.26 eV to 16.57 eV, because the shallow trap defects were passivated by fluorine atoms.

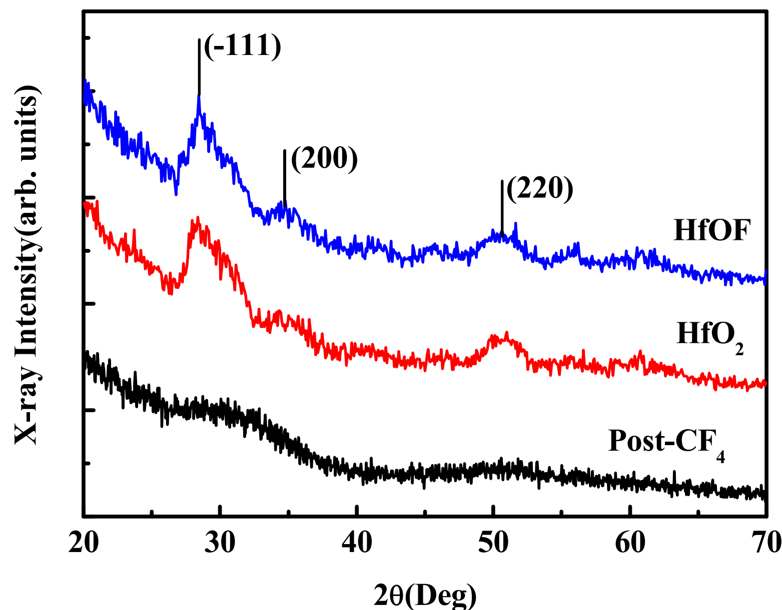

Fig. 2. X-ray diffraction of the HfO_2 trapping layer with and without CF_4 plasma treatment.

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As we know, CF_4 gas was applied to dry etching system extensively. To investigation the CF_4 plasma-induced etching effect in HfO_2 material, Atomic Force Microscope (AFM) was used to analyze the surface roughness of post-HfO_2 deposition CF_4 plasma treatment. The Root-Mean-Square (RMS) variation of surface of HfO_2 and HfOF materials were 0.195 and 0.197 nm, respectively. Elliposmetry was applied to analysis the thickness of CF_4 treated HfO_2 material. The measured thickness of HfO_2 and HfOF films were 5.4nm and 5.9nm, respectively. The results of RMS and thickness difference indicate the CF_4 plasma etching effect is negligible, and the fluorination process would not damage HfO_2 material during CF_4 plasma treatment. High temperature process would influence the crystallization behavior of HfO_2 material, and the crystallization level could affect the program/erase as well as retention characteristics [17], [18]. Therefore, to ensure that the CF_4 plasma itself did not affect the crystallization level, we used X-Ray Diffraction (XRD) to analyze the crystallization level of HfO_2 material after CF_4 plasma treatment and shown in Fig. 2. It not shows obviously crystallization of post-CF_4 plasma treatment. After the blocking oxide deposition thermal cycle, the HfO_2 and HfOF material shows similar crystallization level, so we have confirmed the fluorination process would not affect the crystallization level of HfO_2 material

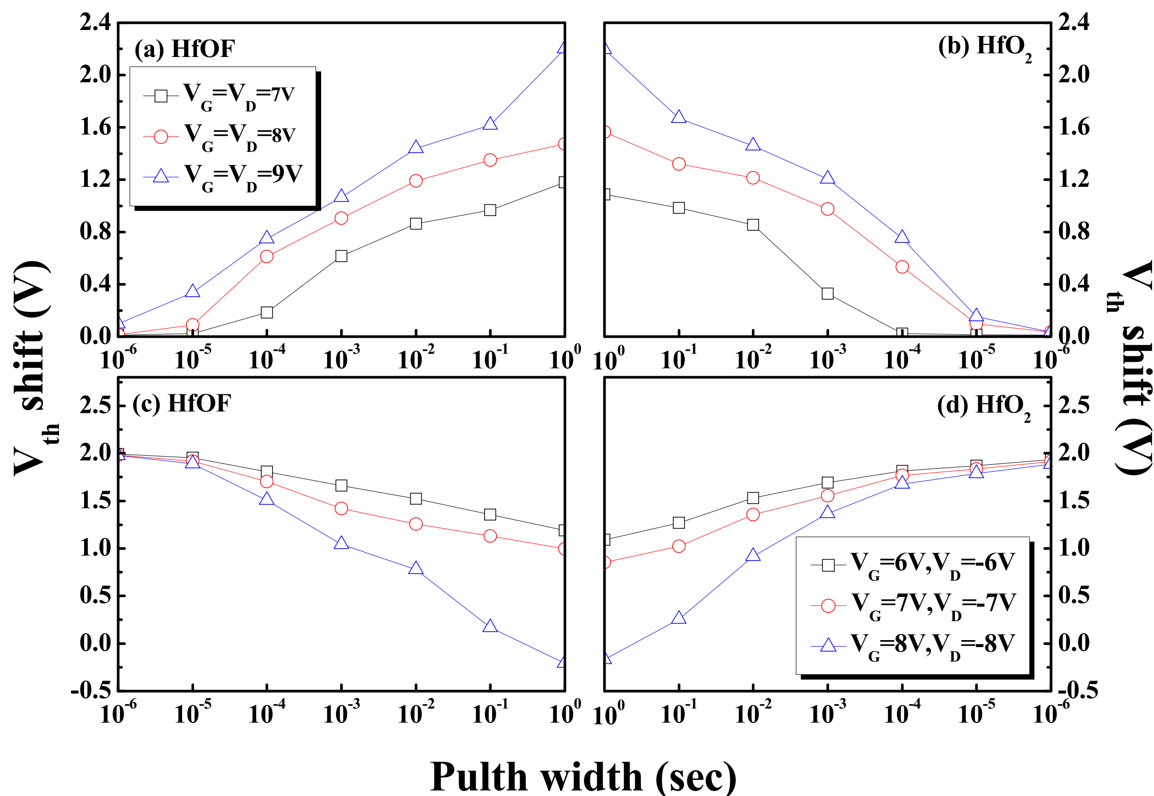

Fig. 3. Program and erase speed characteristics of the SOHOS-type nonvolatile flash memory with and without post- HfO_2 trapping layer deposition CF_4 plasma treatment.

Fig. 3 (a), (b) show the program speed characteristics of the SOHOS-type NVMs with HfO_2 and HfOF trapping layer, respectively. We used channel hot-electron injection (CHEI) for the programming under the bias conditions at (i) $V_G = V_D = 7$ V, (ii) $V_G = V_D = 8$ V, (iii) $V_G = V_D = 9$ V, respectively. The V_{th} shifts of both devices increase with increasing applied gate and drain voltage. This is because the larger the voltage is applied,

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and more hot electrons are generated. More electrons are able to cross the barrier height and trapped in the HfO_2 or HfOF trapping layer, thus the V_{th} shift increase. In addition, compared HfO_2 trapping layer to HfOF trapping layer of SOHOS NVMs, the program speed shows similar trend. It can infer to similar crystallization level. Although fluorine incorporated to HfO_2 trapping layer would diminish oxygen vacancy, the program speed characteristic not changed by post-HfO_2 trapping layer deposition CF_4 plasma treatment. Fig. 3(c), (d) present the erase speed characteristics of the SOHOS-type NVMs with HfO_2 and HfOF trapping layer, respectively. We use band to band hot hole (BTBHH) to erase, and the erase conditions are (i) V_G = -6 V, V_D = 6 V, (ii) V_G = -7 V, V_D = 7 V, (iii) V_G = -8 V, V_D = 8 V, respectively. The erase speed of both devices increase as gate voltage becomes more negative. Similar trend with program characteristic, the fluorination process would not affect the erase characteristic of SOHOS-type NVMs.

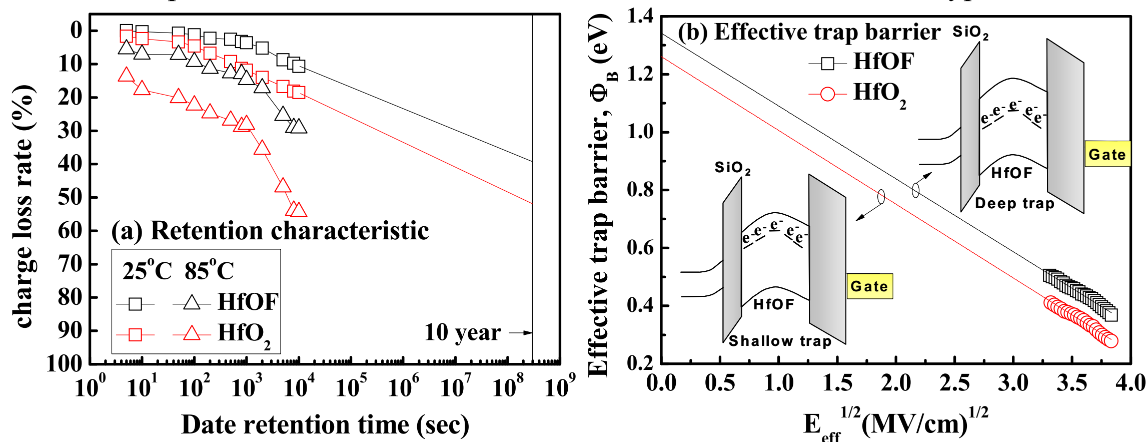

Fig. 4.(a)Data retention characteristic of the SOHOS-type nonvolatile flash memory with post- HfO_2 trapping layer deposition CF_4 plasma treatment at room temperature 25°C and high temperature 85°C. (b) F-P effective barrier fitting of HfO_2 and HfOF gate dielectric. The insets show the band scheme of the SOHOS-type nonvolatile flash memory with shallow and deep electron storage level.

Long-term (10 years) retention is of concern for NVMs. The upper bound of the temperature specification for NVMs is typically 85°C for commercial applications. The understanding of data retention characteristics and charge loss mechanisms has been studied for scaled SONOS structures due to the use of ultra-thin tunnel oxides [19]. It has been reported that thermal excitation is the dominant charge decay mechanism for higher temperature. Retention characteristics of HfOF charge trapping layer compared to that of HfO_2 charge trapping layer of SOHO-type NVMs were shown in Fig. 4.We can observe the charge storage capability of HfOF trapping layer(~90%) is better than HfO_2 trapping layer(~82%) at 10^4 sec. Several fluorine passivation studies demonstrated the fluorine incorporate within bulk Hf-based high permittivity material is effective to passivate shallow trap defect and result in deep trap level [15], [16]. As we know, the trapped charge at deeper level is more difficult detrap. Therefore, we incorporated fluorine atoms into HfO_2 charge trapping layer and result in deep electron trap level. The deep trap level for charge storage effectively improved the charge retention characteristics. As increase the measurement temperature to 85°C, it more conspicuous the charge loss rate of deep electron trap level HfOF trapping layer is lower than shallow electron trap level HfO_2 trapping layer. Frenkel-Poole (F-P) conduction equation was further applied to extract the effective trapping barrier, as shown in Fig. 4(b). We fitted the effective electron charge trap level from measured MOS capacitor I-V data with and without CF_4 plasma treatment.

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The effective trapping barrier for HfOF and HfO_2 gate dielectric is 1.34 and 1.26 eV, respectively. The charge storage band schemes for deep and shallow trap of SOHOS-type NVMs are also shown in inset. The results clearly indicate fluorine incorporation will trap charges in deeper level, which is helpful for retention characteristic of SOHOS-type NVMs charge storage.

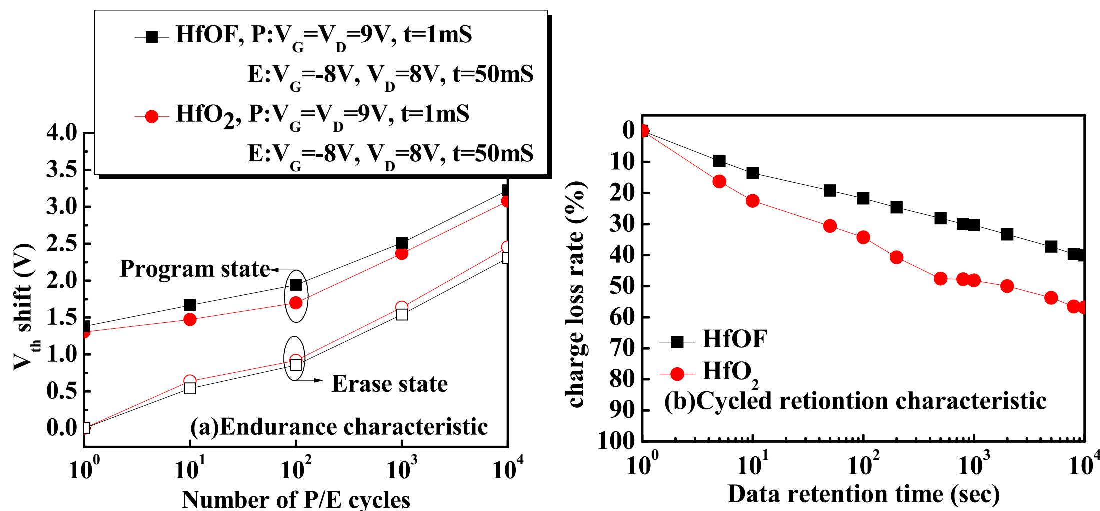

Fig. 5.(a) Endurance and (b) cycled retention characteristic the SOHOS-type nonvolatile flash memory with and without post- HfO_2 trapping layer deposition CF_4 plasma treatment.

Fig. 5(a) displays the endurance characteristics of the SOHOS-type NVMs with HfO_2 and HfOF trapping layer after 10^4 program/erase (P/E) cycles. The devices are programmed under $V_G = V_D = 9$ V for 1 ms, and erased under $V_G = -8$ V and $V_D = 8$ V for 50 ms. As we can observe that the memory window is slightly upon shift and narrowing, it is attributed to the residual charge trapped inside HfO_2 not discharge yet and therefore results in increasing memory window slightly. The trapped charge were difficult to discharge unless the trapped charge position at the hot hole injection point. The retention characteristics of the devices after 10^4 P/E cycles were shown in Fig.5(b). Again, the effect of CF_4 plasma treatment HfO_2 trapping layer-induced deep electron trap was observed. It was quite obvious that the cycled retention characteristic of HfOF trapping layer SOHOS NVMs shows the better charge storage ability than that of HfO_2 trapping layer SOHOS NVMs.

Conclusions

For the first time, fluorine passivation technology integrated with polysilicon-oxide-hafnium oxide-oxide-silicon (SOHOS)-type nonvolatile memory for improving data retention characteristic. That fluorine incorporated into HfO_2 trapping layer by post-HfO_2 trapping layer deposition CF_4 plasma treatment to form fluorinated HfO_2 (HfOF) charge trapping layer eliminate shallow trap effectively and remain deeper trap level for charge storage when charge were programmed into HfO_2 trapping layer. Though shallow trap have been eliminated by fluorine atom, the program/erase characteristics have not been influenced and the data retention characteristic was improved. The results clearly indicate fluorinated HfO_2 charge trapping layer using CF_4 plasma treatment is a feasible technology for future SOHOS-type nonvolatile flash memory application.

Acknowledgments

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