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Performance improvement of pentacene-based organic thin-film transistor with HfO_2 gate dielectrics treated by CF_4 plasma

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Fluorine incorporation into the HfO_2 gate dielectrics by post CF_4 plasma treatment in an inductively coupled plasma chamber was proposed to improve gate leakage current and modify surface property for low-temperature fabrication. During the whole process, the temperature is controlled below 150 ^{o}C. The low-leakage HfO_2 dielectric treated by CF_4 plasma was characterized and then utilized in pentacene-based OTFTs. After CF_4 plasma treatment, the gate leakage and field effect mobility were effectively improved. By integrating high-k HfO_2 by CF_4 plasma treatment and HMDS evaporation treatment, a low operating voltage (-4V), low threshold voltage (-1.12V), a low subthreshold swing (266 mV/decade), a field-effect mobility (0.029cm^2/Vs) and an on/off current ratio (>10^4) were obtained.

Introduction

Organic thin film transistors (OTFTs) have attracted considerable attention because they can potentially be developed into lightweight, flexible, and low-cost electronic device. In order to reduce operation voltage and improve performance, several high-k gate dielectrics were reported, such as Al_2O_3 (1), Ta_2O_5 (2), TiO_2 (3) and HfO_2 (4). Among these dielectrics, HfO_2 thin films were widely investigated as a potential high-k oxide in replacement of SiO_2 for ultra large scale integration (ULSI) technology due to high dielectric constant and wide energy bandgap. In previous reports, HfO_2 gate dielectric treated by CF_4 plasma can effectively reduce leakage current and hysteresis phenomenon (5, 6). In addition, the electrical properties of OTFTs are highly determined between the gate dielectric and channel. The CFx also used to modify the interface to improve the electrical properties of OTFT (7).

Organic thin film transistors with low operation voltage and low process temperature are required for Flexible Electronics (8). Using high-k dielectrics can increase capacitance density which can reduce the threshold voltage and subthreshold swing (9). However, the high-k dielectrics which deposited at low temperature have more defects, so they usually need a high temperature annealing more than 300^{o}C to effectively reduce leakage current. High-density inductively coupled plasma (ICP) sources are widely used in semiconductor fabrication processing. The inductively coupled plasma (ICP) chamber can independently control the plasma density as well as ion bombardment energy. In this work, fluorine incorporation into the HfO_2 gate dielectrics by post CF_4 plasma treatment at 150^{o}C in an ICP chamber was proposed to improve not only gate leakage current but also surface property for low-temperature applications.

Experiment

First of all, a 500-nm SiO_2 film was grown on silicon wafers by wet oxidation. The Metal-insulator-Metal capacitors-(Ni/HfO_2/Ni) were fabricated on SiO_2/Si to analyze the dielectric properties. The 50 nm-thick bottom nikel electrodes and 40 nm-thick HfO_2 gate dielectrics were deposited by electron beam evaporation. After the gate dielectric deposition, samples were treated by CF_4 plasma in an inductively coupled plasma chamber with pressure of 100 mTorr at 150 °C. The flow rate of CF_4, ICP power and process time are 100sccm, 500W, 90sec respectively. Next, top nikel electrodes were evaporated through a shadow mask (A= $4X10^{-5}$ cm^2). The optimized parameter was used to fabricate OTFT. First, a 50-nm-thick nikel film was deposited and patterned through shadow mask to use as the gate electrode. Second, HfO_2 gate dielectric was evaporated, followed by CF_4 plasma treatment. A control sample annealing for 1 hour at 150 °C in N_2 without plasma treatment was also implemented. After CF_4 treatment, HMDS is also evaporated on gate dielectric surface to modify the surface property. Next, 80nm-thick pentacene (Aldrich Chemical Company) active layer was evaporated through a shadow mask on gate dielectric. This evaporation was performed at a deposition rate of 1Å/s at 70 ^{o}C, under a pressure of 3×10^{-6} torr. Finally, a 100 nm-thick gold was deposited onto the pentacene to form a source/drain(S/D) contact. The devices had a channel length of 50μm and a width of 500μm. Figure 1 shows device structure of top contact OTFT.

X-ray photoelectron spectroscopy (XPS) was used to study the chemical bonding. The depth profile of fluorine incorporation was analyzed by the secondary ion mass spectroscopy (SIMS). The surface morphologies of dielectric and pentacene films were analyzed by atomic force microscopy (AFM). The high frequency (100 kHz) capacitance voltage (C-V) characteristics and current-voltage (I-V) curves were measured by Agilent 4156C and HP 4284, respectively.

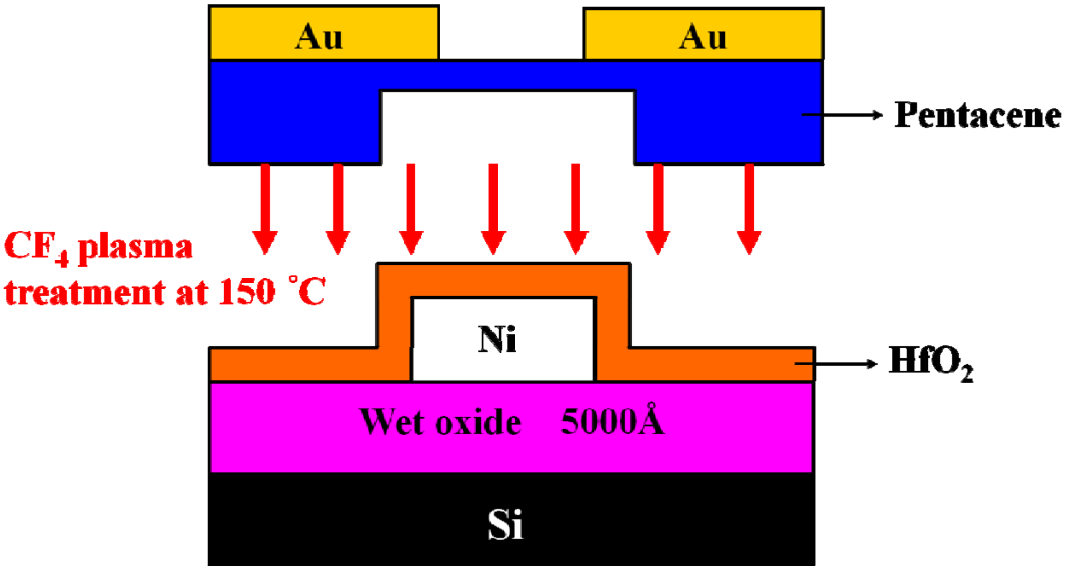
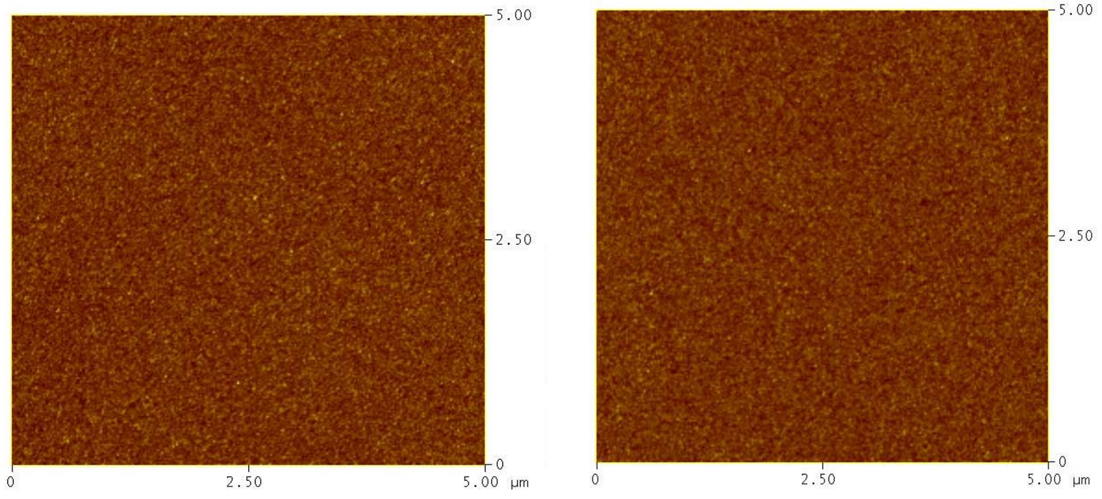


Figure 1 Device structure of top contact OTFT

Results and discussion

Since the plasma treatment maybe result in a rough surface which can degrade the performance, AFM is used to investigate on surface morphology without and with plasma treatment. Figure 2 shows the AFM surface images of HfO_2 without treatment and with CF_4 plasma treatment. The rms roughness value is 0.596nm and 0.515nm respectively. The result shows that the surface roughness is similar to the no treatment sample after plasma treatment.



(a) (b)

Figure 2 AFM surface image of HfO_2 (a) without plasma treatment (b) with CF_4 plasma treatment

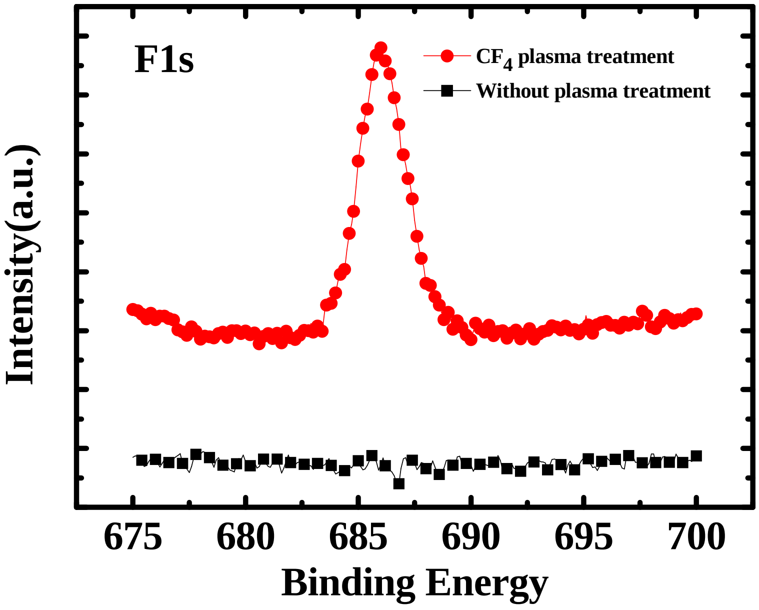
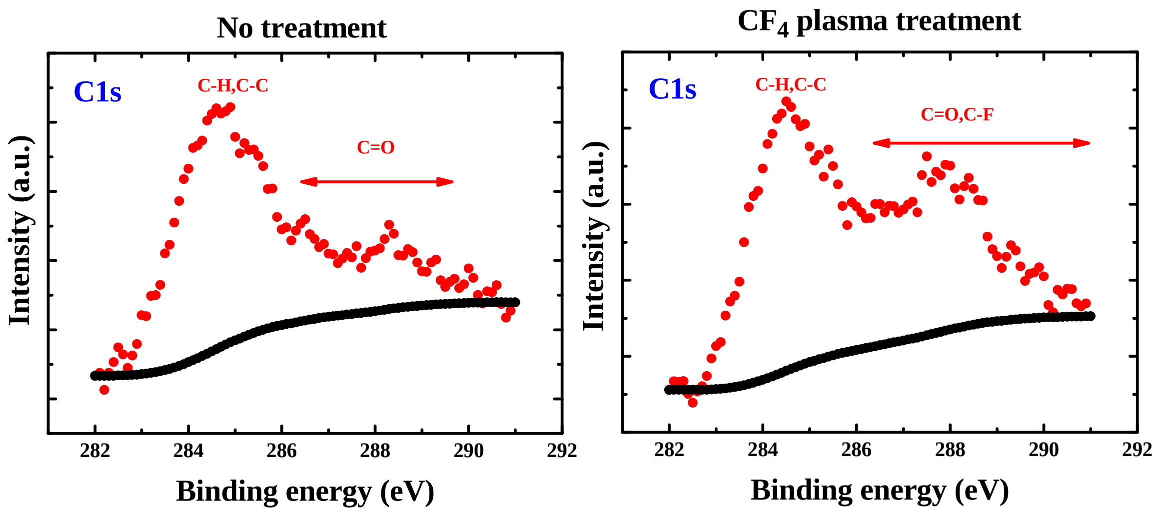


Figure 3 F 1s XPS spectrum for samples with and without CF_4 plasma treatment

F 1*s* XPS spectra in figure 3 show that F is incorporated into HfO_2 for samples with CF_4 treatment. The peak located at ~685 eV corresponds to the F bonds in bulk HfO_2 (10). From C1s XPS spectra shown in figure 4, C-F bond was observed at the surface after plasma treatment.



(a)

(b)

Figure 4 C 1s XPS spectrum for samples (a) without CF_4 plasma treatment (b) with CF_4 plasma treatment

Figure 5 shows the depth profile of SIMS analysis of the HfO_2 films with CF_4 plasma treatment. It can be seen that fluorine is incorporated into bulk HfO_2 film, so that the defects can effectively be passivated in bulk HfO_2.

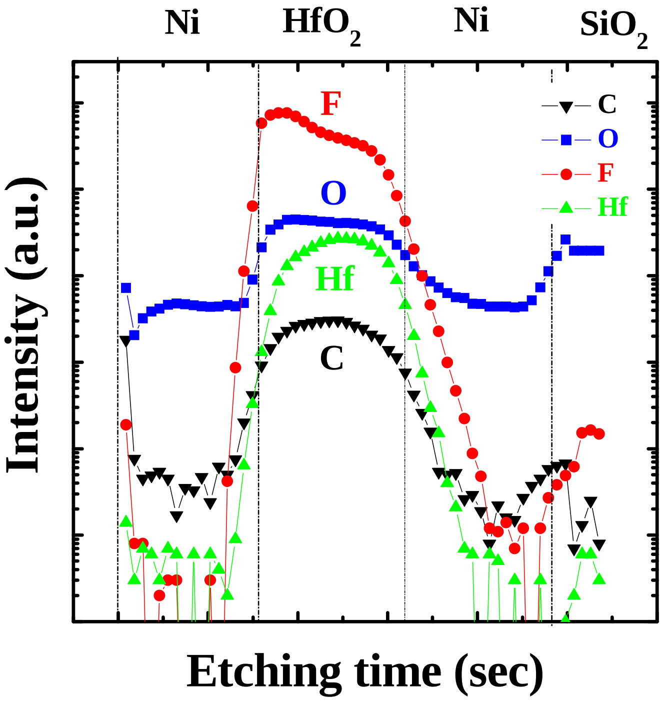
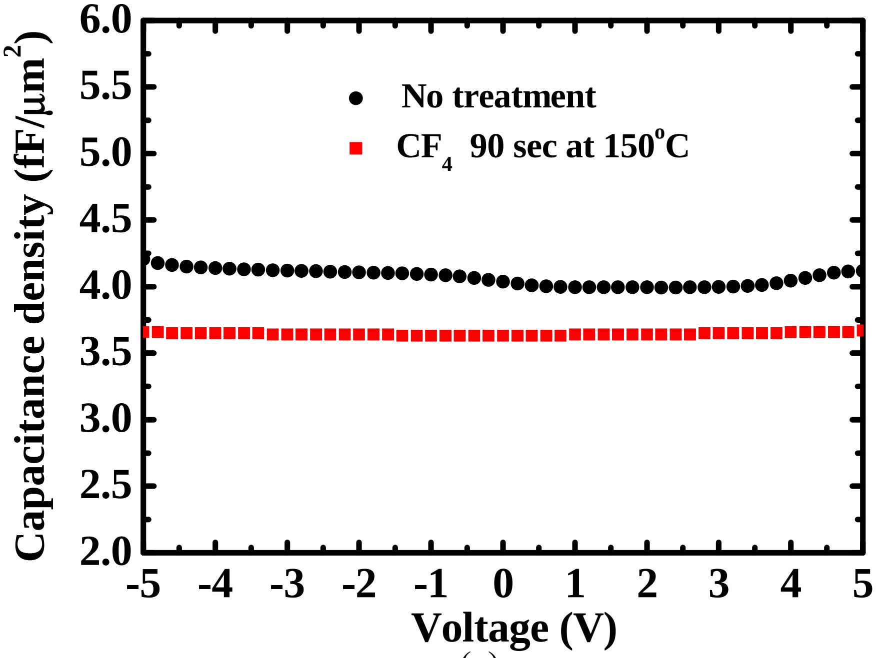
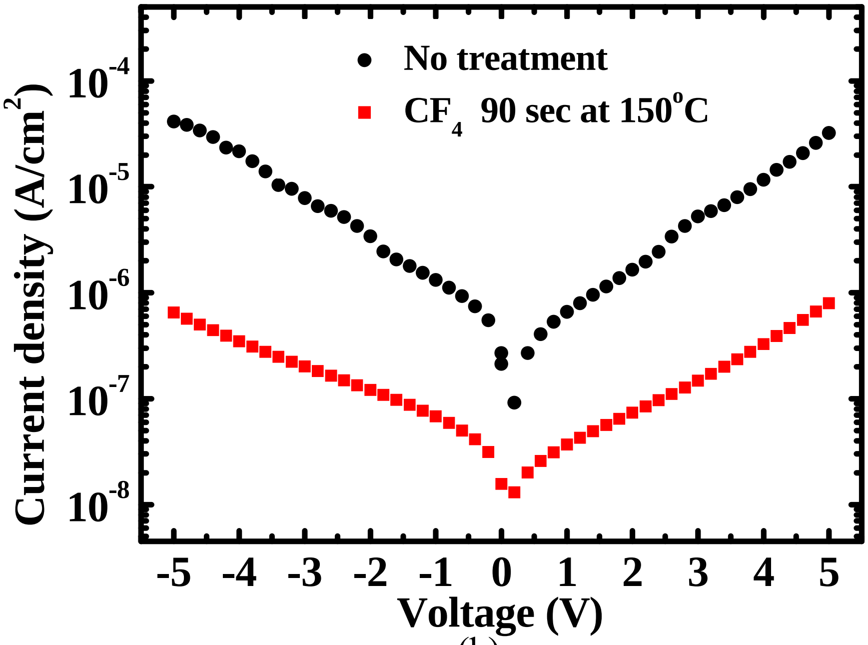


Figure 5 SIMS analysis of Ni/HfO_2/Ni bottom electrode.

The C-V and J–V characteristics of MIM capacitors are shown in figures 6(a) and 6(b), respectively. It is observed that the capacitance slightly declines after plasma treatment. From C1s XPS data, it is deduced that C-F bonding results in a lower capacitance. As shown in figure 6(b), leakage current density of the gate dielectrics was significantly improved with CF_4 plasma at 150 °C in an inductively coupled plasma chamber, and gate dielectric leakage current was $3X10^{-6}$ A/cm^2 at an electric field of 1MV/cm. The results show that fluorine atoms were incorporated into the HfO_2 dielectrics to form Hf–F bonding by CF_4 plasma, resulting in the reduction of gate leakage current (6).



(a)



(b)

Figure 6 (a) C–V characteristics of $Ni/HfO_2/Ni$ capacitors (b) J–V characteristics of $Ni/HfO_2/Ni$ capacitors with and without CF_4 plasma.

Figure 7 shows that the transfer characteristics of OTFTs with HfO_2 gate dielectric treated by annealing for 1 hour at 150 °C in N_2 (control sample), CF_4 plasma and CF_4 plasma followed by HMDS evaporation. Table 1 summarizes the electrical properties of subthreshold swing, on/off ratio, threshold voltage, and the mobility extracted by ID-VG and $ID_{1/2}$ $-V_G$ plot. The mobility is enhanced after gate dielectric was treated by CF_4 plasma and HMDS because of the improvement of carrier transport behavior on pentacene interface of channel/dielectric. Moreover, AFM surface images of pentacene were shown in figure 8. After CF_4 plasma treatment, the grain size was larger resulting in lager mobility than control sample. In Figure 9(a), ID-VD curve of control sample has more distortion due to high gate leakage current and lower mobility. After CF_4 plasma followed by HMDS treatment, the distortion is significantly improved since that F incorporation reduces the leakage current and improves surface property shown in figure 9(c). In figure 9(c), ID-VD shows slightly non-linear property at the low V_{DS} region due to the schottky barrier between pentacene and gold (11-13). In the previous reports, bottom contact structure shows more non-linear behavior than top contact (11, 12). It seems that our top contact structure presents a poor contact. The parasitic resistance in our experimental may result in a lower mobility.

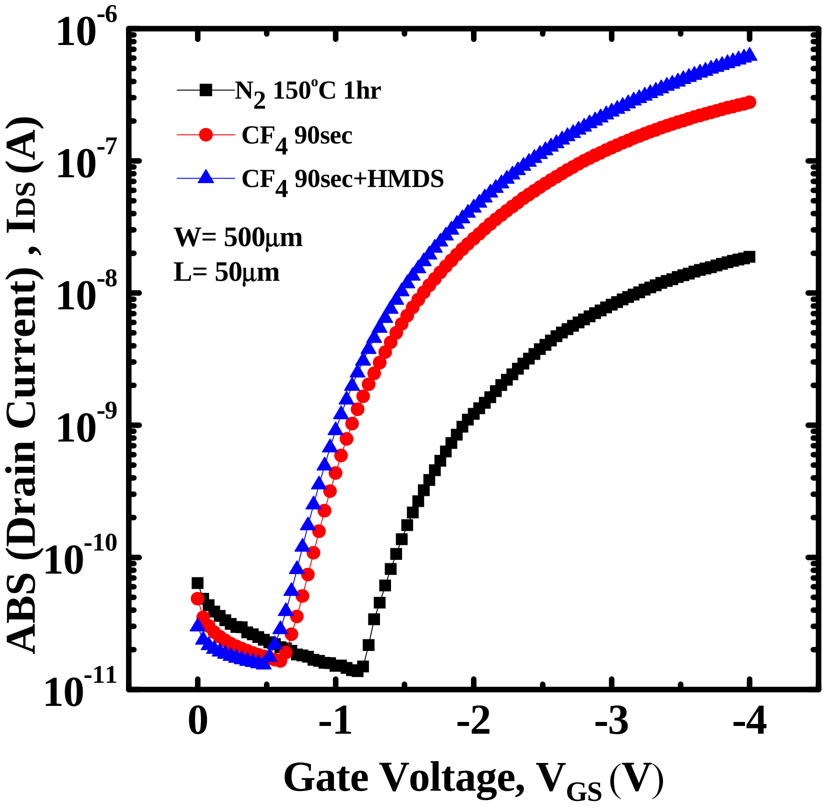
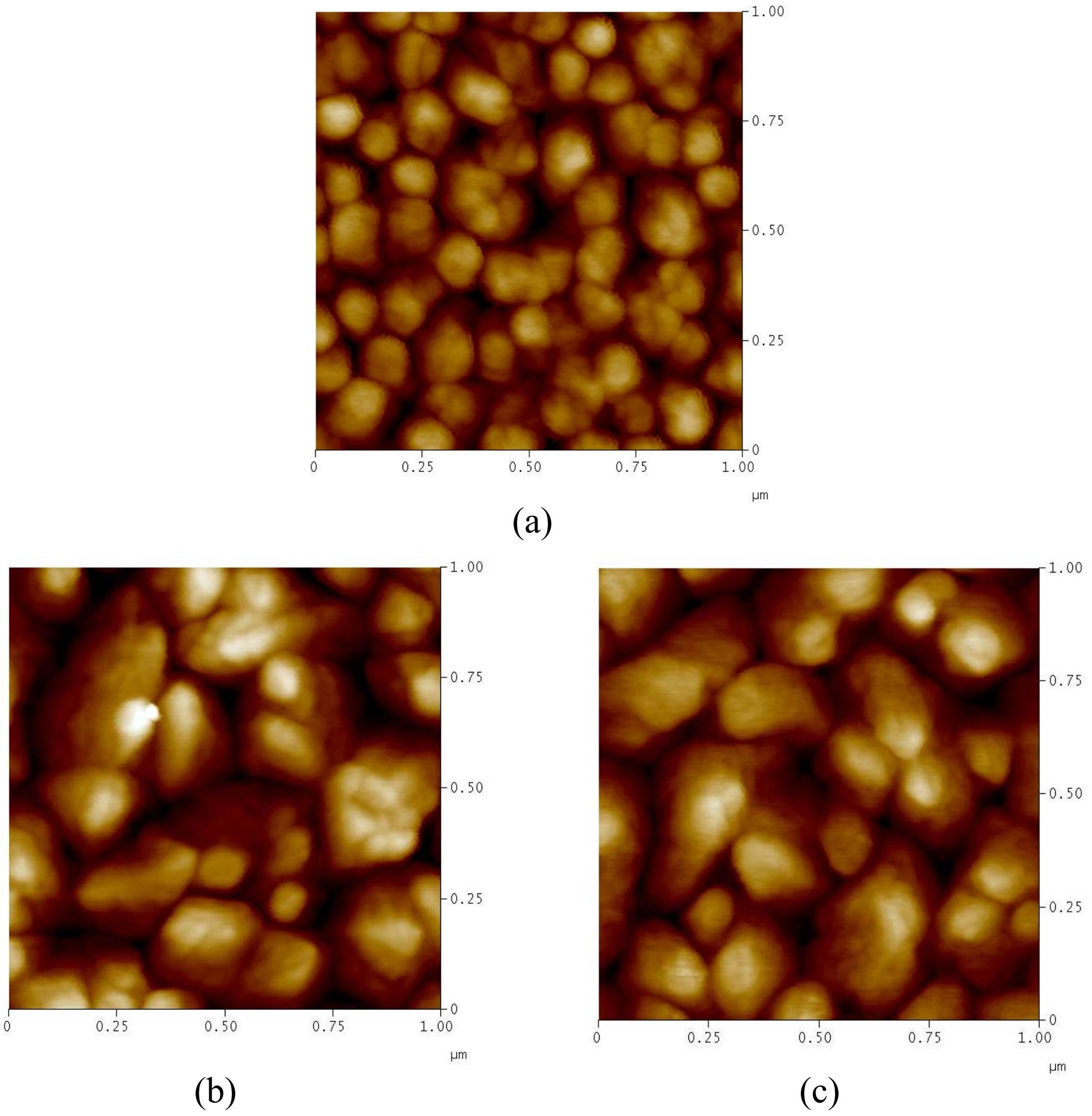


Figure 7 The transfer characteristics of OTFTs with HfO_2 gate dielectric treated by annealing for 1 hour at 150 °C in N_2, CF_4 plasma 90 sec at 150 °C, and CF_4 plasma 90 sec at 150 °C followed by HMDS evaporation treatment.

TABLE I.

	Vt (V)	SS (V/dec.)	Mobility (cm^2/V-s)	Ion/Ioff ratio
N_2 annealing for 1 hour at 150 °C	-1.35	353	1.16×10^{-3}	1.36×10^{3}
CF_4 90sec at 150 °C	-1.18	286	1.82×10^{-2}	1.69×10^{4}
CF_4 90sec at 150 °C +HMDS	-1.12	266	2.90×10^{-2}	4.03×10^{4}

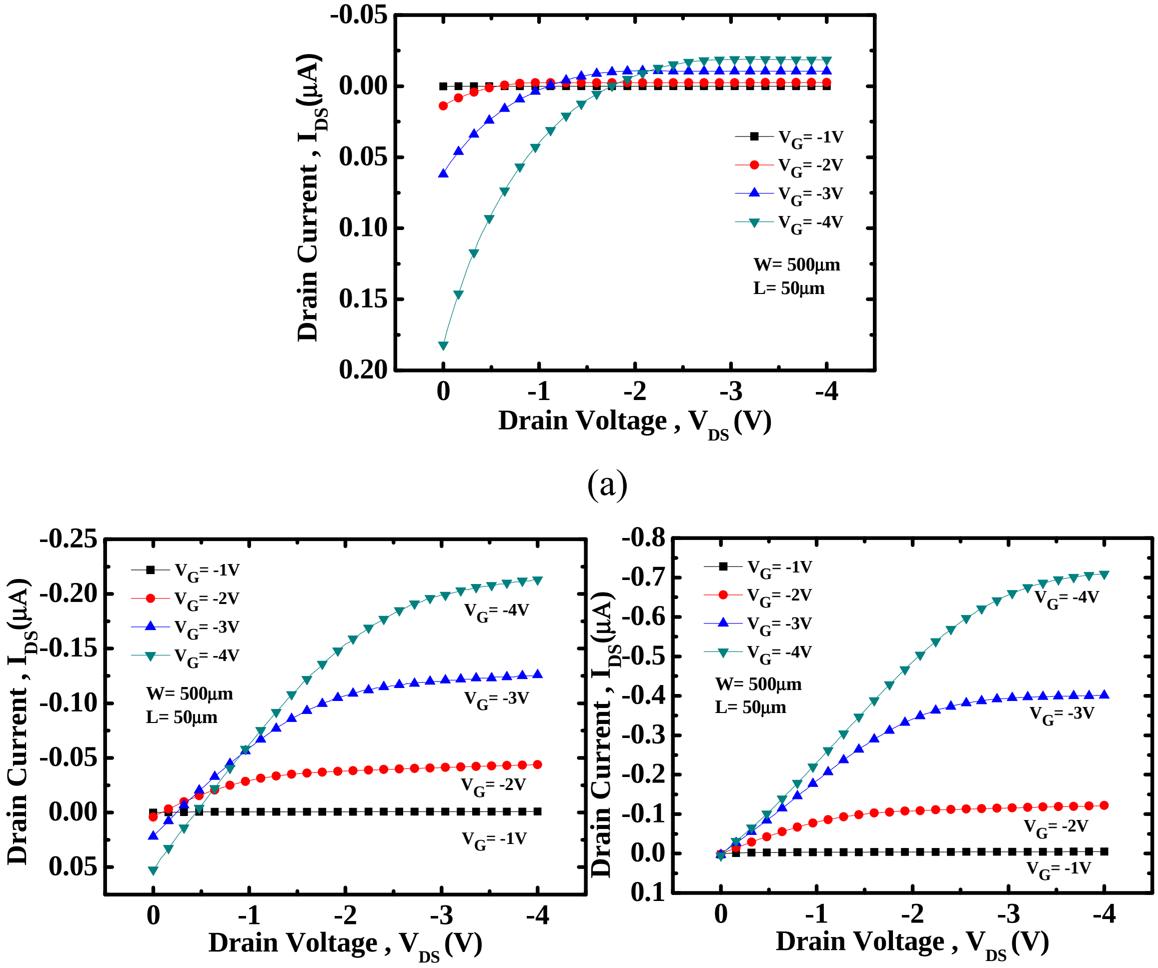


(a)

(b)

(c)

Figure 8 AFM pentacene deposited surface images after gate dielectric treated with (a) annealing for 1 hour at 150 °C in N_2, (b) treated with CF_4 plasma, and (c) treated with CF_4 plasma followed by HMDS evaporation treatment



(a)

(b)

(c)

Figure 9 Output characteristics (*ID–VD*) of OTFTs for (a) annealing for 1 hour at 150 ºC in N_2 (b) CF_4 plasma treated (c) CF_4 plasma followed by HMDS evaporation treatment

Conclusion

In summary, a high-*k* HfO_2 dielectric treated by CF_4 plasma in an inductively coupled plasma chamber was successfully integrated into pentacene-based OTFTs for low processing temperature. Fluorine incorporation into bulk HfO_2 effectively repairs the defect resulting in reduction of leakage current. The formation of C-F bonding at the gate dielectric surface modifies the surface properties resulting in a larger pentacene grain growth. Our pentacene-based OTFT by CF_4 plasma and HMDS evaporation treatment operated at -4V showing a low threshold voltage (-1.12V), a low subthreshold swing (266 mV/decade), a field-effect mobility (0.029 cm^2/Vs) and an on/off current ratio (>10^4).

Acknowledgments

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