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MIXED SIGNAL LETTER

An active device based wide tuning range CMOS transconductor

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Abstract A CMOS transconductor for wide tuning range filter application is presented. The linear transconductor is designed based on the flipped-voltage follower (FVF) circuit and can work in the weak, moderate, and strong inversion regions to maximize the transconductance tuning range. The transconductance tuning can be achieved by changing the bias current of the active resistor, and a ratio of 28 is obtained. The transconductor was evaluated by using TSMC 0.18 μm CMOS process, and the total harmonic distortion (THD) of −56 dB can be obtained by giving a 12 MHz 0.4 Vpp input swing signal. In the design, the maximum power consumption is 2 mW with the transconductance of 1.1 mS under a 1.8 V supply voltage.

Keywords Transconductor · THD · FVF · CMOS

1 Introduction

The trend of the portable solutions tends to include multiple applications in a long-standby system. Cost efficiency has been greatly increased with the emergence of CMOS technology in high performance VLSI implementations. Moreover, to save the silicon area in a standalone system-on-a-chip solution, re-usable circuits for different system applications can be even cost-effective. This study presents a CMOS implementation of a transconductor with a very wide transconductance tuning range for multi-mode applications. The transconductor, which performs the voltage-to-current conversion, is a basic building block in the continuous-time filters [1]. There are numerous works to improve the transconductor linearity [2–5], but the reported technology is not suitable for wide tuning range applications. In the letter, a high performance linear circuit with the use of an active equivalent resistor is designed based on the flipped-voltage follower (FVF) [6] structure. The equivalent resistor circuit could operate in the weak, moderate, and strong inversion regions to achieve a wide transconductance tuning range, and the tuning ability can be achieved by adjusting the bias current.

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2 Proposed transconductor circuit and performance

Figure 1(a) shows the implementation of the transconductor, and the circuit is designed based on the FVF structure. The FVF structure composed by transistors M1 (M2), M3 (M4), and bias current Ib is a very efficient low-voltage implementation. Because the follower is biased at the drain terminal rather the source terminal, the circuit behaves as the conventional source follower with even lower output impedance. Due to the shunt feedback through transistor M3 (M4), the equivalent impedance at the source of transistor M1 (M2) is given by

$$\mathrm{Ro_{eq}} = \frac{1}{\mathrm{gm_1 gm_3 ro_1}} \quad (1)$$

where parameters gmi and roi are the transconductance and the output resistance of transistor Mi, respectively. The output resistance is a relatively low impedance value

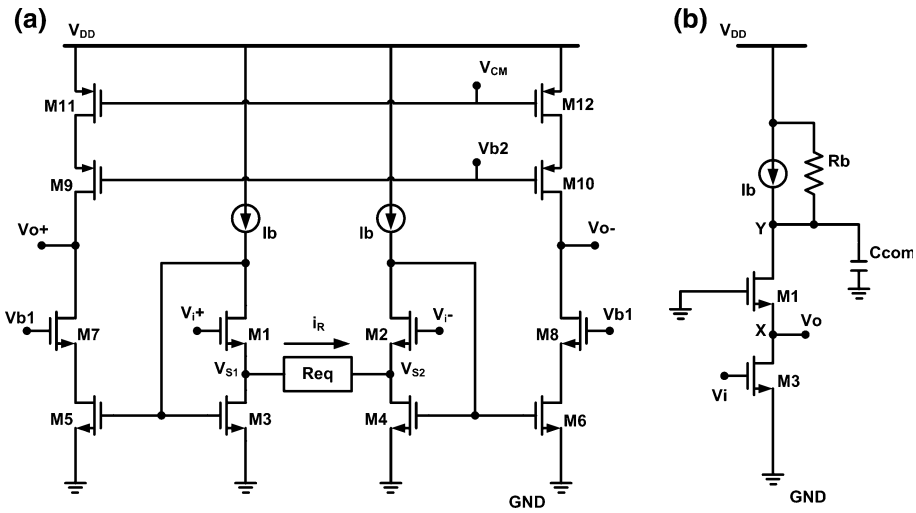

Fig. 1 a The proposed transconductor circuit. b Open loop model of the FVF circuit

compared with the conventional structure, and some of the design constrain can be relaxed under the FVF structure as well. In the proposed circuit, an equivalent resistor Req is used to perform the voltage-to-current conversion. The input voltage $V_{\text{in}} = V_{\text{i}} + -V_{\text{i}}-$ is applied to the resistor through the very low output impedance buffers. Thus, the negative feedback loop would force $V_{\text{i}} + -V_{\text{i}}- = V_{\text{S1}} - V_{\text{S2}}$ to perform the voltage-to-current conversion. We can find that the current $i_{\text{R}} = (V_{\text{i}} + -V_{\text{i}}-)/\text{Req}$, and thus the transconductance would be affected by the value of the equivalent resistance. The current flowing through transistor M3 (M4) is mirrored to transistor M5 (M6) while the drain current I_{D1} (I_{D2}) would be biased to the current source Ib. In addition, the cascode output stage is used to maintain the required gain of the transconductor. The stability of the transconductor is determined by the stability of the FVF buffers, and thus the stability of shunt feedback should be taken into consideration. For the FVF circuit, if we open the loop at the gate of M3 and provide a test voltage source, as illustrated in Fig. 1(b), the open loop gain of $\text{AOL} = -\text{gm}_1\text{ROLY}$ would be obtained, where ROLY is the equivalent impedance at node Y. The circuit has a dominant pole at node Y which equals to 1/ROLYCY and a non-dominant pole at node X which equals to 1/ROLXCX, where ROLX is the equivalent impedance at node X. For stability issues, the non-dominate pole should be larger then twice the gain bandwidth of the circuit, and thus the constrain $\text{CX/CY} < \text{gm}_1/4\text{gm}_3$ should be maintained. The condition is easily achieved by proper sizing of transistors M1 (M2) and M3 (M4). Moreover, to further improve circuit stability, a compensating capacitor Ccom could be also added at the drain node of transistor M1 (M2).

In order to add the tuning ability for the transconductor, active devices, instead of a passive resistor, are used to implement an equivalent resistor with the drawback of the degraded linearity performance. Figure 2 shows the equivalent resistor circuit. If the transistors MR1 and MR2 are working in the saturation region, we could find that

$$i_{\text{R1}} = I_{\text{Tune}} - i_{\text{R}} = \frac{1}{2}K(V_{\text{G}} - V_{\text{S1}} - V_{\text{th}})^2 \tag{2}$$

$$i_{\text{R2}} = I_{\text{Tune}} + i_{\text{R}} = \frac{1}{2}K(V_{\text{G}} - V_{\text{S2}} - V_{\text{th}})^2 \tag{3}$$

where K is the MOS strong inversion parameter and V_{th} is the MOS threshold voltage. By subtracting Eq. 2 from Eq. 3, the current i_{R} which flows through the equivalent resistor would be given by

$$i_{\text{R}} = \frac{1}{4}K(V_{\text{S1}} - V_{\text{S2}})[2(V_{\text{G}} - V_{\text{th}}) - (V_{\text{S1}} + V_{\text{S2}})] \tag{4}$$

When we combine the equivalent resistor circuit into the transconductor, as shown in Fig. 1(a), the DC voltage at nodes V_{S1} and V_{S2} could be defined as

$$V_{\text{S1}} = V_{\text{cm}} + \frac{V_{\text{d}}}{2} - V_{\text{SF}} \tag{5}$$

$$V_{\text{S2}} = V_{\text{cm}} - \frac{V_{\text{d}}}{2} - V_{\text{SF}} \tag{6}$$

where V_{cm} is the input common-mode voltage, V_{d} is the input differential-mode voltage, and V_{SF} is the voltage shift from the FVF circuit. By substituting 5 and 6 into 4, we can obtain

$$i_{\text{R}} = \frac{1}{2}KV_{\text{d}}(V_{\text{G}} - V_{\text{th}} - V_{\text{cm}} + V_{\text{SF}}) \tag{7}$$

From Eq. 7, we can find that the output current has a linear relationship with the input voltage, and the transconductance can be tuned by adjusting the gate voltage of

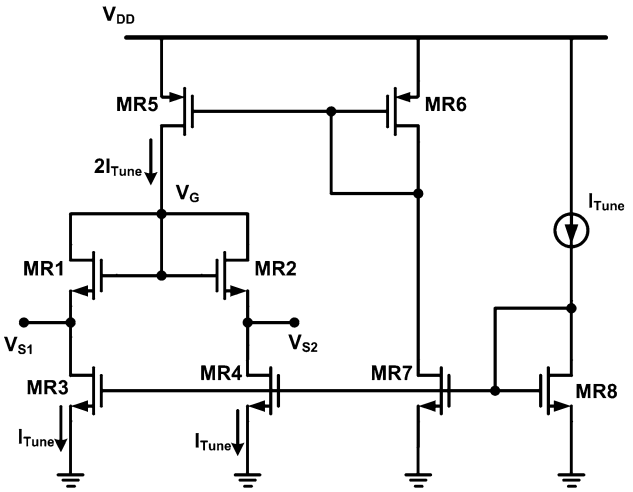

Fig. 2 The equivalent resistor circuit

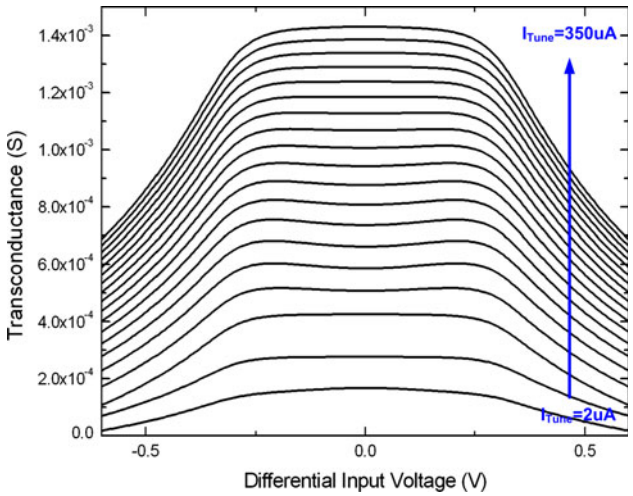

Fig. 3 The Gm range of the proposed transconductor

transistors MR1 and MR2. In our final resistor circuit implementation, the bias current I_{Tune} could be changed to choose the gate voltage and thus the transconductance can also be tuned, as shown in Fig. 2. The above design carried out was analyzed based on the assumption that transistors operate in the strong inversion region. However, if the provided current I_{Tune} is small enough, the equivalent resistor would operate in the moderate or weak inversion region to provide smaller transconductance. Similar analysis can be also performed by giving

$$i_{\text{R1}} = I_{\text{Tune}} - i_{\text{R}} = I_{\text{D1}} \exp\left(\frac{V_{\text{G}} - V_{\text{S1}}}{nU_{\text{T}}}\right) \tag{8}$$

$$i_{\text{R2}} = I_{\text{Tune}} + i_{\text{R}} = I_{\text{D1}} \exp\left(\frac{V_{\text{G}} - V_{\text{S2}}}{nU_{\text{T}}}\right) \tag{9}$$

where I_{D1} is the reverse saturation current, n is the subthreshold slope factor, and U_{T} is the thermal voltage. By subtracting Eq. 8 from Eq. 9 and substituting Eqs. 5 and 6 into it, the output current which could be approximated through a Taylor series expansion is given by

$$i_{\text{R}} = V_{\text{d}} \left(\frac{I_{\text{D1}}}{nU_{\text{T}}}\right) \left(1 + \frac{V_{\text{G}} - V_{\text{cm}} + V_{\text{SF}}}{nU_{\text{T}}}\right) \tag{10}$$

Again, the linear relationship confirms the circuit operation and thus the proposed transconductor can operate to achieve a wider tuning range for multi-mode wireless applications.

The transconductor was designed in the TSMC 0.18 μm Deep N-WELL CMOS process, and thus body effects can be simply eliminated by connecting the source and the bulk terminals together in the design. Figure 3 shows the large signal simulation with respect to the function of differential input voltage. The magnitude of Ib is 200 uA in this design. When the current Ib is large, the gate voltage of transistors M3 and M4 becomes large and the source voltage of transistors M1 and M2 becomes small. Therefore, transistors M3 and M4 will enter the triode region under large input swing, and the linearity performance is degraded. On the opposite, when the current Ib is small, transistors M3 and M4 will enter the weak inversion region, and thus the limited transconductance is shown. In this design, the required transconductance and linearity should be maintained, and the optimal value of current Ib is swept by simulation. The tuning range of the transconductance is from 50 uS to 1.4 mS. Compared with the traditional tuning range ratio of less than 5 [7], the ratio of the proposed circuit is 28, and a wide tuning range is achieved. In 7 and 10, the value of voltage V_{G} is defined by the tuning current I_{Tune}, and the calculated value of equivalent resistance is 5 K. When we adjust the bias current, the value changes from 1 to 30 K and the result is consistent with simulation. We should note that a small aspect ratio of transistors MR1 and MR2 is required, so the equivalent resistance circuit is biased from weak inversion region to saturation region. For the linearity performance, the simulated THD of −56 dB is obtained by giving a 12 MHz 0.4Vpp input swing signal under a power consumption of 2 mW.

3 Conclusions

A CMOS implementation of a wide tuning range transconductor is presented. The transconductor is designed based on the FVF structure and an equivalent resistor circuit. Instead of a passive resistor, the active resistor could work in the weak, moderate, and strong inversion regions to extend the transconductance tuning range. Through the use of the transconductor as a building block, we can

design the multi-mode circuit for the wireless and mobile applications. The theoretical analysis of the high performance operation and the simulation results are provided to demonstrate the validity of the transconductor.

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