Diode-Triggered Silicon-Controlled Rectifier With Reduced Voltage Overshoot for CDM ESD Protection

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***Abstract*—Diode-triggered silicon-controlled rectifiers (DTSCRs) are used for on-chip electrostatic discharge protection. The role of the trigger diode string in determining the transient voltage overshoot is investigated using a very fast transmission line pulse. A DTSCR containing only poly-bound trigger diodes has a voltage overshoot of just 1.5 V at 7 A, which is significantly less than what is found with STI-bound diodes. A DTSCR with only STI-bound trigger diodes has a lower leakage current. Therefore, DTSCRs with different trigger diode configurations may be suitable for different applications, e.g., high speed or low power.**

***Index Terms*—Charge device model (CDM), electrostatic discharge (ESD), silicon-controlled rectifier (SCR).**

I. Introduction

SILICON-CONTROLLED RECTIFIER (SCR) devices safely handle high current densities, making them attractive for electrostatic discharge (ESD) protection [1]. Various designs have been proposed to further improve the ESD protection efficiency of SCR. For example, the structure in [2] utilizes a dummy-gate structure to improve the turn-on speed of the SCR device. Among the various SCR-based ESD protection designs, the diode-triggered SCR (DTSCR) prevails in advanced CMOS technologies due to its design simplicity [3], [4]. When SCR-based protection devices are subject to nanosecond-scale discharges, such as charged device model (CDM) ESD, they are often unable to clamp the pad voltage below the breakdown voltage of thin gate oxides, particularly in sub-100-nm CMOS technologies [5]–[10]. Although the holding voltage of a typical SCR is about 1.5 V, the device cannot be switched instantly from off to on; if the applied ESD pulse has a subnanosecond rise time, a transient voltage overshoot is observed [11], and it requires that the SCR be augmented by an additional protection element [12], [13]. Before the SCR fully turns on, the voltage across its terminals is determined by the trigger circuit [14]. This observation suggests that one should employ a trigger circuit that turns on quickly to provide good voltage clamping.

At high frequencies, diodes exhibit inductive characteristics as a result of conductivity modulation [15]. This indicates that the diode string trigger circuit of a DTSCR will itself display some transient voltage overshoot [14]. In a given technology node, poly-bound diodes [16] have smaller voltage overshoot than do STI-bound diodes, a result of the shorter base region [17]. It follows that a DTSCR built using poly-bound diodes should provide better voltage clamping than would one built using STI-bound diodes. This work evaluates that conjecture by means of experiments performed on DTSCR devices fabricated in a 65-nm low-power CMOS technology.

TABLE I
TEST STRUCTURES STUDIED IN THIS WORK

	Acronym in Text / Figures	Type of Diode Intrinsic to the SCR (D_1)	Type of External Trigger Diodes (D_2, D_3, and D_4)
A	STI-DTSCR	STI-bound	all STI-bound
B	Diode-String	STI-bound (no SCR action, SCR cathode removed)	all STI-bound
C	Mix-DTSCR	STI-bound	all Poly-bound
D	Poly-DTSCR	Poly-bound	all Poly-bound

II. Experiment

The test structures used in this work are listed in Table I. The DTSCRs all contain three external p^+/n-well diodes, labeled as D_2, D_3, and D_4 in Fig. 1(a). D_2, D_3, and D_4 each have a p-n junction perimeter of 200 μm. In test structure A (STI-DTSCR), these are STI-bound diodes with a p^+-to-n^+ spacing of 360 nm. Test structure B (Diode-String) is similar to A, except that the n^+ cathode of the SCR has been removed, disabling the SCR and allowing one to observe the characteristics of just the diode string. In test structure C (Mix-DTSCR), D_2, D_3, and D_4 are poly-bound diodes with a p^+-to-n^+ spacing (gate width) of 65 nm. Test structure D (Poly-DTSCR) is similar to C, except that D_1, the trigger diode integrated within the SCR, has been changed from STI-bound to poly-bound. The cross section of a Poly-DTSCR is shown in Fig. 1(b).

In all cases, the SCR has an effective width of 50 μm; this also means that D_1 has a 50-μm perimeter. The SCR

Manuscript received July 19, 2011; revised September 7, 2011 and September 26, 2011; accepted October 1, 2011. Date of publication October 13, 2011; date of current version March 7, 2012. This work was supported in part by the National Science Council, Taiwan, under Contract NSC 98-2221-E-009-113-MY2 and in part by the "Aim for the Top University Plan" of National Chiao Tung University and the Ministry of Education, Taiwan. The work of W.-Y. Chen was supported by the Graduate Students Study Abroad Fellowship from the National Science Council, Taiwan. The work of E. Rosenbaum was supported by the SRC.

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Digital Object Identifier 10.1109/TDMR.2011.2171487

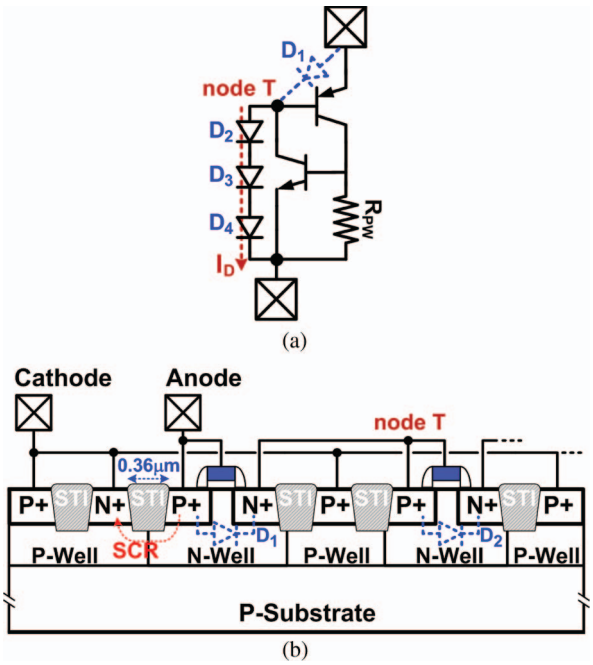

Fig. 1. (a) Schematic representation of the DTSCRs used in this work and (b) cross section of a Poly-DTSCR.

anode-to-cathode spacing ($S_{\rm ac}$) was fixed at the minimum value allowed by the layout design rules, which is 0.36 μm, so as to minimize the intrinsic turn-on delay of the SCR [4].

A very-fast transmission line pulse (vf-TLP) system is used to generate pulses with a pulse width of 5 ns and a rise time of 100 ps [18], [19]. These pulses are applied to the DTSCRs, and the device response is recorded using a 12-GHz oscilloscope.

III. VF-TLP Results and Discussion

A single quasi-static I–V point is obtained from the vf-TLP data by averaging the current and voltage over a 500-ps interval, starting 3 ns after the pulse rising edge (see Fig. 3). The resulting I–V curves are shown in Fig. 2(a). There are three regions in the quasi-static I–V curve: (I) SCR is off, and $\overline{V_{\rm DUT}} < V_{t1}$, where V_{t1} is the on-voltage of the diode string; (II) SCR is on; and (III) SCR is on, and the diode string is also on, because $\overline{V_{\rm DUT}} > V_{t1}$. In regions I and II, the three DTSCRs have nearly identical quasi-static I–V characteristics. In region III, where the SCR and the diode string provide parallel paths for the ESD current, the Poly-DTSCR has lower on-resistance than the other two DTSCRs because the poly-bound diodes have a smaller static $R_{\rm on}$ than the STI-bound diodes.

In Fig. 2(b), the current is instead plotted as a function of the peak voltage appearing across the device under test (DUT). The STI-DTSCR and the Diode-String have nearly identical I–V characteristics, at least for $V_{\rm peak} < 13$ V, highlighting that $V_{\rm peak}$ is determined by the trigger circuit, not the SCR. Changing the SCR-based structure from STI-DTSCR to Poly-DTSCR dramatically reduces the amount of voltage overshoot ($V_{\rm OV}$), not only because the poly-bound diodes have a lower static $R_{\rm on}$ than STI-bound diodes but also because they display less inductive behavior.

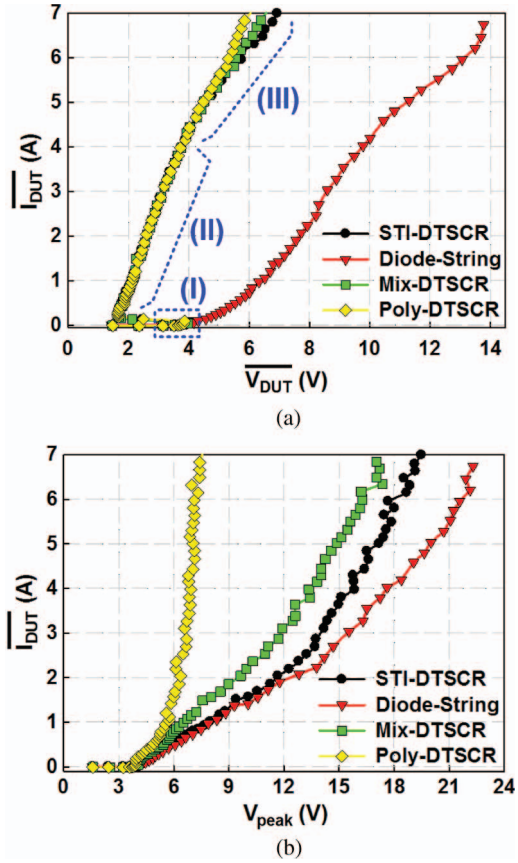

Fig. 2. (a) Quasi-static I–V characteristics and (b) peak overshoot voltage versus quasi-static current for the different test structures. Data extracted from vf-TLP.

Two additional observations are made in regard to the data in Fig. 2(b). First, the Mix-DTSCR provides only marginally better voltage clamping than does the STI-DTSCR. Defining $V_{\rm OV} = V_{\rm peak} - \overline{V_{\rm DUT}}$, the Mix-DTSCR provides only about a 2-V reduction in $V_{\rm OV}$ at 7 A. This result indicates that, in the Mix-DTSCR, the STI-bound diode $\rm D_1$ dominates the total impedance of the current path from $\rm D_1$ to $\rm D_4$, at least on the subnanosecond time scale.

Second, the I–V curve for the Mix-DTSCR shows a gradual slope change starting at around 12 V, which is the n-well/p-well junction breakdown voltage; this is attributed to avalanche-generated electrons flooding the n-well of $\rm D_1$ and reducing its on-resistance. This effect is not seen in the I–V curves of the STI-DTSCR and the Diode-String because their on-resistances are dominated by the STI-bound diodes $\rm D_2$, $\rm D_3$, and $\rm D_4$; in contrast, the I–V curves for these devices undergo a sudden slope change at about 13.5 V. This has been attributed to n-well/p-well junction breakdown followed by the triggering of the parasitic SCR between the $\rm p^+$ of $\rm D_1$ and the $\rm n^+$ of $\rm D_4$, which provides an additional current path in parallel with the trigger circuit [14]; the parasitic SCR is triggered at a voltage higher than the 12-V junction breakdown voltage because each diode in the DTSCR is surrounded by a $\rm p^+$ guard ring [see Fig. 1(b)] [20]. The Diode-String's quasi-static I–V curve [Fig. 2(a)] similarly undergoes a slope change at 13.5 V.

In Fig. 3, $V_{\rm DUT}(t)$ for all three DTSCRs is plotted for pulses with $\overline{I_{\rm DUT}} = 2$ A. The voltage across the Poly-DTSCR

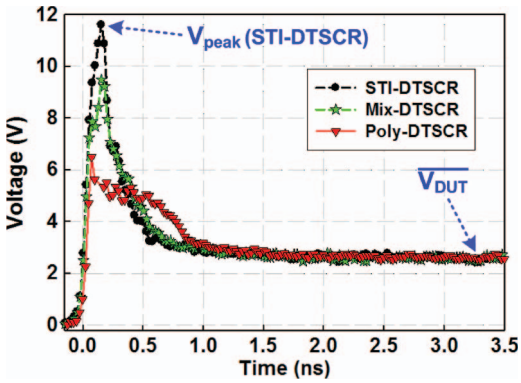

Fig. 3. VF-TLP. Measured voltage waveforms for different DTSCRs.

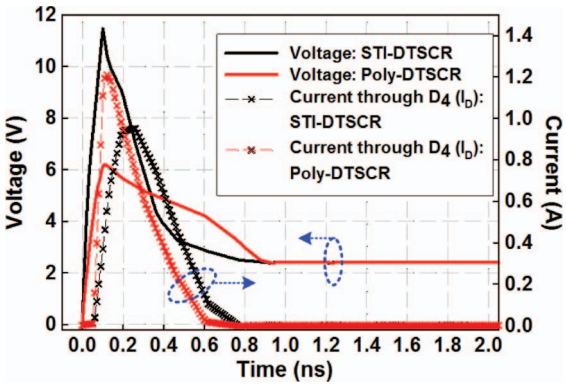

Fig. 4. Simulated transient waveforms for STI-DTSCR and Poly-DTSCR.

is clamped to 6 V, whereas it nearly reaches 10 V in the Mix-DTSCR and exceeds 11 V in the STI-DTSCR. However, the Poly-DTSCR reaches its steady-state voltage more slowly, with $V_{\rm DUT}(t)$ showing a shoulder rather than collapsing rapidly toward its final value. In fact, between 0.5 and 0.9 ns, the voltage across the Poly-DTSCR is higher than that across the STI-DTSCR or the Mix-DTSCR. To understand this result, the transient responses of STI-DTSCR and Poly-DTSCR were simulated using Cadence Virtuoso Spectre. The trigger diodes are modeled using the same approach presented in [21]. The SCRs are modeled as cross-coupled n-p-n and p-n-p transistors; model parameters are provided by the foundry based on the Gummel–Poon BJT model. The simulation results are shown in Fig. 4; the simulated $V_{\rm DUT}(t)$ looks quite similar to $V_{\rm DUT}(t)$ obtained from vf-TLP measurement. The simulated current in D_4 (i.e., through the diode string), I_D, is also plotted in Fig. 4. I_D for the STI-DTSCR has a slower rise time than that for the Poly-DTSCR, and I_D continues to flow at later time points in the STI-DTSCR. I_D augments current flow through the SCR, thereby helping to reduce the voltage at the anode; a faster turnoff of I_D removes the supplemental current path. In the Poly-DTSCR, once the diode string turns off, the decay of the anode voltage is determined solely by the intrinsic SCR and is a relatively slow process. Despite the shoulder in its $V_{\rm DUT}(t)$, the Poly-DTSCR is still the best CDM ESD protection device among the investigated DTSCRs due to its substantially reduced peak voltage.

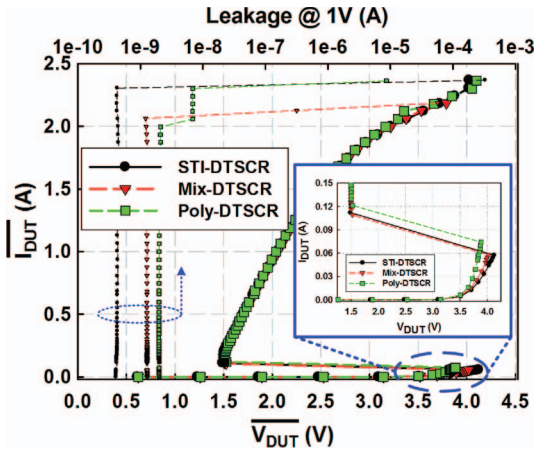

Fig. 5. Quasi-static I–V characteristics of different DTSCRs, extracted from 100-ns TLP.

TABLE II
MEASUREMENT RESULTS OF DIFFERENT DTSCRS

	Vf-TLP	100-ns TLP			ΔC	Leakage @ 1V
	V_{OV} @ 7 A	I_{t1}	V_{t1}	I_{fail}		
STI-DTSCR	12.6 V	57.3 mA	4.12 V	2.36 A	—	420 pA
Mix-DTSCR	10.6 V	58 mA	4.02 V	2.12 A	+16 fF	1.27 nA
Poly-DTSCR	1.5 V	74.1 mA	3.88 V	2.06 A	+37 fF	2 nA

IV. ADDITIONAL PERFORMANCE METRICS

Quasi-static I–V characteristics obtained from 100-ns TLP [22] measurements are shown in Fig. 5. Because all DTSCRs have the same anode-to-cathode spacing, all three DTSCRs have the same holding voltage of 1.5 V. The trigger voltage and current V_{t1} and I_{t1} are obtained from the data shown in the figure inset. The failure current $(I_{\rm fail})$ is defined as the TLP current which causes the leakage (measured at 1 V) to increase by more than 10%. The test structure layout did not permit for measurement of the device S-parameters, which would allow for accurate measurement of the capacitance with the bondpads and other parasitics de-embedded. However, using an LCR meter to measure the total capacitance of each structure, one can easily observe the incremental increase in capacitance as the trigger diodes are changed from STI-bound to poly-bound. The values of $V_{\rm OV}$, V_{t1}, I_{t1}, $I_{\rm fail}$, and C are listed in Table II. The Poly-DTSCR has slightly reduced $I_{\rm fail}$, slightly increased capacitance, and greatly increased leakage (5×) relative to the STI-DTSCR.

The dc I–V characteristics of stand-alone diodes are shown in Fig. 6. Below 0.6 V, the gate leakage current dominates the junction leakage current, and the poly-bound diode conducts more current than the STI-bound diode. The large leakage current of poly-bound diodes explains why the Poly-DTSCR has higher leakage current than the STI-DTSCR. The poly-bound diodes used in this work each have their gate tied to their anode, i.e., the p^+ side. The measurement results in Fig. 6 suggest that the leakage current of a Poly-DTSCR can likely be reduced below the value shown in Table II simply by changing the gate connection from the anode to the cathode

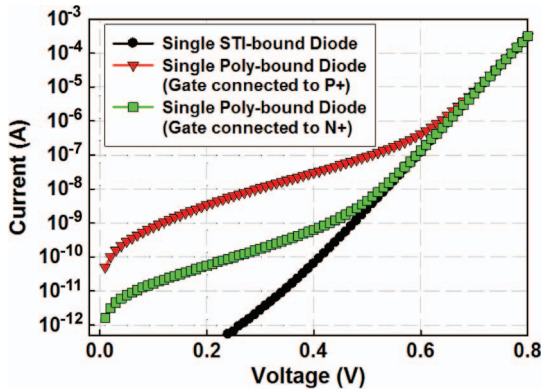

Fig. 6. DC I–V characteristics of a single STI-bound diode and a single poly-bound diode with varying gate connections. Both diodes have the same p-n junction perimeter of 200 μm.

(p^+ to n^+). Measurement results indicate that such a change also reduces the capacitance of the diode and does not affect its ESD performance, results confirmed by the data in [23] and [24].

V. Conclusion

The trigger circuit used with an SCR-based ESD protection device determines the magnitude of the voltage overshoot that occurs before the SCR fully turns on. Poly-bound diodes exhibit reduced voltage overshoot relative to STI-bound diodes; this work demonstrates that, when poly-bound diodes are integrated into a DTSCR, the resulting structure provides very good voltage clamping (an experimental finding recently confirmed by others [25]). All the diodes in the trigger circuit, including the diode intrinsic to the SCR, must be poly-bound to obtain the benefit.

Depending on whether low power or high speed is the design objective, either an STI-DTSCR or a Poly-DTSCR may be the better selection. The STI-DTSCR has significantly lower leakage current and can be augmented by a secondary protection circuit in order to provide CDM ESD protection. However, the secondary protection will reduce the performance of radio-frequency or high-speed input/output circuits. The Poly-DTSCR reduces the need for a secondary protection at the cost of increased leakage current.

Acknowledgment

Test structures were fabricated under the TSMC University Shuttle Program.

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