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Minimizing variation in the electrical characteristics of gate-all-around thin film transistors through the use of multiple-channel nanowire and NH_3 plasma treatment

Po-Chun Huang [a], Lu-An Chen [b], Chen-Chia Chen [b], Jeng-Tzong Sheu [b,*]

[a] Department of Materials Science and Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 30050, Taiwan
[b] Institute of Nanotechnology/Department of Materials Science and Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 30050, Taiwan

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ABSTRACT

In this paper we describe the electrical performance of gate-all-around (GAA) thin-film transistors (TFTs) featuring poly-Si multiple-channel nanowires (NWs). To minimize the variations in the electrical characteristics of GAA NW TFTs, we compared the effects of several approach, including the use of a multiple-gate structure, the number of multiple channels, and NH_3 plasma treatment. We demonstrated not only the gate configuration but also the presence of multiple channels efficiently reduced the variation in the electrical characteristics. Finally, NH_3 plasma treatment of the GAA NW TFTs featuring multiple channels further decreased the electrical variations because it decreased the trap density, which modulated device performance.

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1. Introduction

Although polysilicon thin-film transistors (poly-Si TFTs) are attracting much attention for their use in active-matrix liquid crystal displays [1,2], fine-grain structures in the channel can affect their carrier transport and device performance. Poly-Si consists of a number of single-crystal grains. Between poly-Si grains, there exists a high defect density region called grain boundary with a typical value of defect density ca. 10^{12} cm^{-2}. Such a large number of randomly oriented grain boundaries usually cause large variations in the device's electrical characteristics, including the threshold voltage and subthreshold swing (SS) [3]. Hence, several methods, including excimer laser annealing [4] and metal-induced lateral crystallization [5], have been developed to increase the grain size and minimize grain boundary defects and, thereby, improve the electrical characteristics of poly-Si TFTs. Recently, a multiple-gate structure was reported in which the additional electric field enhanced the control over the channel surface potentials and the device performance, providing improved immunity to short channel effects [6,7]. In addition, TFT characteristics are dramatically improved upon reducing the channel width, particularly when using a nanowire (NW) as channel [8,9]. Poly-Si TFTs featuring multiple NW channels can exhibit improved performance relative to that of traditional planar devices because of the increment of effective channel width and the reduced grain boundary trap density in the channel region [10,11]. When the channel width is on the order of the poly-Si grain size the random distribution of grain boundary causes even greater electrical fluctuation including threshold voltage and SS [9,12,13]. Therefore, uniformity of the grain boundary is critical when scaling down device dimensions.

In a previous study [7], we found that a gate-all-around (GAA) poly-Si NW TFT exhibited excellent gate controllability because the GAA structure enhanced the electric field. In this present study, we investigated the performance of GAA NW TFTs featuring multiple gate configurations; in particular, we compared tri-gate and GAA structures and studied the impact of multiple channels to further reduce the fluctuations in device performance. Indeed, the variations in threshold voltage and SS were effectively modulated. Finally, we found that NH_3 plasma treatment further minimized the fluctuations and further improved the performance of these GAA NW TFTs.

2. Experiment

The 1-μm-long multiple channels of the poly-Si NWs were fabricated using a spacer patterning technique [7]. At first, the 75-nm-thick undoped amorphous-Si (α-Si) layer was deposited

* Corresponding author.
E-mail address: jtsheu@faculty.nctu.edu.tw (J.-T. Sheu).

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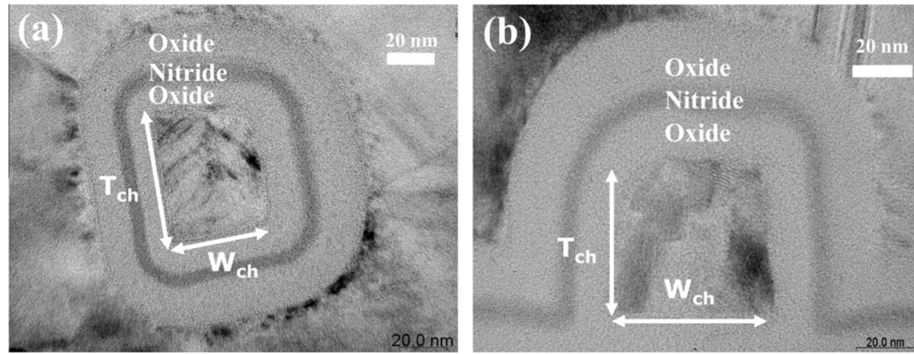

Fig. 1. TEM images of (a) GAA and (b) tri-gate devices having a channel thickness of 62 nm and a channel width of 44 nm. The ONO stack (O/N/O = 10.5 nm/5.5 nm/15.3 nm) was prepared through conformal deposition using LPCVD.

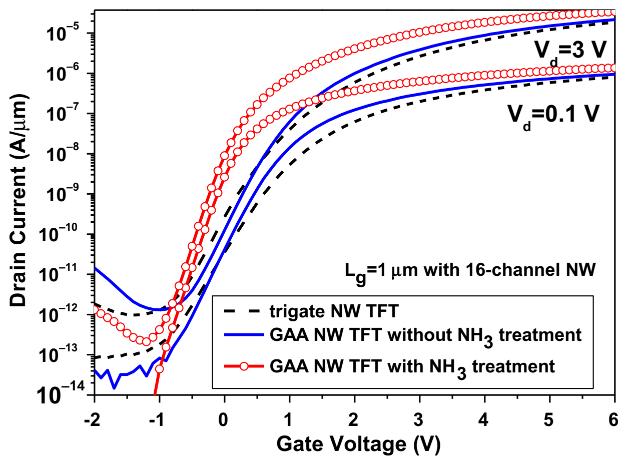

Fig. 2. The comparison of transfer curves for GAA and tri-gate NW TFTs. After NH_3 treatment, the GAA NW TFTs exhibited superior performance. The GAA NW TFTs that had been subjected to NH_3 plasma treatment exhibited improved device characteristics, including a lower value of V_{th} (0.18 V), a steeper SS (184 mV/dec), a very high On/Off current ratio (1.64×10^8), and a small DIBL (58 mV/V).

onto a 200-nm-thick bottom oxide (BOX) at 550 °C using low-pressure chemical vapor deposition (LPCVD). In sequence, solid phase crystallization (SPC) was performed at 600 °C for 24 h in a nitrogen ambient to turn the α-Si into a polycrystalline Si structure. The key parameter of the spacer patterning technique was the thickness of followed deposition of the tetraethylorthosilicate (TEOS) oxide and nitride spacer. The TEOS oxide thickness defined the height of the nitride spacer. After definition of the TEOS pattern by reactive ion etching (RIE), the nitride was deposited and then etched using RIE. The thickness of the nitride film corresponded to the width of the spacer. In the study, the thicknesses of the TEOS and nitride layers were chose to be 70 and 60 nm, respectively, for these processing conditions. Using the nitride spacer as a hard mask, 1-μm-long multiple channels of poly-Si NW having a channel width (W_{ch}) of 44 nm were formed. By varying the thicknesses of the TEOS and nitride layers, nanoscale structures were readily defined without the need for advanced lithography techniques. After wet etching in diluted HF solution (1:100) to remove the 70–80 nm BOX layer, the poly-Si NW was released from the BOX substrate. Next, the sequential conformal deposition (LPCVD) of dielectric of ONO stacks (TEOS/nitride/TEOS = 10.5 nm/5.5 nm/15.3 nm) and 200-nm-thick *in situ* N^+ poly-Si was performed to surround the channels. After gate pattern transformation, the etching of dielectric on source and drain surface was performed. The self-aligned phosphorus ion implantation was then completed at a dose of

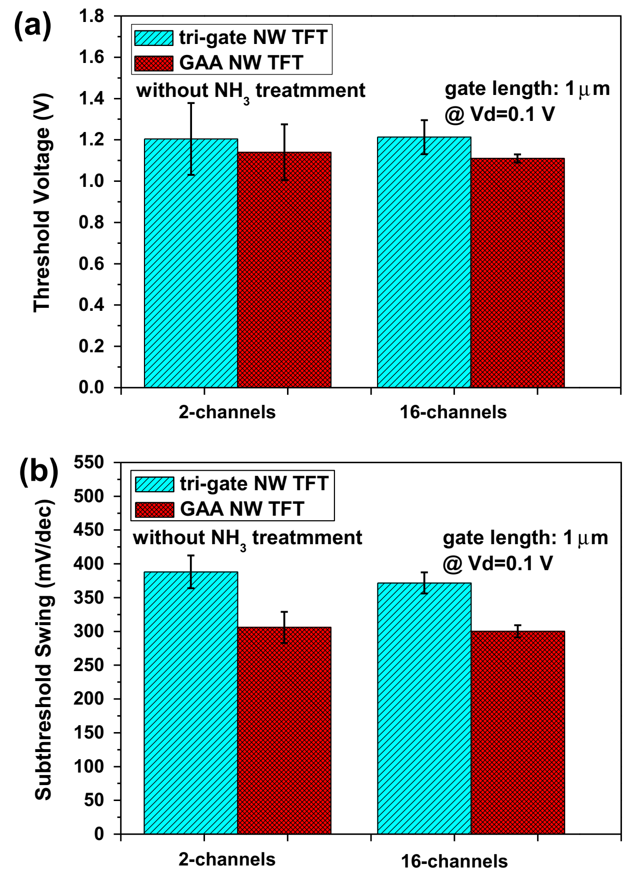

Fig. 3. Mean values and standard deviations of the (a) threshold voltage and the (b) subthreshold swing of GAA and tri-gate NW TFTs featuring 2 and 16 channels.

5×10^{15} cm^{-2} for the formation of ohmic contact. TEOS passivation, thermal annealing (600 °C, 6 h), standard metal contact formation, and sintering processes were performed to provide the final structure. To study the impact of the grain boundary defects, the samples were subjected to NH_3 plasma treatment in a parallel-plate plasma reactor at a power density of 0.7 W/cm^2 at 300 °C for 1 h.

3. Results and discussion

Fig. 1 presents transmission electron microscopy (TEM) images of NW channels possessing a GAA structure and a tri-gate structure surrounded by ONO layers. These devices had a nominal channel

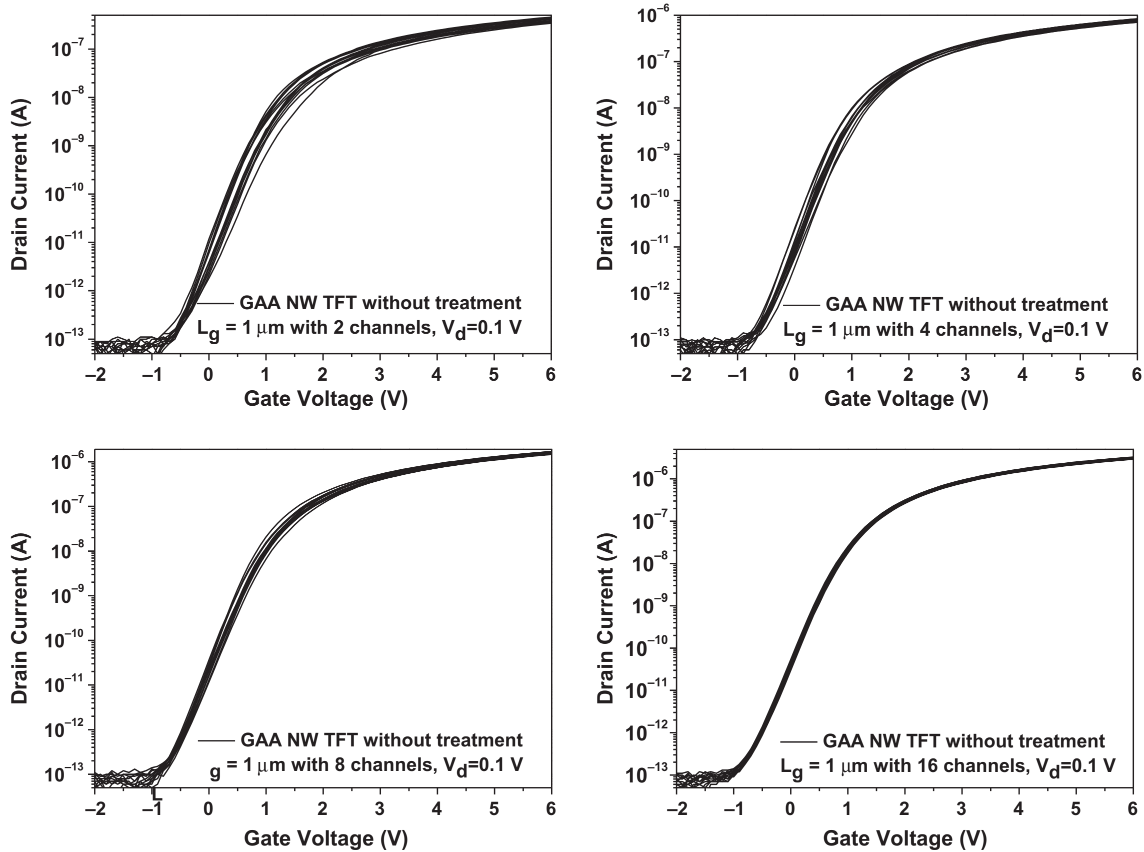

Fig. 4. Transfer characteristics of GAA NW TFTs for channel number of (a) 2, (b) 4, (c) 8, and (d) 16. The uniformity of electrical characteristics has been effectively improved with increasing of channel number.

length (L) of 1 μm, a channel width (W_{ch}) of 44 nm, and a channel thickness (T_{ch}) of 62 nm. The ONO stack (O/N/O = 10.5 nm/5.5 nm/15.3 nm) was conformably deposited around the channel. The total geometry channel width estimated by $[2 \times (W_{ch} + T_{ch})]$ was ca. 212 nm for one channel GAA device. Such a stack layer can improve the future integrating memory function when using a system-on-panel (SOP) approach [14]. To prevent the effects of non-uniformity of our fabricated NWs, especially during the film deposition and etching processes, the devices under investigation were selected from the same vicinity of the chip.

Fig. 2 presents the transfer curves of the GAA and tri-gate NW TFTs. Relative to the tri-gate device, the GAA NW TFTs, even when it had not been subjected to the treatment process, suppressed the short channel effects (SCEs), providing a smaller drain induce barrier lowering (DIBL), a lower leakage current, and a steeper SS. Because the GAA devices provided additional electric field strength at the corner and bottom regions, leading to improvements in the values of the drain current and V_{th} [the gate voltage required to yield a normalized drain current of I_d ($W = L$) = 10 nA at V_d = 0.1 V]. These improvements were also as a result of the channel potential being tightly controlled by the surrounding electric field. Moreover, the large number of trap states in the poly-Si channel region also played a critical role influencing the device performance and the SCEs. As a result, the poly-Si TFT exhibited a large leakage current due to the large field emission current near the drain side and grain boundary trap states in the channel [15]. Thus, after treatment process the N and H atoms passivated the traps on the channel surface and/or in the channel area [7]. The passivation species diffused mainly through the gate oxide into the channel from the channel edge. These passivation radicals were also further reducing the grain boundary potential barrier, hence, off-state leakage current was minimized and on-state current was enhanced. As a result, the proposed device exhibited a higher On/Off current ratio (>10^8) than that of the untreated samples (>10^7). Therefore, the GAA NW TFTs that had been subjected to NH_3 plasma treatment exhibited improved device characteristics, including a lower value of V_{th} (0.18 V), a steeper SS (184 mV/dec), a very high On/Off current ratio (1.64×10^8), and a small DIBL (58 mV/V).

Fig. 3(a) displays the mean values and the standard deviations of V_{th} for the different gate configurations possessing different numbers of channels. For the GAA NW TFTs possessing 2 and 16 channels, the mean values of V_{th} were 1.14 and 1.11 V, respectively; for the corresponding tri-gate devices, these values were 1.20 and 1.21 V, respectively. Notably, because the electric field surrounded the entire channel, the GAA NW TFTs exhibited a smaller mean value of V_{th} relative to that of its tri-gate counterpart. In addition, the GAA NW TFTs exhibited a smaller standard deviation of its value of V_{th}; such relative stability is critical for larger-glass active-matrix liquid crystal displays (AMLCD) applications. Furthermore, the grain boundaries of the SPC poly-Si were randomly distributed in the channel region, resulting in variation of its electrical characteristics. These grain boundaries trap charges and build up potential barriers to the flowing carriers, resulting in additional scattering that leads to device degradation [15]. After SPC, the grain size in the channel region was approximately 25–40 nm in our experiment; relative to the NW channel having a value of W_{ch} of 44 nm, we expected the device to suffer from fluctuating electrical characteristics mainly due to these random distribution grain boundaries [12]. Our results reveal that the gate structure and the number of channels both influence the device characteristics. The standard deviations of the electrical characteristics of both the tri-gate and GAA NW TFTs were reduced

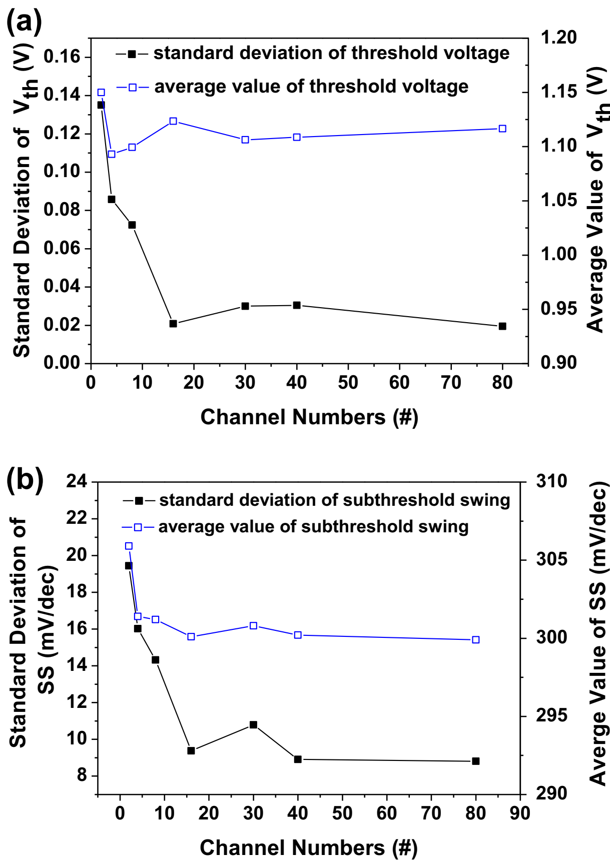

Fig. 5. The electrical fluctuation has been minimized after devices featuring 16 channels. (a) The mean and standard deviation of the threshold voltage and (b) the mean value and standard deviation of subthreshold swing. The statistics were obtained from measurements of 15 GAA NW TFTs from three different chips, at V_d = 0.1 V.

effectively upon increasing the number of channels. The standard deviation of the value of V_{th} of the tri-gate TFTs decreased from 174 to 82 mV; that of the GAA NW TFTs decreased from 135 to 21 mV. Interestingly, the improvement of variation was greater when increasing the number of channels from 2 to 16 than it was when changing the gate configuration from a tri-gate to a surrounding gate. Fig. 3(b) reveals similar results for the SS. The GAA NW TFTs with 16 channels had a smallest average value (300 mV/dec) and standard deviation (9.38 mV/dec) of SS among all of the TFTs. Thus, the GAA structure improved the mean values of V_{th} and SS, and increasing the number of channels can effectively minimize the electrical variations. Fig. 4 displays the transfer characteristics of devices with channel number of 2, 4, 8, and 16. The transfer characteristics were resulted from measurements of 15 devices. Device-to-device variation was minimized with increasing of channel number. Fig. 5 shows the standard deviation of threshold voltage and SS has been minimized of devices with different channel number. Device with 16 channels reaches a local minimum in both standard deviation of threshold voltage and SS (about 21 mV and 9.38 mV/dec, respectively). Fig. 5(a) also shows that the average threshold voltage is around 1.1 V, and extending total geometry channel width by increasing the channel numbers did not affect the mobility for the constant current extraction method of V_{th}. Fig. 5(b) exhibits the similar result of the SS, the average value is maintained at 300 mV/dec as channel number increased. However, the variation is reduced by increasing channel number and reaches a minimum value after utilizing 16 channels in our proposed device. Many crystallization technologies have been demonstrated to enlarge grain size and to effectively reduce the impact of grain boundary in the channel for device performance improvement [4,5]. However, it inherently brings the statistical variation induced by grain boundary [16]. In this study, multiple channel design provides a promising alternative to further improve the uniformity of electrical characteristics. Moreover, increasing the number of channels not only decreased the variation of the electrical properties but also improved the On/Off current ratio (as shown in Fig. 4). Presumably due to the increase the number of channels extending total geometry channel width and providing mores corners leading more driving current. And, the off-state leakage current remained tightly controlled by the surrounding electric field. Fig. 6 shows the normalized transconductance of the proposed GAA TFT with multiple NW channels. The transconductance shows almost similar performance after normalized with total geometry channel width for devices with different channel numbers. With GAA multiple-channel structure, the device exhibited improvement in driving current and minimized fluctuations.

Fig. 7 displays the transfer characteristics of GAA NW TFTs prepared with and without NH_3 plasma treatment. The curves in Fig. 7 are the collected from different chips of a same batch. Five devices were characterized from each chip. The multiple-channel structure results in higher treatment efficiency relative to that of a traditional planar device [7]. As results shown in Fig. 2, we observe that the threshold voltage and SS are all improved after NH_3 plasma treatment which reduced the trap states in the channel region. Moreover, the plasma passivation treatment also effectively reduces the electrical fluctuation. The 2-channel devices exhibited further minimization in standard deviation in their values of V_{th} (106 mV) and SS (15.88 mV/dec) compare to untreated device (V_{th} is 135 mV and SS is 19.44 mV/dec) as shown in Fig. 7(a). Fig. 7(b) shows that the treated 16-channel GAA NW TFTs exhibits a very small value of standard deviation in its value of V_{th} and SS (30 mV and 11.4 mV/dec, respectively). In spite that NH_3 plasma treated 16-channel devices present a slightly deterioration in electrical uniformity compare to untreated ones, however, the device performance still shows obviously improvement. Fig. 8 presents the typical output characteristics of the GAA devices with and without NH_3 plasma treatment process. The inset to Fig. 8 compares the performances of the GAA and tri-gate devices that had been prepared without NH_3 plasma treatment. The additional electric field of the GAA structure increased the vertical electric field such that it became more prominent than that of the horizontal component [17]. Consequently, the GAA NW TFTs exhibited

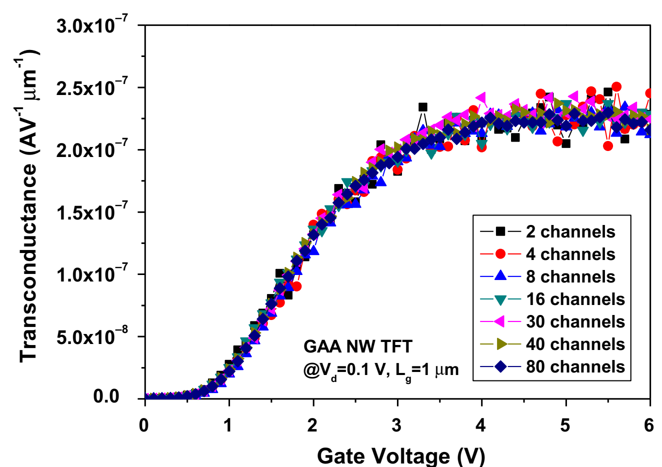

Fig. 6. Normalized transconductance of GAA NW TFTs featuring different channel numbers with a gate length of 1 μm. The current driving capability was not degraded as the channel number increases.

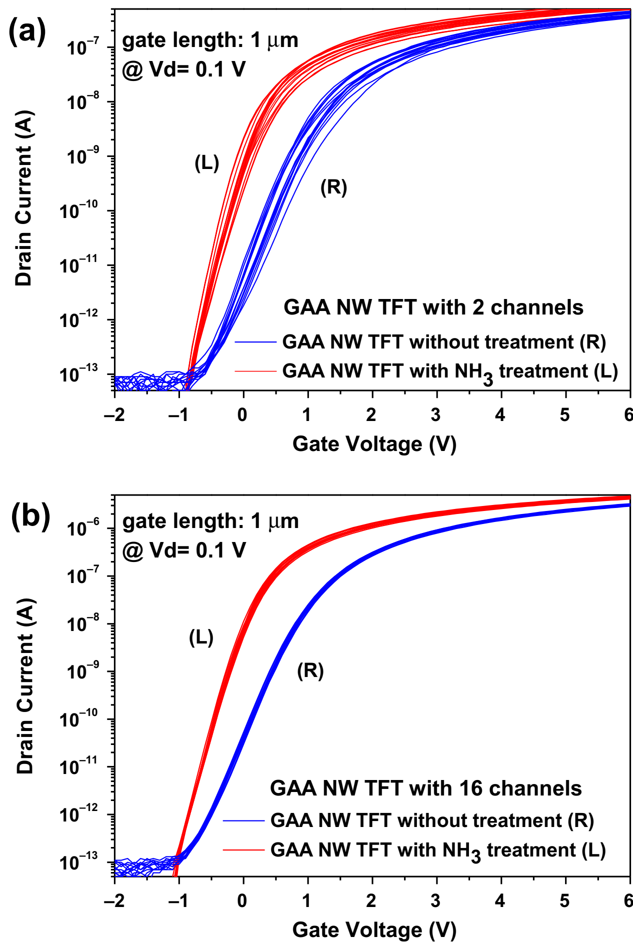

Fig. 7. Transfer characteristics of GAA NW TFTs with (a) 2 and (b) 16 channels, with and without NH_3 plasma treatment. *I–V* curves were resulted from measurements of 15 devices from three chips.

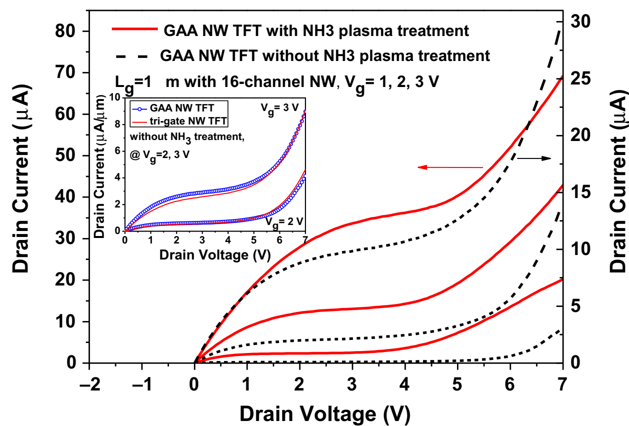

Fig. 8. Typical output characteristics of 16-channel GAA NW TFTs with and without treatment process featuring a gate length of 1 μm. The kink point was improved from 3.6 to 4.2 V at $V_g = 3$ V. The inset compares the performances of the GAA and tri-gate devices that had been prepared without NH_3 plasma treatment.

suppression of the kink effect. The kink point of GAA device was improved from 3.5 to 3.9 V (at $V_g = 2$ V) comparing to that of tri-gate device. After NH_3 plasma treatment, which reduced the trap density of states, the passivated GAA NW TFTs displayed further improvements in both the performance of its output characteristics and the kink effect. The kink point was improved from 3.6 to 4.2 V (at $V_g = 3$ V) which is also related to the density of traps in active region and high electric field at the drain junction.

4. Conclusion

We have characterized GAA NW TFTs featuring multiple channels to minimize the variation of its electrical characteristics. The gate structure and the number of channels both improved the device performance relative to that of tri-gate TFTs. Although the different gate configurations affected both the mean values and standard deviations of the performance metrics, increasing the number of channels decreased the grain boundary variation, effectively minimizing the electrical variations. To further improve the variations in device performance, devices were subjected to NH_3 plasma treatment to reduce the trap density of states in the grain boundary. The proposed device of GAA NW TFTs with 16 channels combine with plasma treatment exhibited a low threshold voltage (0.18 V), a steep SS (184 mV/dec), a high On/Off current ratio (1.64×10^8), a small DIBL (58 mV/V), and displayed the minimized standard deviation of V_{th} (30 mV) and SS (11.4 mV). The kink effect was also suppressed. We suspect that such GAA multiple-channel TFTs would be suitable devices for applications in low-voltage circuit operations.

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