A 2.4 GHz Reference-Less Receiver for 1 Mbps QPSK Demodulation

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***Abstract*—A 2.4 GHz reference-less single chip wireless receiver for 1 Mbps QPSK demodulation is presented. The receiver accomplishes LO carrier recovery and data demodulation directly from the RF received signal without resort to resonator based reference, such as crystal oscillator. Integrating LNA, mixer, LO carrier recovery loop, postamplifier, and digital demodulator on a single chip, the total power consumption is 20.4 mW. The measured phase noise from a recovered carrier at 2.432 GHz is about −111 dBc/Hz at 1 MHz offset. The chip size is 1.75×1.55 mm^2.**

***Index Terms*—Body area network (BAN), carrier recovery, demodulator, QPSK, reference-less, wireless receiver.**

I. Introduction

WIRELESS sensor networks (WSN) and bio-inspired electronics have drawn tremendous research efforts [1]–[9] recently. For sensor node integrated circuits design, small form factor, low power, and system cost are of special interests to promote pervasive and ubiquitous adaptations. Conventionally, RF receiver front-end includes a LO (local oscillator) generator that utilizes crystal or other resonator based reference for carrier frequency synthesis. The crystal oscillator itself in general dissipates extra power and is too bulky for single chip integration. Meanwhile, due to unavoidable crystal frequency mismatches between the transmitter and receiver side, a carrier recovery loop is required at the digital base band to compensate frequency offset for data demodulation.

Recently, several techniques were proposed to generate on chip reference frequency in integrated circuit technologies to replace crystal [10]–[16]. Most of their accuracy falls in the range of a few percent while consuming milliwatt power. For the frequency accuracy to be closer to that of a temperature-compensated crystal oscillator (TCXO), it may require additional costly trimming process [10].

This paper proposes a low cost, small form factor, single chip reference-less wireless receiver which recovers the LO frequency directly from the received RF signal [17]. Based on the concept of wireless remote frequency synchronization to the transmitter side, it eliminates extra reference generator at the receiver side, and also facilitates wireless clock distribution. Since the LO carrier at the receiver side is tracking the frequency at the transmitter side directly during data receiving, the issue of carrier frequency offset between the transmitter and receiver in conventional wireless transceivers is eliminated. Meanwhile, it

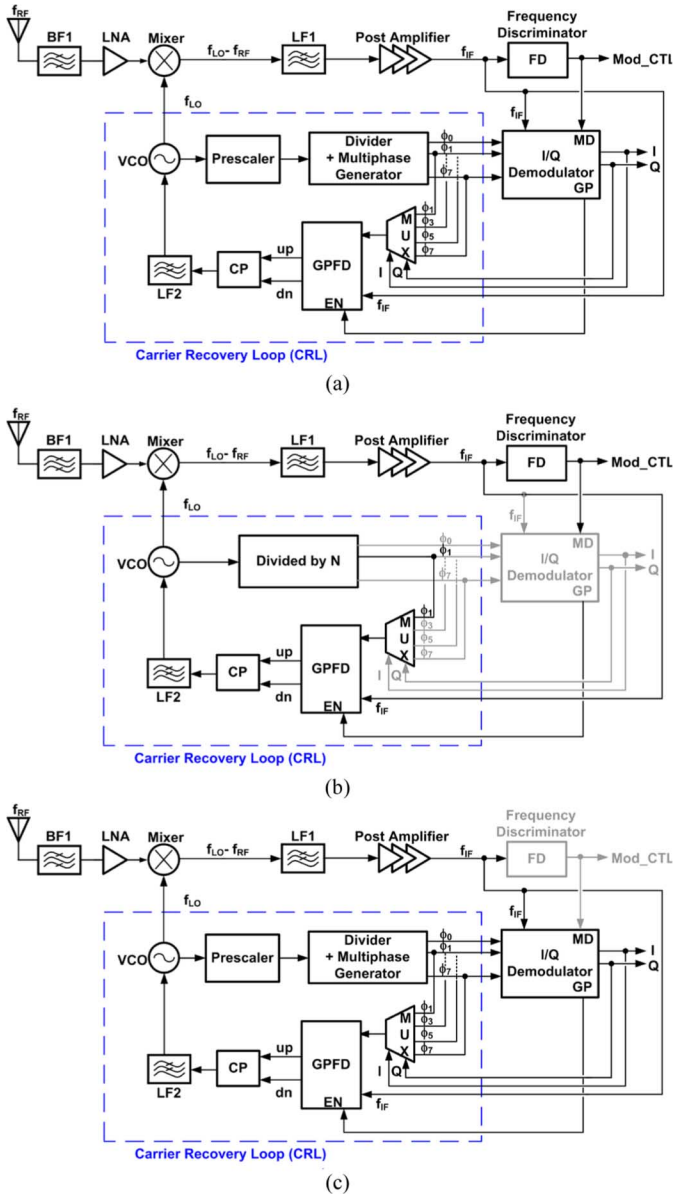

Fig. 1. (a) Proposed receiver architecture. (b) Frequency acquisition mode. (c) Phase tracking and data demodulation mode.

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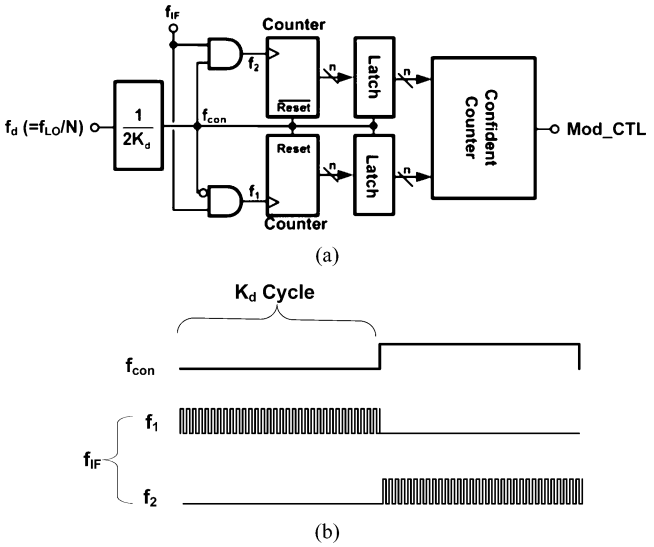

Fig. 2. (a) Frequency discriminator. (b) Timing diagram of edge counter.

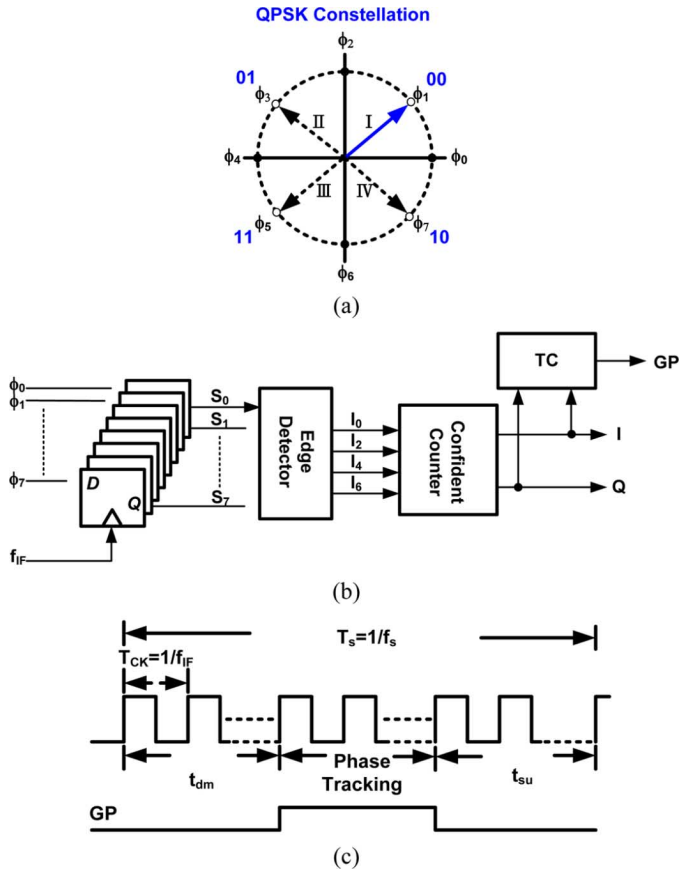

Fig. 3. (a) QPSK signal constellation. (b) Demodulator. (c) Timing diagram.

accomplishes data demodulation along with carrier and timing recovery without resort to an extra baseband ADC.

This paper is organized as follows. Section II describes the proposed receiver architecture and operation principle. The system behavior and stability is discussed in Section III. Section IV introduces the detailed circuit schematic of each block. Experimental results are shown in Section V, and Section VI concludes this paper.

II. Architecture

To demonstrate the proposed concept, an experimental prototype for QPSK wireless receiver at 2.4 GHz is implemented. Fig. 1(a) shows the receiver architecture. It integrates LNA, mixer, channel selection filter, postamplifier, data demodulator, frequency discriminator, and LO carrier recovery loop (CRL) on a single chip. As a single channel experimental prototype, the interference is rejected by both external band selection filter and on chip channel selection filter. The LNA and mixer respectively provide 16.6 dB and 6.7 dB gain. The postamplifier incorporating channel selection filter are composed of six stages, which enlarge the output to digital swing.

The CRL composes of a VCO, prescaler, divider and multiphase generator, phase selector (MUX), and a gating phase frequency detector (GPFD). Incorporating with the data demodulator, it recovers carrier frequency and clock from the QPSK modulation signal for frequency down conversion and data demodulation.

A. Frequency Acquisition

Let the cascade divide ratio of the prescaler and feedback divider be N, $f_{\rm LO}$ denotes the VCO frequency, and $f_{\rm IF}$ represents the IF frequency. At the onset for data receiving, a constant phase preamble $(f_{\rm RF})$ from the transmitter is received, and the voltage controlled oscillator (VCO) is preset to its highest frequency which is larger than $f_{\rm RF}$. The CRL is operated in the frequency acquisition mode, as illustrated in Fig. 1(b). Meanwhile, the phase selector (MUX) passes a fixed divider output phase (one of $\phi_0, \ldots, \phi_7$) to the GPFD. The down converted signal $f_{\rm IF}$, where $f_{\rm IF} = f_{\rm LO} - f_{\rm RF}$, is then compared to $f_{\rm LO}/N$ by the GPFD. If $f_{\rm LO} - f_{\rm RF} > f_{\rm LO}/N$, $f_{\rm LO}$ decreases so that $f_{\rm IF}$ is reduced more than $f_{\rm LO}/N$ for $N > 1$. Contrarily, if $f_{\rm LO}/N > f_{\rm LO} - f_{\rm RF}$, $f_{\rm LO}$ increases so that $f_{\rm IF}$ is increased more than $f_{\rm LO}/N$. By the negative feedback mechanism, when the loop is settled

$$f_{\rm IF} = f_{\rm LO} - f_{\rm RF} = \frac{f_{\rm LO}}{N} \tag{1}$$

Thus, the local frequency is determined by N and the RF input frequency, where

$$f_{\rm LO} = \frac{N}{N-1} f_{\rm RF}. \tag{2}$$

The frequency locking detector is realized by a frequency discriminator. Fig. 2 illustrates detailed circuit schematic, which is based on the concept of edge counting [18]. As is described in (1), when the loop approaches locked, the IF frequency $(f_{\rm IF})$ would be equal to the divider output $(f_d = f_{\rm LO}/N)$ In order to improve the resolution for frequency detection, f_d is scaled down by $2K_d$ to generate a control signal $f_{\rm con}$. The high and low level of $f_{\rm con}$ alternatively performs as gating pulse of $f_{\rm IF}$, whose counting edges are stored in two latches. In this design, if the contents of latches fall within $(\mathrm{K_d}\pm 2)$, the confident counter will be toggled. When the contents in latches hit the target consecutively, implying that $f_{\rm LO}$ approaches locked state, and the status of frequency locked is then resolved by the confident counter.

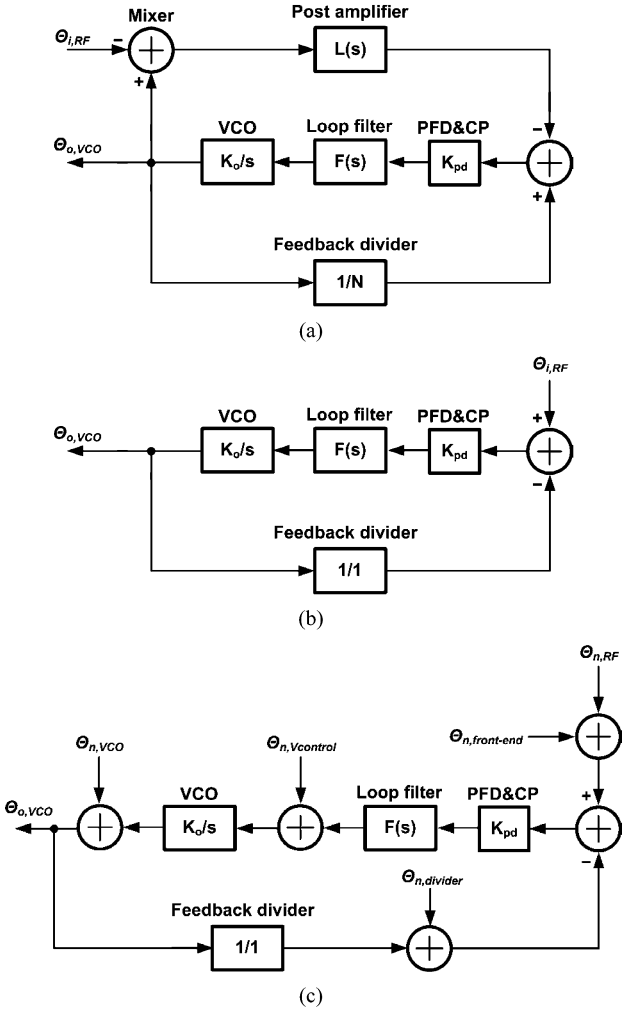

Fig. 4. (a) Receiver behavior model. (b) Equivalent model. (c) Noise model.

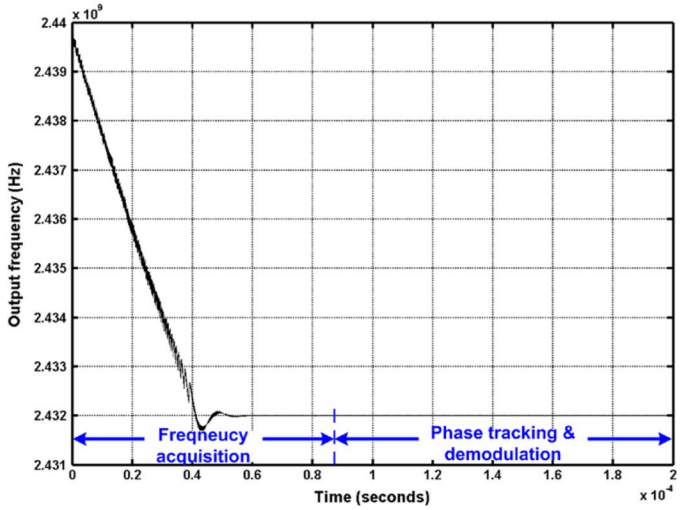

Fig. 5. The simulated settling behavior.

TABLE I
DESIGNED PARAMETERS

System parameters	**N**	152
	K	f_{IF}/f_s=16
	K_d	128
	GDC	0.25
CRL parameters	**VCO frequency**	2.2 – 2.6 GHz
	VCO gain (K_o)	100 MHz/V
	Charge pump current (I_{cp})	60 μA
	Loop bandwidth	500 KHz
	Phase margin	65°

To successfully demodulate M-ary phase modulation signal, the IF signal should fall into one of the M phase zones during data demodulation. It means that the frequency difference between $f_{\rm IF}$ and f_d should be within a locking window before the CRL steps into phase demodulation. For an M-ary PSK modulation signal, let f_s be the symbol rate, it can be shown that the lower bound of K_d can be derived as

$$K_d \geq 2M \times \frac{f_{\rm IF}}{f_s}. \tag{3}$$

B. Phase Tracking and Data Demodulation

When the loop approaches locked, the receiver will acknowledge transmitter for data receiving. The mode control signal (Mod_CTL) will then switch the CRL to phase tracking mode, as illustrated in Fig. 1(c). Afterwards, the CRL will keep track the carrier frequency as well as demodulate the QPSK signal simultaneously.

Fig. 3 illustrates the scheme for QPSK demodulator and timing diagram for the gating PFD. At the postamplifier output, $f_{\rm IF}$ switches its phase among (0°, 90°, 180°, and 270°) periodically at symbol rate (f_s), as is shown in Fig. 3(a). For QPSK demodulation, the divider output f_d $(f_d = f_{LO}/N)$ generates 8 phases $(\phi_0, \ldots, \phi_7)$ to capture $f_{\rm IF}$. Here $(\phi_0, \phi_2, \phi_4, \phi_6$ divides the signal constellation into four zones, and the IF signal is directly demodulated by detecting the operating zones (I, II, III, IV) that $f_{\rm IF}$ falls into. This is accomplished by sampling $(\phi_0, \ldots, \phi_7)$ using $f_{\rm IF}$ followed by edge detector and decoder. The I/Q digital output is then demodulated after confident counter, as shown in Fig. 3(b)

In each phase zone, the targeted phase for frequency tracking and phase synchronization is $(\phi_1, \phi_3, \phi_5, \phi_7)$ respectively. The demodulator then switches its corresponding targeted phase according to the demodulated I/Q data through the MUX to the GPFD. Thus, the CRL can continuously track the RF signal to maintain the stability of VCO output frequency during data receiving. To avoid mis-disturbing the carrier frequency during phase switching in QPSK signaling, a timing controller in the demodulator will generate gating pulse (GP) to enable the GPFD, as also shown in Fig. 3(c). In each symbol time $(T_s = 1/f_s)$, let the clock cycles $(T_{ck} = 1/f_{\rm IF})$ for data demodulation (zone detection) be t_{dm}, the setup time for next data period phase transition be t_{su}, and the ratio between IF frequency $(f_{\rm IF})$ and symbol rate (f_s) be K, i.e.,

$$K = \frac{f_{\rm IF}}{f_s}. \tag{4}$$

During these intervals $(t_{dm} + t_{su})$, the GPFD is disabled by GP. The active period (GDC) for the GPFD becomes

$$\text{GDC} = \frac{K - t_{dm}/T_{ck} - t_{su}/T_{ck}}{K}. \tag{5}$$

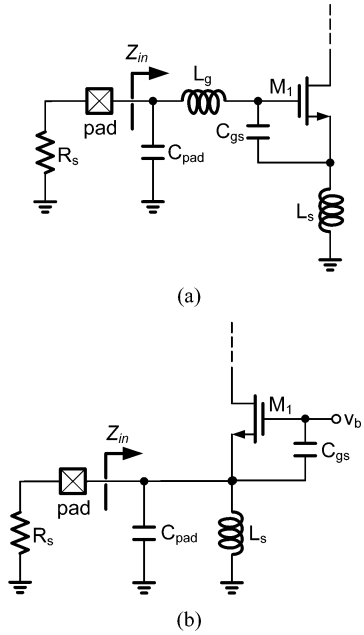

Fig. 6. Low-noise amplifier based on: (a) common-source and (b) common-gate topology.

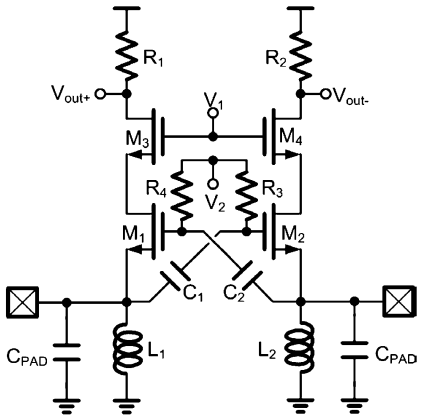

Fig. 7. Differential gm-boosted CGLNA.

The loop bandwidth for the CRL during phase tracking and data demodulation mode is designed by taking GDC into account. On the other hand, the tracking bandwidth against noise disturbance for data demodulation reflects in t_{dm}. Both suggest that a higher K improves its robustness for demodulation and carrier tracking performance, but also demands a wider bandwidth of IF amplifier and demodulator.

III. Behavior Model

The stability of the wireless carrier recovery loop is investigated using a PLL-like linear model. Fig. 4(a) shows the system block diagram. Let the gain of PFD and charge pump be K_{pd}, VCO gain be K_o, and the transfer function of loop filter and postamplifier be $F(s)$ and $L(s)$ respectively.

The phase transfer function from the received RF signal $\theta_{i,\mathrm{RF}}$ to the VCO output $\theta_{o,\mathrm{VCO}}$ can be derived as

$$\frac{\theta_{o,\mathrm{VCO}}}{\theta_{i,\mathrm{RF}}} = \frac{-L(s)G(s)}{-1 - G(s)(L(s) - 1/N)} \tag{6}$$

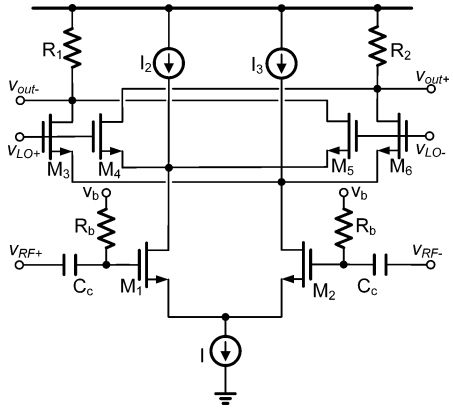

Fig. 8. Frequency down-converted mixer.

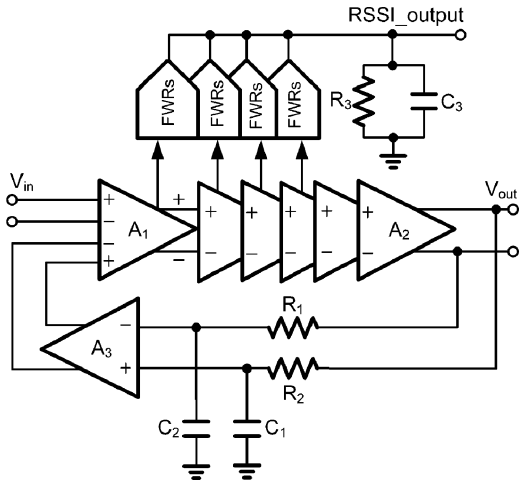

Fig. 9. Postamplifier architecture.

where $G(s) = K_{pd}K_oF(s)/s$. In this design, the bandwidth of postamplifier is much higher than the IF frequency such that the phase shift caused by $L(s)$ is negligible. Thus, the system transfer function can be simplified as

$$\frac{\theta_{o,\mathrm{VCO}}}{\theta_{i,\mathrm{RF}}} = \frac{G(s)}{1 + G(s)(1 - 1/N).} \tag{7}$$

If $N \gg 1$ ($\mathrm{N} = 152$ in this case), the system transfer function can be approximated as

$$\frac{\theta_{o,\mathrm{VCO}}}{\theta_{i,\mathrm{RF}}} \approx \frac{G(s)}{1 + G(s)} \tag{8}$$

Thus, the signal transfer function is the same as that of a typical PLL with feedback factor equal to 1, as is shown in Fig. 4(b). The loop gain $G(s)$ can be designed to maintain its stability accordingly. Fig. 4(c) illustrates the noise model of the receiver front end, where $\theta_{n,\mathrm{front-end}}$ denotes the excess noise caused by the receiver front-end, and NF is the corresponding noise figure. We have

$$\begin{aligned}\theta_{o,\mathrm{VCO}} &\approx \frac{G(s)}{1 + G(s)}\theta_{n,\mathrm{RF}} + \frac{G(s)}{1 + G(s)}\theta_{n,\mathrm{front-end}} \\ &= \frac{G(s)}{1 + G(s)}\theta_{n,\mathrm{RF}} \times \left(1 + \frac{\theta_{n,\mathrm{front-end}}}{\theta_{n,\mathrm{RF}}}\right) \\ &= \frac{G(s)}{1 + G(s)}\theta_{n,\mathrm{RF}} \times \mathrm{NF}.\end{aligned} \tag{9}$$

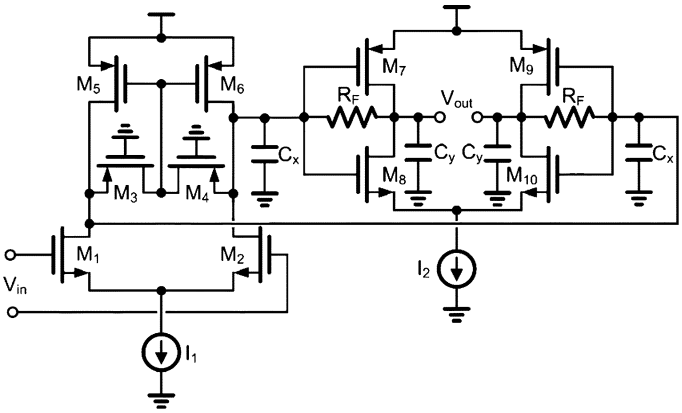

Fig. 10. Gain cell of postamplifier.

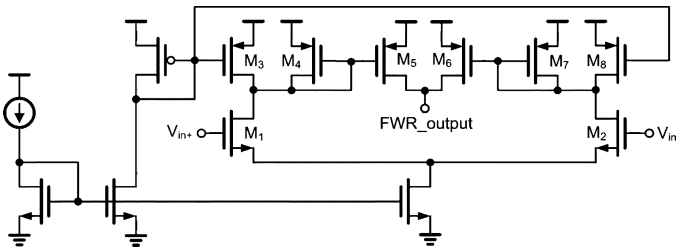

Fig. 11. Full wave rectifier for RSSI.

Thus, the VCO phase noise will be elevated by the noise figure of the receiver front-end after phase locked. The designed parameters are summarized in Table I, and the simulated settling behavior is shown in Fig. 5.

The GPFD is compared at IF frequency $(K\omega_{\rm s})$ and is periodically enabled and disabled by the gating pulses (GP) for an active period of GDC, which is generated from the I/Q demodulator at a symbol rate $(\omega_{\rm s})$. Assuming that the voltage ripple caused by the nonidealities of PFD, charge pump and periodically gating is represented as

$$V_{\rm ripple}(t) = V_{\rm GP}(t) \times V_m \sin(K\omega_s t) \tag{10}$$

where V_m presents the ripple amplitude and $V_{\rm GP}(t)$ is the gating pulse. If the VCO gain is represented as $K_{\rm VCO}$, and its output frequency is ω_0, the VCO output can be represented as

$$\begin{aligned} V_{\rm VCO}(t) &= V_0 \cos\left(\omega_0 t + K_{\rm VCO}\int V_{\rm ripple}(t)\,dt\right) \\ &\approx V_0 \cos\omega_0 t - \sum_{n=1}^{\infty} X[n][\cos(\omega_0 - n\omega_s)t \\ &\quad - \cos(\omega_0 + n\omega_s)t] \\ X[n] &= \frac{K_{\rm VCO}V_0V_m}{2K\omega_s}\left[\frac{\sin(\pi(n-K)\times {\rm GDC})}{\pi(n-K)}\right. \\ &\quad \left. + \frac{\sin(\pi(n+K)\times {\rm GDC})}{\pi(n+K)}\right] \end{aligned} \tag{11}$$

where GDC should be greater than zero to maintain the close loop system. Equation (11) reveals that the reference spurs will spread at multiples of ω_s at double side of the center frequency. On the other hand, the higher data rate results in a lower reference spurs. The maximum spurs will occur at $n = K$ $(\omega_{\rm spurs} = \omega_0 \pm K\omega_s)$ which dominates the SFDR of output spectrum. Therefore, the SFDR can be approximated as

$$\begin{aligned} {\rm SFDR} &= 20\log\left(\frac{2K\omega_s}{{\rm GDC}\times K_{\rm VCO}V_m}\right) \\ &= 20\log\left(\frac{2\omega_{\rm IF}}{{\rm GDC}\times K_{\rm VCO}V_m}\right). \end{aligned} \tag{12}$$

It can be seen that the SFDR is improved by a factor of $20\log({\rm GDC})$ since the GPFD only activates for a short period. The SFDR will be the same as that of a conventional PLL if GDC equals to 1. In this design, $\omega_{\rm s}$ is the 1 MHz symbol rate, ω_m $(\omega_{\rm IF})$ is the 16 MHz IF signal, and GDC is around 0.25.

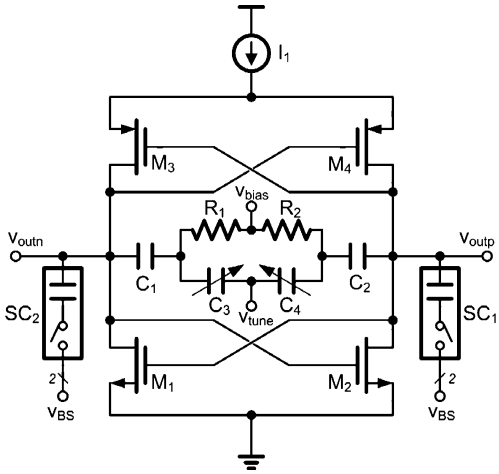

Fig. 12. The circuit schematic of VCO.

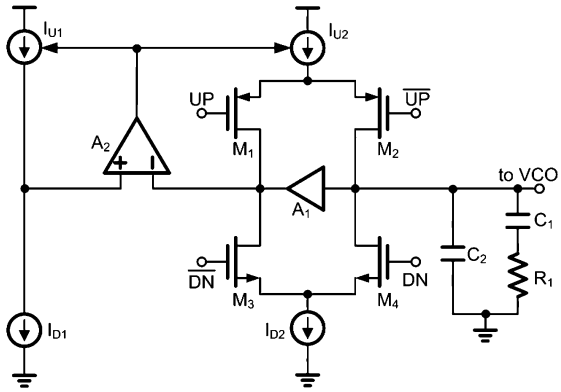

Fig. 13. The circuit schematic of charge pump and loop filter.

IV. Building Blocks

A. Low Noise Amplifier

Conventionally, low noise amplifiers in RF receiver are based on common-source [19] or common-gate [20] architectures, as are shown in Fig. 6. A common-source LNA (CSLNA) in general has better noise performance compared to its common-gate counterpart (CGLNA). However, it requires two on-chip inductors for narrow band input matching [21]. Contrarily, CGLNA only needs a single inductor for input matching, as shown in

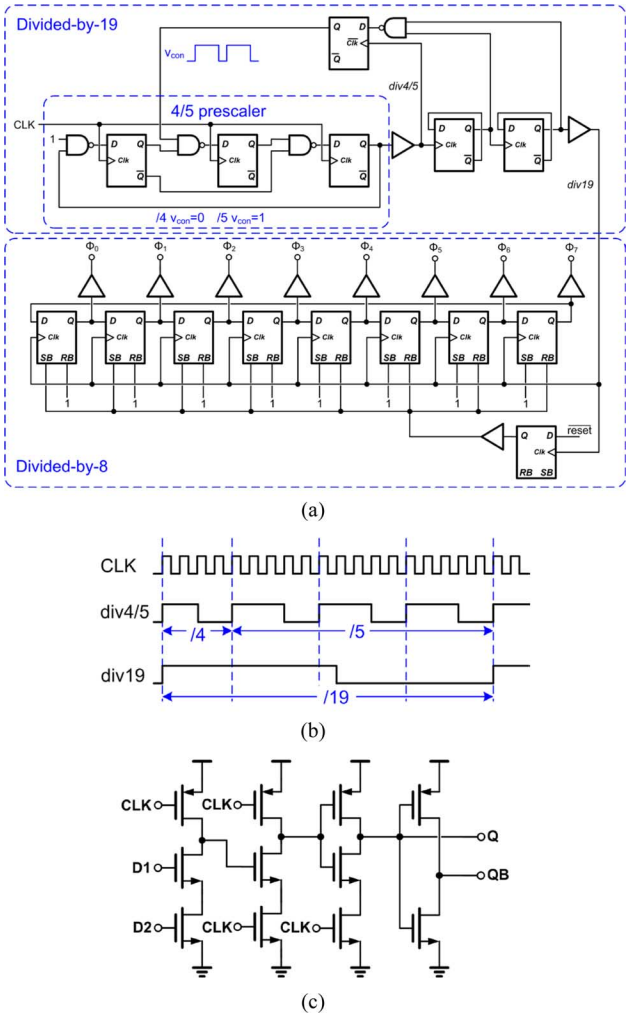

Fig. 14. The architecture of: (a) feedback divider, (b) timing diagram of divided-by-19 divider, and (c) NAND gate embedded TSPC filp-flop.

Fig. 6(b). It can provide broadband matching depending on the quality factor of the resonator ($\mathrm{L_s}, \mathrm{C_{pad}} + \mathrm{C_{gs}}$).

The noise figure of a common gate LNA can be derived as

$$F_{\mathrm{CGLNA}} = 1 + \frac{\overline{i_{nd}^2}\left(\frac{1}{1+g_m R_s}\right)^2}{\overline{i_{ns}^2}\left(\frac{g_m R_s}{1+g_m R_s}\right)^2} = 1 + \frac{\gamma g_{d0}}{g_m^2 R_s} = 1 + \frac{\gamma}{\alpha}\Big|_{g_m R_s = 1} \tag{13}$$

where α and γ are bias-dependent parameters. To further improve its noise performance, differential gm-boosted CGLNA topology is adopted in this design [20]–[22]. Fig. 7 shows the detailed circuit schematic. Its noise figure can be derived as

$$\begin{aligned} F_{\mathrm{CGLNA,gm-boosted}} &= 1 + \frac{\gamma}{\alpha}\frac{1}{(1+A)} \\ &= 1 + \frac{\gamma}{\alpha}\frac{1}{\left(1+\frac{C_C}{(C_C+C_{gs})}\right)} \\ &= 1 + \frac{\gamma}{\alpha}\left(\frac{C_{gs}+C_C}{C_{gs}+2C_C}\right) \end{aligned} \tag{14}$$

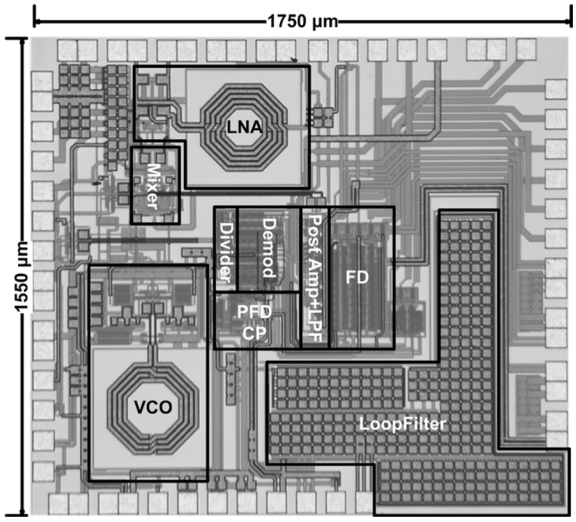

Fig. 15. Chip microphotograph.

where A $\sim$ 1 by differential excitation. By choosing $C_C \gg C_{gs}$, the noise figure can be derived as

$$F_{\mathrm{CGLNA,gm-boosted}} = 1 + \frac{\gamma}{2\alpha}\Big|_{g_m R_s = 1/2}. \tag{15}$$

(15) shows that the noise figure performance can be improved compared to (13) thanks to differential $\mathrm{g_m}$ boosted technique. On the other hand, its power consumption for input matching can be reduced.

B. Frequency Down-Converted Mixer

A double-balanced Gilbert mixer with active load is adopted for frequency down conversion. Fig. 8 shows the circuit schematic. In a typical Gilbert mixer, the low frequency and high frequency noise contribution can be derived as [23]

$$i_{o,\mathrm{low\_frequency\_noise}} = 4I\frac{V_n}{S \times D} \tag{16}$$

$$\overline{i_{o,\mathrm{high\_frequency\_noise}}} = 4kT\gamma\frac{I}{\pi A} \tag{17}$$

where A and S respectively shows the amplitude and slope of the LO signal, I is the dc current, D is the LO period, V_n denotes low frequency input-referred noise of LO, k is Boltzman's constant, T is absolute temperature and γ is the channel noise factor. (16) and (17) reveal that both the high and low frequency noise contributed by switching pairs are proportional to I. Let V_{ov} represents the overdrive voltage of $\mathrm{M_1}$ and $\mathrm{M_2}$, the conversion gain can be approximated as

$$A_v = \frac{2}{\pi} g_{m1,2} R_{1,2} = \frac{4(I_{2,3})R_{1,2}}{\pi V_{ov}}. \tag{18}$$

To relax the severe trade-off between the conversion gain and noise figure, current bleeding technique is adopted in this design [24]. By injecting currents I_2 and I_3 into the transconductance stage, it can decrease the dc current flowing through the commutating stage and lower the noise contribution from switching pair while sustaining the conversion gain.

The simulated conversion gain of LNA and mixer are about 16.6 dB and 6.7 dB, and noise figure are about 3.5 dB and 13.3

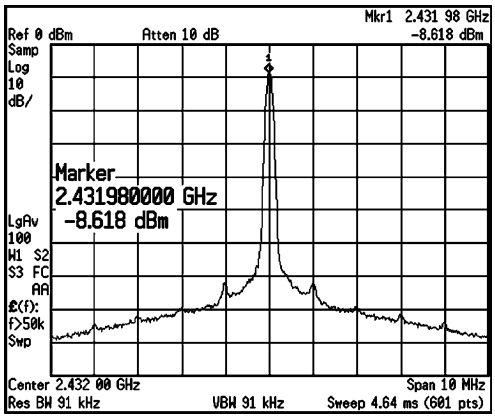

Fig. 16. Measured recover spectrum of the local oscillator.

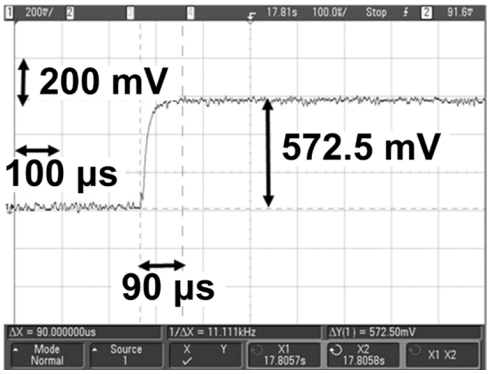

Fig. 17. Measured frequency locking time.

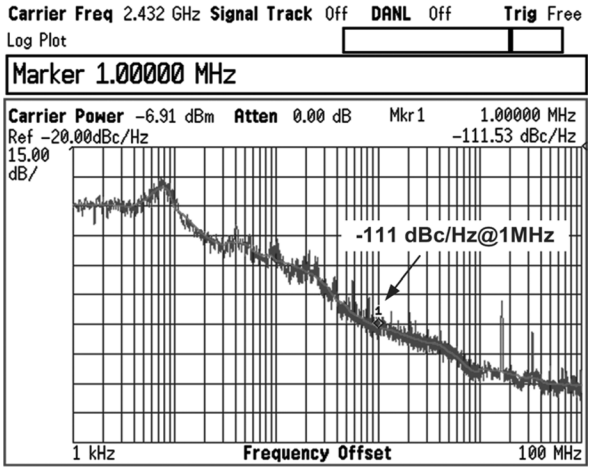

Fig. 18. Measured phase noise performance.

dB respectively. The corresponding single sideband noise figure of front-end circuits is about 7.3 dB.

C. Postamplifier

The received RF signal is amplified to digital output swing by a postamplifier. Fig. 9 shows the circuit schematic. It provides received signal strength indicator (RSSI) to adjust the conversion gain in the receiver front-end. The postamplifier is composed of an offset-cancellation amplifier (A_1) followed by five identical gain cells (A_2) and an offset cancellation network (R_1-R_2, C_1-C_2, A_3).

To achieve low power design goals, all the amplifiers are based on Cherry-Hooper topology [25] to have a better power

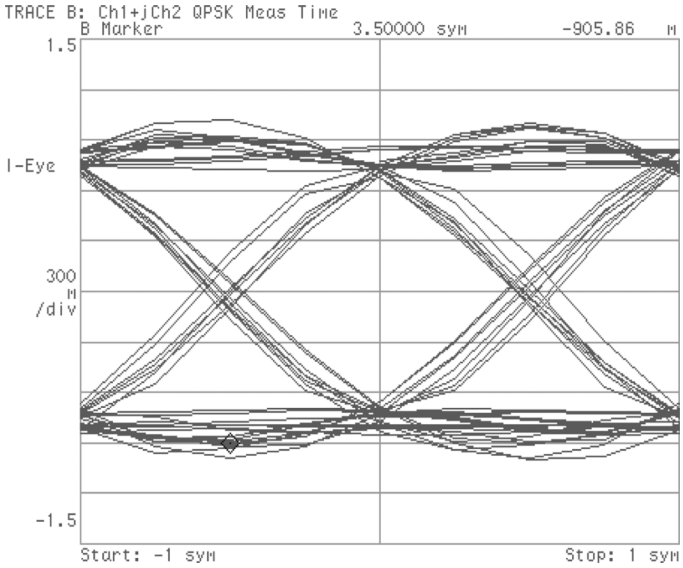

Fig. 19. Eye diagram for demodulated signal.

efficiency in terms of gain-bandwidth performance. Fig. 10 shows the detailed circuit schematic of a gain cell. Here M_1-M_6 performs as a transconductance stage, while M_7-M_{10} and R_F performs as a transimpedance stage.

The common mode feedback loop of the transconductance stage is realized by PMOS operating in linear region (M_5, M_6) to save chip area. The core amplifier of the TIA is an inverter-based architecture for gain enhancement and low power operation by reusing dc biased current. The transfer function of each gain stage can be derived as

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{A_{vo}\omega_n^2}{s^2 + 2\xi\omega_n^2 + \omega_n^2} \tag{19}$$

where

$$\begin{aligned} A_{vo} &\approx \frac{g_{m1}\left[(g_{m7}+g_{m9})R_F - 1\right]}{(g_{m7}+g_{m9}) + 1/r_{\text{out1}} + 1/r_{\text{out2}}} \\ &\approx g_{m1}\left[R_F - \frac{1}{(g_{m7}+g_{m9})}\right] \\ \omega_n^2 &\approx \frac{(g_{m7}+g_{m9}) + 1/r_{\text{out1}} + 1/r_{\text{out2}}}{C_x C_y R_F} \\ r_{\text{out1}} &= r_{o1,2} \| r_{o5,6} \| r_{o3,4}; r_{\text{out2}} = r_{o9,10} \| r_{o7,11} \\ \xi &\approx \frac{C_x + C_y}{2 \times \sqrt{C_x C_y R_F (g_{m7}+g_{m9})}}. \end{aligned}$$

For a maximally-flat Butterworth response ($\zeta \sim 0.707$), the -3 dB bandwidth of the gain stage can be approximated as

$$\omega_{-3\text{ dB}} = \sqrt{\frac{(g_{m7}+g_{m9}) + 1/r_{\text{out1}} + 1/r_{\text{out2}}}{C_x C_y R_F}}. \tag{20}$$

The plateau gain of the postamplifier is about 70 dB and the high frequency -3 dB bandwidth is 80 MHz, which is five times more than the IF bandwidth to alleviate group delay variations.

The RSSI is composed of a RC low-pass filter (R_3 and C_3) and four stage full wave rectifiers (FWR), which are connected to the output of gain cells. Fig. 11 shows the detailed circuit schematic of the full wave rectifier. The input voltage is converted to current form by the differential pair (M_1-M_2), and then

TABLE II
PERFORMANCE BENCHMARK

Reference	This work	[28]	[29]	[30]	[31]	[32]
Center frequency	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
Data rate	1 Mbps	N/A	N/A	200 Kbps	1 Mbps	3 Mbps
Sensitivity (BER < 10^{-3})	-65 dBm	-60 dBm	N/A	-75 dBm	-80 dBm	-84 dBm
LO phase noise	-111 dBc/Hz @1MHz	N/A	-127 dBc/Hz @3MHz	-136 dBc/Hz @1MHz[a]	-111 dBc/Hz @1MHz	-112 dBc/Hz @1MHz
Additional components required	RF filter	RF filter A/D X'tal Osc.	RF filter A/D X'tal Osc.	RF Filter A/D X'tal Osc. BAW Osc. BAW Filter	X'tal Osc.	X'tal Osc.
System level integration	PCB	PCB	Receiver	PCB	Transceiver	Transceiver
Power consumption	20.4 mW	6.3 mW[b]	32.5 mW[c]	18.7 mW[d]	108 mW[e]	35.64 mW[e]
Receiver chip size	2.7 mm^2	N/A	2.9 mm^2	N/A	N/A	N/A
Technology	180 nm CMOS	180 nm CMOS	90 nm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS

(a) BAW DCO locked by a crystal-based ADPLL
(b) LNA and mixer only
(c) LNA, mixer and LO
(d) excludes crystal oscillator
(e) receiver mode

rectified through current mirrors (M_4-M_5) and (M_6-M_7). The dynamic range of RSSI is about 40 dB.

D. Carrier Recovery Loop

The CRL consists of a VCO, prescaler, divider, multiphase generator, phase selector (MUX), and a gating phase frequency detector (GPFD). Incorporating with the data demodulator, it recovers carrier frequency and clock from the QPSK modulation signal for frequency down conversion and data demodulation.

Fig. 12 illustrates the LC tank QVCO. Based on complementary architecture, it improves phase noise performance thanks to a more symmetric output waveform [26]. Also, it benefits from two fold negative conductance for power saving. Here both C_3 and C_4 are accumulation mode MOS varactors for fine frequency tuning. In addition, SC_1 and SC_2 are added in parallel for coarse tuning to cope with PVT variations.

Fig. 13 shows the schematic of charge pump and loop filter. To alleviate reference spurs induced by current mismatch of up and down currents (I_{U2} and I_{D2}) due to channel length modulation, a regulated current feedback loop consisted of A_2, I_{U1}, and I_{D1} is employed. Here I_{U1} and I_{D1} are replicas of I_{U2} and I_{D2}, and the pumping currents can track each other by adjusting the gate voltage of the current source [27].

The divider chain in the feedback path of the CRL is composed of a high speed divided-by-19 divider followed by a divided-by-8 divider, as shown in Fig. 14. The divided-by-19 divider is composed of a 4/5 prescaler, a divide-by-4 divider and a control logic. Fig. 14(b) shows the timing diagram. To reduce power dissipation as well as propagation delay, TSPC flip-flops with embedded NAND gates are incorporated in the dividers, as shown in Fig. 14(c). The synchronous divided-by-8 divider also performs as a multiphase generator. Fig. 14(a) shows the circuit schematic. The 8 phases output signals are then utilized to capture QPSK symbols, and one of them is passed to the GPFD for phase tracking.

V. EXPERIMENTAL RESULTS

The single-chip crystal-less wireless receiver has been fabricated in a 0.18 μ m CMOS process, and powered by a 1.8 V supply. A single channel experimental prototype is implemented to demonstrate the concept. The power dissipation for the RF/analog front-end ($\mathrm{LNA} + \mathrm{mixer} + \mathrm{post\ amplifier} + \mathrm{channel\ selection\ filter}$) is about 9.6 mW, while the data demodulator and CRL consumes about 10.8 mW. Fig. 15 shows the chip photograph. The chip size is 1.75×1.55 mm^2, and is mounted on a printed circuit board for measurement.

The rejection of out band interferers mainly relies on external band selection filter. By using TA0532A SAW filter, the out band interferers are suppressed 40 dB. Besides, a 6th order low pass filter is implemented incorporating postamplifier for channel selection in this design. To emulate the RF signal at the transmitter side, a 1 Mbps QPSK modulated signal is generated by Tekronix AWG7000B arbitrary waveform generator, and then up converted to 2.416 GHz through R&S SMIQ03 signal generator. For $\mathrm{BER} < 10^{-3}$, the in band signal to interference ratio must be higher than 15 dB to maintain phase locked. With -65 dBm input signal at the receiver side the measured recovered spectrum is shown in Fig. 16. It can be seen that the closest spurs are at 1 MHz offset corresponding to the data rate. The sensitivity can be further improved by reducing signal

loss caused by chip on board assembly, and also modifying the IF amplifier and channel selection filters architecture to bandpass instead of lowpass.

The measured settling time of the CRL is shown in Fig. 17, the duration of preamble should be larger than 90 μsec for frequency synchronization. The proposed architecture can extract the carrier frequency directly from the RF signal without resort to extra resonator based reference. The measured phase noise performance is shown in Fig. 18, which is about -111 dBc/Hz at 1 MHz offset. Fig. 19 shows the eye diagram of demodulated I/Q signal. It reveals clear eye for the data demodulation as well.

Table II shows the performance benchmark for 2.4 GHz wireless sensor applications. Compared to the prior art, the proposed receiver accomplishes frequency down conversion as well as OQPSK demodulation without extra ADCs, on chip reference, and additional carrier recovery loops in the base band. It achieves much higher data rate (1 Mbps) in contrast to the prior art.

VI. Conclusion

This paper proposes a novel single chip wireless QPSK receiver without resort to extra resonator based reference. In contrast to conventional architectures, the receiver recovers the RF carrier frequency directly from the incident radio signal for frequency down conversion. Meanwhile, it accomplishes phase and frequency tracking as well as QPSK demodulation simultaneously. Thus, no additional baseband ADCs or timing recovery loop are required in this receiver. It greatly improves the system integration level.

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