

Performance Enhancement of Thin-Film Transistors With Suspended Poly-Si Nanowire Channels by Embedding Silicon Nanocrystals in Gate Nitride

Chia-Hao Kuo, Horng-Chih Lin, *Senior Member, IEEE*, and Tiao-Yuan Huang, *Fellow, IEEE*

Abstract—In this letter, we fabricated and characterized thin-film transistors with a suspended poly-Si nanowire (NW) channel and gate nitride with embedded silicon nanocrystals (Si NCs). The embedded Si NCs increase the surface roughness, thus reducing the adhesive force as the nitride is in contact with the poly-Si NW channel during the operation. Such a feature results in a reduction in pull-in voltage and sharper pull-out behavior. Moreover, this approach also greatly improves the endurance characteristics of the devices.

Index Terms—Adhesive force, nanocrystal (NC), nanowire (NW), poly-Si.

I. INTRODUCTION

MICROELECTROMECHANICAL MOSFETs have recently drawn considerable attention and been widely studied because of their potential applications in several areas, such as switches, resonators, memory, and sensor devices [1]–[7]. One important issue associated with most suspended-type devices is the high operation voltage (> 5 V), which makes it incompatible with nowadays CMOS design [1], [2], [6]. To overcome this hurdle, we have recently proposed a novel device with suspended poly-Si nanowire (NW) channels, which can effectively decrease the operation voltage by shrinking the air gap thickness down to the sub-100-nm regime [8]. This allows the pull-in of the suspended channel to occur at a gate voltage smaller than 2 V. Moreover, owing to the tiny NW channels, the ratio between the etch depth and thickness of the sacrificial oxide is significantly reduced, allowing the use of a simple wet chemical etch step to release the suspended object. Nevertheless, we have also found that the endurance of the fabricated devices is only mediocre. That is, significant shrinkage in the window between the two logic states is usually observed within a few hundreds of cycles. To address this issue,

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C.-H. Kuo and T.-Y. Huang are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan.

H.-C. Lin is with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the National Nano Device Laboratories, Hsinchu 300, Taiwan (e-mail: hc.lin@faculty.nctu.edu.tw).

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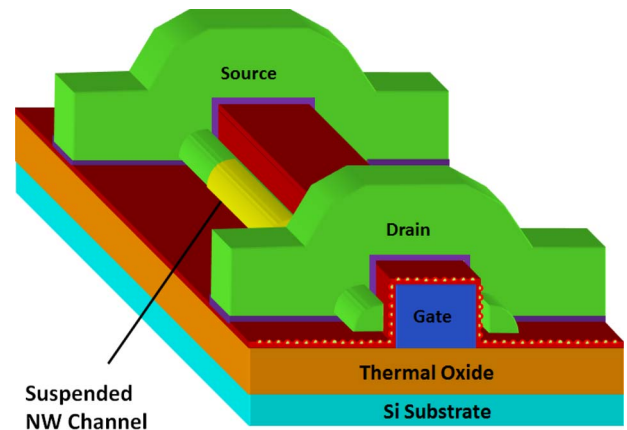


Fig. 1. Schematic structure of the device with Si NCs embedded in the gate nitride.

in this letter, we present an improved version by incorporating silicon nanocrystals (Si NCs) in the gate nitride layer of the suspended NW channel.

II. DEVICE STRUCTURE AND FABRICATION

Fig. 1 depicts the schematic structure of the device with Si NCs incorporated. The fabrication process of the device is basically the same as that described in [8] and [9]. In brief, after the formation of an n^+ poly-Si gate on a Si wafer capped with a thermal oxide, SiN (20 nm), sacrificial oxide (40 nm), and poly-Si (100 nm) were subsequently deposited. Afterward, source/drain (S/D) regions were lithographically defined, whereas poly-Si NW channels were defined by using the sidewall spacer etching techniques [10]. To suspend the NW channels, the sacrificial oxide between the NW and the gate nitride was then selectively removed with an HF-containing solution. In this letter, the Si NCs incorporation was done with the following procedure conducted in a low-pressure chemical vapor deposition system at 700 °C [11]. First, a 15-nm-thick bottom SiN was deposited with dichlorosilane (SiCl_2H_2 , 65 sccm) and ammonia (NH_3 , 15 sccm) gases. Subsequently, by turning off the NH_3 gas flow and increasing the flow rate of the dichlorosilane to 100 sccm, Si NCs are *in situ* formed on the surface of the deposited nitride. The duration of this period is 45 s. Finally, a 5-nm-thick top-SiN with a flow rate condition identical to that of the bottom one was deposited to cover the Si NCs. For comparison purposes, control devices with a single 20-nm-thick SiN layer were also fabricated.

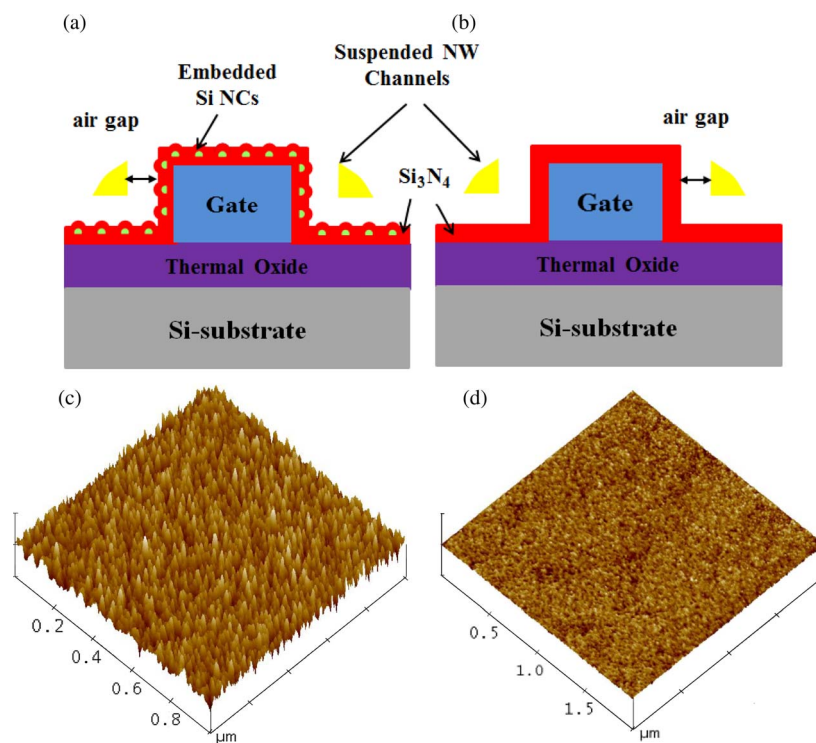


Fig. 2. Cross-sectional schematics of devices (a) with and (b) without Si NCs embedded in the nitride film and AFM images of blanket nitride films (c) with and (d) without Si NC dots incorporated ($1 \mu\text{m} \times 1 \mu\text{m}$ scan size).

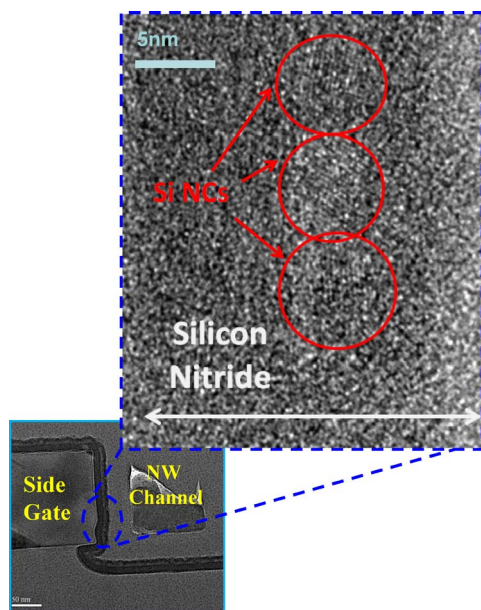


Fig. 3. Cross-sectional TEM picture of a device with Si NCs. The picture was taken before the sacrificial oxide was removed. Inset shows an enlarged view of the Si NCs in the silicon nitride.

The cross-sectional views of the fabricated devices with and without embedded Si NCs in the SiN layer are shown in Fig. 2(a) and (b), respectively. Fig. 2(c) and (d) displays the atomic force microscopic (AFM) images ($1 \times 1 \mu\text{m}^2$) taken from blanket SiN films with and without embedded Si NCs, respectively. The root-mean-square roughness values of the SiN films with and without embedded Si NCs were 0.703 and 0.234 nm, respectively. The density of Si NC dots in Fig. 2(c) is estimated to be around $5 \times 10^{11} \text{ cm}^{-2}$. Fig. 3 displays the cross-

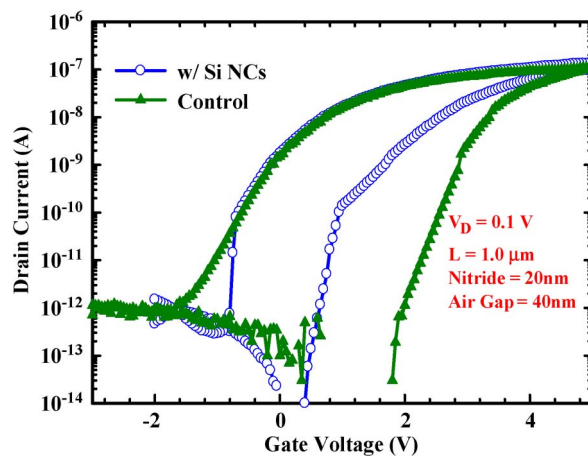


Fig. 4. Hysteresis I - V characteristics of the fabricated devices with and without embedded Si NCs.

sectional transmission electron microscopic (TEM) image of a fabricated device taken prior to the stripping of the sacrificial oxide layer. In the picture, the embedded Si NCs in the SiN are clearly observed.

III. RESULTS AND DISCUSSION

Typical hysteresis characteristics of devices with and without embedded Si NCs are shown in Fig. 4. It is shown in the figure that the turn-on of the device can be triggered at a much smaller gate voltage (V_G) as Si NCs are incorporated. As mentioned in the previous section, the presence of the Si NCs roughens the nitride surface, and the electric field strength near the protruding nitride surface is enhanced during operation. Such feature may increase the effective electrostatic force between the gate

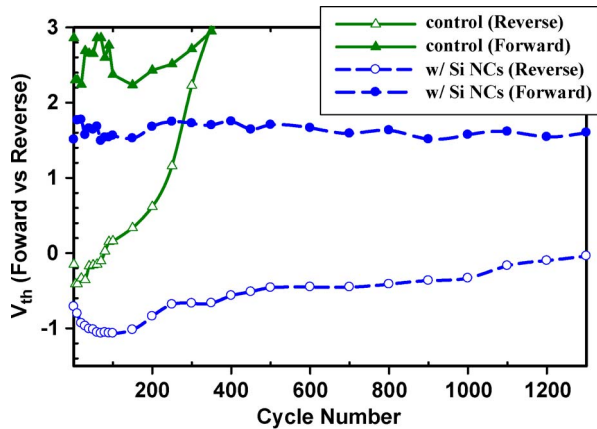


Fig. 5. Endurance characteristics of devices with and without embedded Si NCs.

and the channel at a specific V_G , explaining the experimental observation.

In addition, for the control device, it is shown in Fig. 4 that the subthreshold characteristics of the forward sweeping curve is much steeper than the reverse one. This effect can be explained by the presence of an additional adhesive force while the channels are in intimate contact with the gate nitride, which would retard the detachment of suspended NWs from the gate nitride [12]. On the other hand, the device with Si NCs exhibits a sudden drop in the reverse sweeping with subthreshold swing (SS) of ~ 49 mV/dec. This is again attributed to its roughened gate nitride surface. As the gate voltage is swept backward to release the electrically attractive force between the two objects, the adhesive force existing in the contact portion of the gate nitride and the NW channel would become the dominant component to balance the restoring force coming from the displacement of the NW channels [13]. For nitride with Si NCs incorporated, the increased surface roughness reduces the effective contact area between the nitride and the suspended channel and thus the associated adhesive force. As a consequence, the pull-off action of the suspended NW channels can be triggered earlier than the control sample and results in a steeper SS.

Another important advantage offered by the proposed embedded-Si-NCs approach is the improvement of device reliability. Fig. 5 shows the measured endurance characteristics of devices with and without embedded Si NCs. For simplicity, V_{th} is defined as $V_G @ I_D = 10 \text{ nA} \times (W/L)$. The cycling tests were executed with cycles of consecutive forward and reverse sweeping measurements. In the figure, V_{th} values of both forward and reverse sweeping curves are recorded, and the difference between the two states is defined as the window size. It can be seen that, for the control device, the failure in terms of window shrinkage occurs after roughly 250 cycles. The failure mechanism is postulated to be related to the stiction or the contact fatigue of NWs [14]. On the other hand, considerable window size remains for the device with embedded Si NCs even after 1300 cycles. As the occurrence of stiction is closely related to the adhesive force between the contacted objects [13], [14],

obviously, the reduced effective contact area of the roughened nitride surface with the aforementioned NCs also benefits the endurance characteristics of the device operation.

IV. CONCLUSION

In this letter, we have refined a recently developed fabrication process by incorporating Si NCs in the gate nitride layer of the device with suspended poly-Si NW channels. With this refinement, significant performance improvements in terms of reduced turn-on voltage and meliorated endurance characteristics are demonstrated. These improvements are believed to be related to the roughened surface of the nitride with embedded Si NCs.

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