

A Closed-Form Quantum “Dark Space” Model for Predicting the Electrostatic Integrity of Germanium MOSFETs With High- k Gate Dielectric

Yu-Sheng Wu, *Student Member, IEEE*, and Pin Su, *Member, IEEE*

Abstract—This paper provides a closed-form model of the “dark space (DS)” for Ge MOSFETs with high- k gate dielectrics. This model shows accurate dependences on barrier height, surface electric field, and quantization effective mass of the channel and gate dielectric. Our model predicts that the surface DS due to quantum confinement decreases with reverse substrate bias and increasing channel doping. Our model can be also used for devices with a steep retrograde doping profile. This physically accurate model will be crucial to the prediction of the subthreshold swing and electrostatic integrity of advanced Ge devices.

Index Terms—Closed-form model, dark space (DS), eigenenergy, germanium, wavefunction penetration (WP).

I. INTRODUCTION

AS THE HIGH- k /metal-gate stack is introduced to continue scaling of equivalent oxide thickness (EOT), high-mobility channel materials such as Ge have been proposed to compensate for the mobility loss due to the high- k gate stack [1], [2]. However, larger “dark space (DS)” [3]–[8] due to quantum confinement is one major concern for Ge devices because it may significantly increase the overall equivalent electrical oxide thickness [9] (EOT_e or CET) in the subthreshold region and degrade the device electrostatic integrity. Since the quantum-confinement effect pushes the carriers away from the interface, “DS” can be viewed as the distance from the interface to the centroid of the carrier layer (normalized with the permittivity ratio) [4], [5]. With the triangular well and infinite oxide barrier approximations, a carrier layer thickness model for Si channel had been proposed in the past [10]. However, for Ge channel devices with high- k gate dielectric, these approximations may result in significant error in the prediction of the DS because of the small effective mass of the channel carrier and the finite dielectric barrier height. Although the impact of finite barrier

height on Si devices has been considered by empirically fitting the ground-state eigenenergy dependence on the surface electric field with numerical simulation recently [11], [12], the fitting results were not scalable and not applicable for Ge devices.

In this paper, we provide a closed-form DS model for Ge MOSFETs with high- k dielectrics. This model gives insights to the minimization of the DS, and it can be used to predict the electrostatic integrity of advanced Ge devices. This paper is organized as follows. In Section II, we derive the closed-form models for the ground-state eigenenergy and the DS. In Section III, we verify our model with technology-computer-aided-design (TCAD) simulation. In addition, the application of our DS model on the prediction of the subthreshold swing (SS) is demonstrated. Finally, we draw the conclusion in Section IV.

II. DS MODELING

As the DS increases overall EOT_e and hence degrades the SS, a closed-form model of the DS can be derived through the SS. The SS is defined as $(d \log_{10}(Q_i)/dV_G)^{-1}$ with Q_i being the sheet carrier density, which is proportional to $\ln[1 + \exp(-(E_{C,\text{surf}} + E_0 - E_F)/kT)]$ [10] under the ground-state approximation (i.e., most carriers populate at the ground state for Ge channel). $E_{C,\text{surf}}$, E_0 , and E_F are the conduction band edge at the surface, ground-state eigenenergy, and Fermi level, respectively. When E_F is sufficiently smaller than $E_{C,\text{surf}} + E_0$ (e.g., in the subthreshold region), Q_i is proportional to $\exp(-(E_{C,\text{surf}} + E_0 - E_F)/kT)$. Therefore, the SS can be expressed as

$$\text{SS} = \left(\frac{kT}{q}\right) \cdot \ln(10) \cdot \left\{ 1 - \frac{dF_S}{dV_G} \cdot \frac{\varepsilon_{\text{ch}}}{\varepsilon_{\text{di}}} \cdot \left[T_{\text{di}} + \frac{d\left(\frac{E_0}{q}\right)}{dF_S} \right] \right\}^{-1} \quad (1)$$

with ε_{ch} and ε_{di} being the permittivity of the channel and the gate dielectric, respectively. T_{di} is the thickness of the gate dielectric, and F_S is the surface electric field in the channel. Equation (1) shows that carrier centroid X_0 due to quantum confinement can be expressed as

$$X_0 = d(E_0/q)/dF_S \quad (2)$$

and $\text{DS} = X_0/(\varepsilon_{\text{ch}}/\varepsilon_{\text{ox}})$. Fig. 1 shows that (2) returns to $2E_0/(3qF_S)$ [10] for a triangular potential well with infinite oxide barrier ϕ_b , under which $E_0 = (\hbar^2/(2m_{\text{ch}}))^{1/3} \cdot (9/8 \cdot \pi \cdot$

Manuscript received July 28, 2011; revised September 30, 2011 and November 14, 2011; accepted November 15, 2011. Date of publication December 19, 2011; date of current version February 23, 2012. This work was supported in part by the National Science Council of Taiwan under Contract NSC 100-2628-E-009-024-MY2 and in part by the Ministry of Education in Taiwan under the Aim for the Top University Program. The review of this paper was arranged by Editor J. C. S. Woo.

The authors are with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 30013, Taiwan (e-mail: pinsu@faculty.nctu.edu.tw).

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Digital Object Identifier 10.1109/TED.2011.2177091

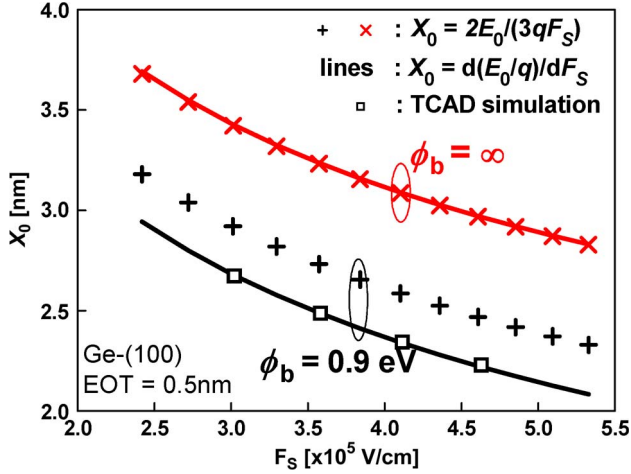


Fig. 1. Comparison of the two expressions of carrier centroid X_0 . The X_0 from the TCAD simulation [13] is calculated by $(\int x \cdot \Psi_0^2(x) dx) / (\int \Psi_0^2(x) dx)$ with $\Psi_0(x)$ being the spatial distribution of the ground-state wavefunction.

$qF_S)^{2/3}$ [10]. However, for high- k dielectric with finite barrier height ($\phi_b = 0.9$ eV), X_0 calculated by (2) agrees with the TCAD simulation [13], and it is significantly smaller than $2E_0/(3qF_S)$. In other words, (2) is a more general expression for X_0 .

To derive a DS model for a Ge channel with small quantization effective mass m_{ch} , a more accurate $E_0 - F_S$ relationship than the one used in [10] needs to be employed. First, for a uniformly doped channel with doping concentration N_{ch} (negative for p-type substrate), a parabolic channel potential well $V_{ch}(x) = q \cdot [F_S \cdot x + (qN_{ch}/2\varepsilon_{ch}) \cdot x^2]$ has to be used in the derivation of ground-state eigenenergy E_0 . Using the perturbation theory [14] and treating the $q \cdot (qN_{ch}/2\varepsilon_{ch}) \cdot x^2$ term as a perturbation to the triangular well $V_{ch,tri}(x) = q \cdot F_S \cdot x$, E_0 can be expressed as $E_{0,tri} + q \cdot (qN_{ch}/2\varepsilon_{ch}) \cdot \int x^2 \cdot \Psi_{0,tri}^2(x) dx$ with $E_{0,tri}$ and $\Psi_{0,tri}(x)$ being the ground-state eigenenergy and wavefunction of triangular well $V_{ch,tri}(x)$, respectively. It can be further shown that

$$E_0 = E_{0,tri} + (4/15) \cdot (N_{ch}/\varepsilon_{ch}) \cdot (E_{0,tri}/F_S)^2. \quad (3)$$

To derive an accurate $E_{0,tri}$ for Ge devices with high- k dielectrics, the wavefunction penetration (WP) effect needs to be considered. The wavefunction $\Psi_{0,tri}(x)$ for the channel carrier can be expressed as [10]

$$\Psi_{0,tri}(x) = c_1 \cdot Ai(k_{ch} \cdot (x - x_{ch})) \quad (4)$$

where $k_{ch} = (2m_{ch}qF_S/\hbar^2)^{1/3}$, $x_{ch} = E_{0,tri}/(qF_S)$, and $Ai(x)$ is the Airy function of the first kind. When the dielectric barrier height is reduced from infinity to a finite ϕ_b , $E_{0,tri}$ is reduced by $\Delta E_{0,tri} = E_{0,tri}(\phi_b = \infty) - E_{0,tri}(\phi_b)$ because of WP. Equation (4) indicates that the wavefunction (and, hence, the carrier distribution) will be shifted toward the interface by $x_{ch}(\phi_b = \infty) - x_{ch}(\phi_b) [= \Delta E_{0,tri}/(qF_S)]$, which is responsible for the X_0 reduction $X_0(\phi_b = \infty) - X_0(\phi_b) [= d(\Delta E_{0,tri}/q)/dF_S]$. Hence, $d\Delta E_{0,tri}/dF_S \cong \Delta E_{0,tri}/F_S$. In other words, $\Delta E_{0,tri} \cong \alpha \cdot F_S$ with α being a coefficient independent of F_S .

To derive coefficient α , the wavefunction in the gate dielectric $\Psi_{0,di}(x)$ is needed. Since the potential well in the dielectric is $V_{di}(x) = (\varepsilon_{ch}/\varepsilon_{di}) \cdot q \cdot F_S \cdot x + \phi_b$, $\Psi_{0,di}(x)$ can be expressed as

$$\Psi_{0,di}(x) = c_2 \cdot Ai(k_{di} \cdot (x - x_{di})) + c_3 \cdot Bi(k_{di} \cdot (x - x_{di})) \quad (5)$$

where $k_{di} = (2m_{di}(\varepsilon_{ch}/\varepsilon_{di})qF_S/\hbar^2)^{1/3}$, $x_{di} = (E_{0,tri} - q\phi_b)/(\varepsilon_{ch}/\varepsilon_{di} \cdot qF_S)$, m_{di} is the effective mass in the dielectric, and $Bi(x)$ is the Airy function of the second kind. Using the boundary conditions that the eigenfunction and its first derivative divided by the carrier effective mass are continuous across the channel/dielectric interface ($x = 0$) and $\Psi_{0,di}$ vanishes at the dielectric boundary ($x = -T_{di}$), it can be shown that $E_{0,tri}$ satisfies the following nonlinear equation:

$$[Ai(-k_{ch} \cdot x_{ch}) \cdot Bi'(-k_{di} \cdot x_{di}) - (m_{di}/m_{ch}) \cdot (k_{di}/k_{ch}) \cdot Bi(-k_{di} \cdot x_{di}) \cdot Ai'(-k_{ch} \cdot x_{ch})] \cdot Ai(-k_{di} \cdot (x_{di} + T_{di})) = 0 \quad (6)$$

where $Ai'(x)$ and $Bi'(x)$ are the first derivatives of $Ai(x)$ and $Bi(x)$, respectively. Using the first-order Taylor expansion for (6) around $E_{0,tri}(\phi_b = \infty)$, we can derive the dependences of $\Delta E_{0,tri}$ on m_{ch} , m_{di} , and ϕ_b , and then α can be obtained as

$$\alpha = q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}} \right). \quad (7)$$

Therefore, $E_{0,tri}$ can be expressed as

$$E_{0,tri} = \left(\frac{\hbar^2}{2m_{ch}} \right)^{1/3} \cdot \left(\frac{9}{8} \pi \cdot qF_S \right)^{2/3} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}} \right) \cdot F_S. \quad (8)$$

Substituting (8) into (3), we can obtain a closed-form model for E_0

$$E_0 = \left(\frac{\hbar^2}{2m_{ch}} \right)^{1/3} \cdot \left(\frac{9}{8} \pi \cdot qF_S \right)^{2/3} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}} \right) \cdot F_S + \frac{4}{15} \cdot \frac{N_{ch}}{\varepsilon_{ch}} \cdot \left[\left(\frac{\hbar^2}{2m_{ch}F_S} \right)^{1/3} \cdot \left(\frac{9}{8} \pi \cdot q \right)^{2/3} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}} \right) \right]^2. \quad (9)$$

It is shown in (9) that E_0 is not exactly proportional to $(F_S)^\lambda$ [11]. This explains why in [11] λ has to be treated as a fitting parameter as relation $E_0 \propto (F_S)^\lambda$ was used. In addition, although λ had been empirically derived by introducing several fitting parameters to consider the ϕ_b and N_{ch} dependence values [12], the m_{ch} and m_{di} dependences were not considered. Therefore, the fitting parameters used in [12] cannot be employed for devices with different channel and dielectric materials.

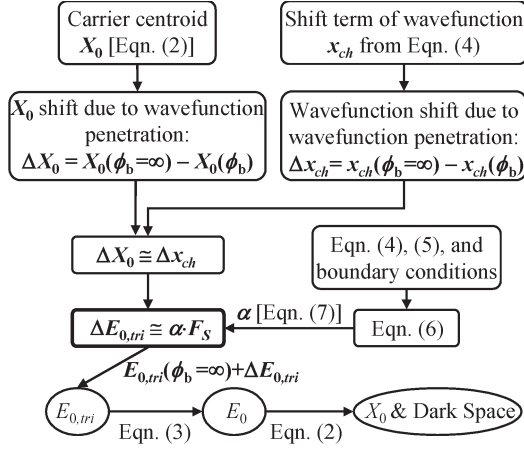


Fig. 2. Flowchart demonstrating the derivation of the closed-form model for DS considering the parabolic well and the WP effect.

Using (2), we can obtain a closed-form model for carrier centroid X_0

$$X_0 = \left[\frac{2}{3} \left(\frac{\hbar^2}{2m_{ch}qF_S} \right)^{\frac{1}{3}} \cdot \left(\frac{9}{8}\pi \right)^{\frac{2}{3}} - \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}} \right) \right] \cdot \left\{ 1 + \frac{8}{15} \frac{N_{ch}}{\varepsilon_{ch}} \left[\left(\frac{\hbar^2}{2m_{ch}F_S^4} \right)^{\frac{1}{3}} \cdot \left(\frac{9}{8}\pi \cdot q \right)^{\frac{2}{3}} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}} \right) \cdot \frac{1}{F_S} \right] \right\} - \frac{8}{15} \frac{N_{ch}}{\varepsilon_{ch}} \frac{1}{qF_S^3} \cdot \left[\left(\frac{\hbar^2}{2m_{ch}} \right)^{\frac{1}{3}} \cdot \left(\frac{9}{8}\pi \cdot qF_S \right)^{\frac{2}{3}} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}} \right) \cdot F_S \right]^2 \quad (10)$$

After normalization with the permittivity ratio, the DS can be determined by $X_0/(\varepsilon_{ch}/\varepsilon_{ox})$. Fig. 2 summarizes the derivation procedures of the closed-form model for the DS.

III. VERIFICATION AND APPLICATION ON SS

To verify our closed-form model of E_0 and DS, we have performed the TCAD simulation that numerically solves the self-consistent solution of coupled Poisson and Schrödinger equations [13]. For a given F_S near the onset of threshold, Fig. 3 shows that E_0 for Ge-(100) and Si-(100) nMOS devices decreases with barrier height ϕ_b because of the WP effect, and our model agrees well with the TCAD simulation. In addition, the E_0 reduction for Ge-(100) is more significant than that for Si-(100) because Ge-(100) possesses smaller m_{ch} and, hence, larger α [see (7)]. Fig. 4(a) indicates that, when the WP effect is not considered, the X_0 of Ge-(100) is significantly larger than that of Si-(100). When the WP effect is considered, however, the discrepancy of X_0 for Ge-(100) and Si-(100) is substantially reduced because of the more significant reduction of X_0 for Ge-(100). After normalization with the permittivity ratio, Fig. 4(b) shows that the discrepancy of the DS for Ge-(100)

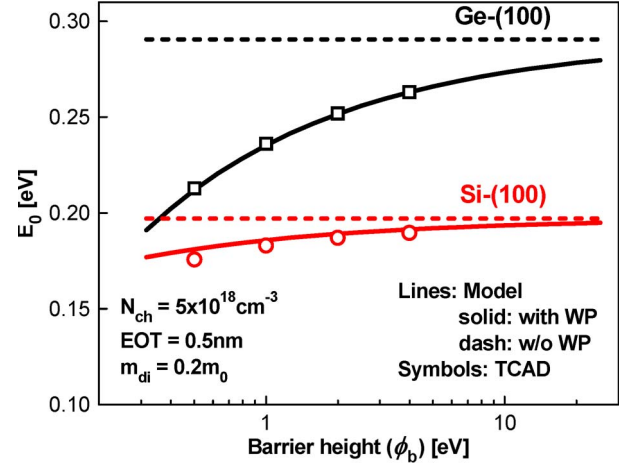


Fig. 3. Barrier height dependences of E_0 for Si-(100) and Ge-(100) surfaces with and without considering the WP effect. Although all results shown in this paper are for nFET, our model is also applicable for pFET.

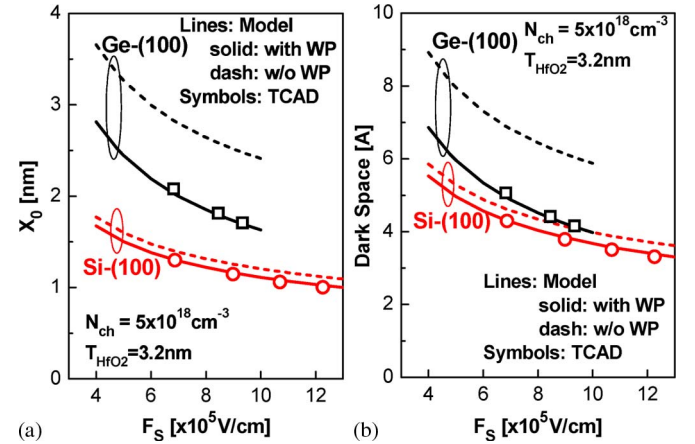


Fig. 4. (a) Comparison of X_0 for Si-(100) and Ge-(100) surfaces with and without considering the WP effect. ϕ_b and m_{di} used for HfO_2 are 0.9 eV and $0.2m_0$ [15], respectively. (b) The DS is directly derived by the results from (a) divided by $(\varepsilon_{ch}/\varepsilon_{ox})$.

and Si-(100) will be further reduced because of the higher permittivity for Ge channel. The discrepancy of the DS becomes smaller than 1 \AA for the F_S near the onset of threshold. Fig. 5 shows that the DS depends on the surface orientation because of the different quantization effective mass m_{ch} . Since the DS increases with decreasing m_{ch} , the DS of the Ge-(100) surface is larger than those of the Ge-(110) and Ge-(111) counterparts. This is contrary to the Si devices that the DS of the (100) surface is smaller than those of the (110) and (111) counterparts. The DS also depends on the material of gate dielectric because the properties of gate dielectric such as ϕ_b and m_{di} will determine the degree of the WP effect. Fig. 6 shows that, among the three high- k dielectrics, HfO_2 possesses smaller DS than Al_2O_3 and La_2O_3 .

Since F_S is related to N_{ch} and can be modulated by substrate bias V_{sub} , the DS also depends on N_{ch} and V_{sub} . As the F_S near the onset of threshold is $[2qN_{ch} \cdot (2\varphi_B - V_{sub})/\varepsilon_{ch}]^{1/2}$ ($\varphi_B = (kT/q) \cdot \ln(N_{ch}/n_i)$, where n_i is the intrinsic carrier concentration), F_S increases with N_{ch} and reversed V_{sub} . Fig. 7 shows that the DS near the onset of threshold decreases with

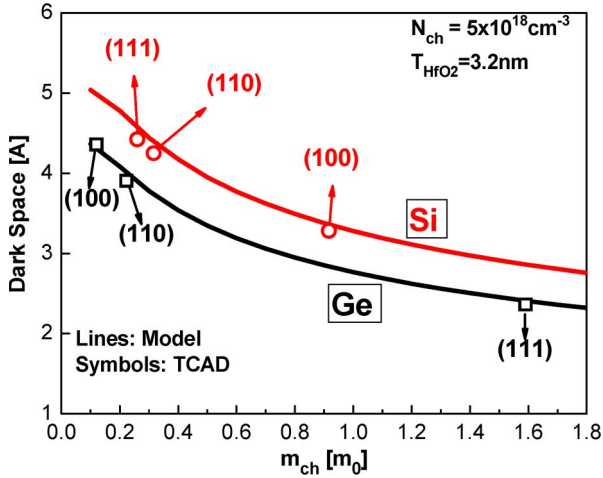


Fig. 5. Impact of channel quantization effective mass and surface orientation on the DS of Si and Ge devices. The curve of Ge is below that of Si because of the higher ($\epsilon_{ch}/\epsilon_{ox}$) ratio for Ge. For Ge nFET, the m_{ch} for (100), (110), and (111) surfaces are $0.12m_0$, $0.223m_0$, and $1.59m_0$, respectively [16]. For Si nFET, the m_{ch} for (100), (110), and (111) surfaces are $0.916m_0$, $0.316m_0$, and $0.26m_0$, respectively [16].

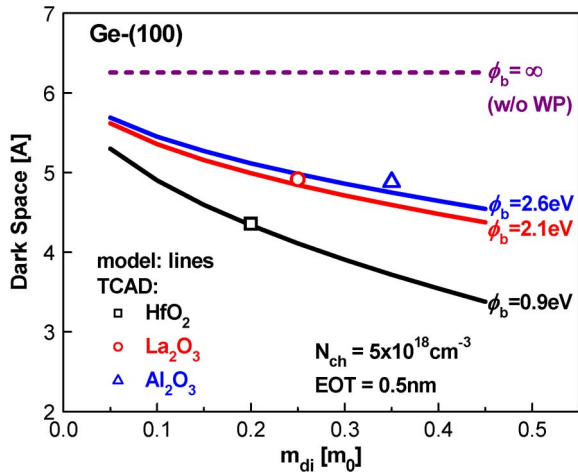


Fig. 6. Impact of gate dielectric material on the DS of the Ge-(100) device. ϕ_b used for La_2O_3 and Al_2O_3 are 2.1 and 2.6 eV, respectively. m_{di} used for La_2O_3 and Al_2O_3 are $0.25m_0$ and $0.35m_0$, respectively [15].

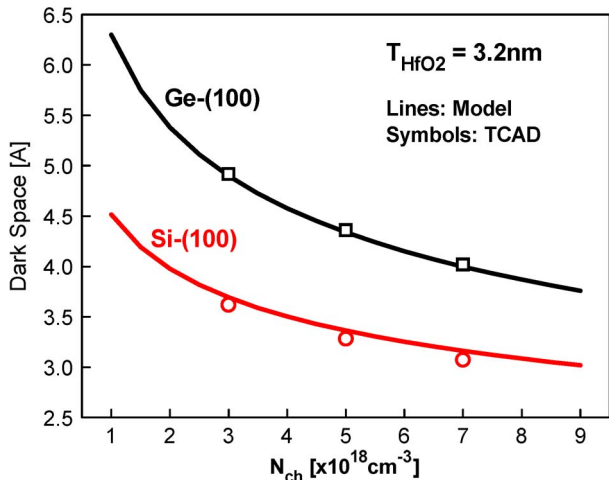


Fig. 7. Channel doping dependence values of the DS for Si-(100) and Ge-(100) surfaces.

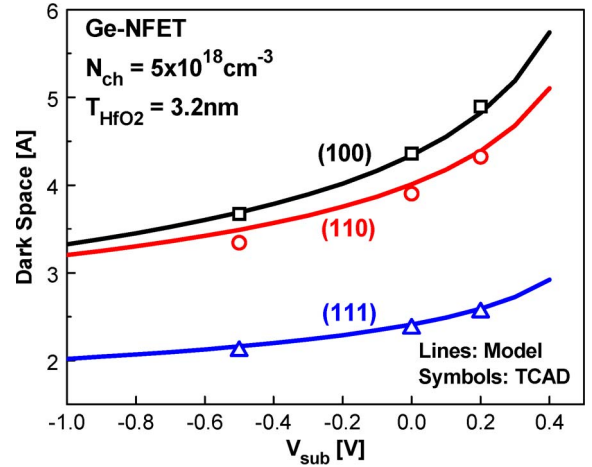


Fig. 8. Substrate bias dependences of the DS for Ge nFET with various surface orientations.

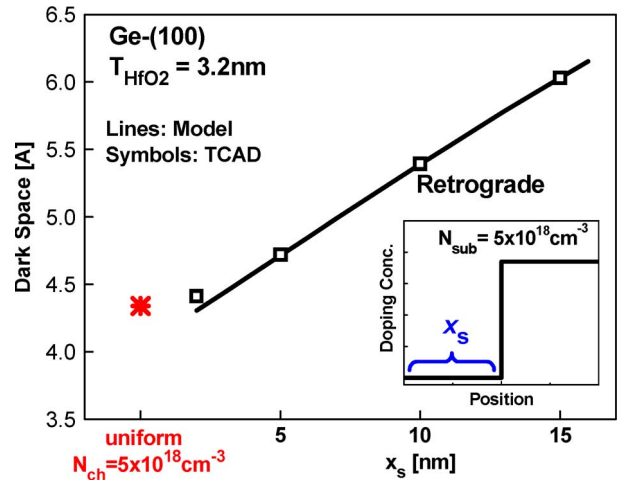


Fig. 9. Comparison of DS for a steep retrograde doping profile with various intrinsic region depths x_s and the uniform doping profile.

increasing N_{ch} because the DS decreases with increasing F_S (see Fig. 4). Similarly, Fig. 8 indicates that applying reversed V_{sub} will reduce the DS because of larger F_S . In addition, it is shown that the Ge-(100) surface exhibits higher DS sensitivity to V_{sub} than the Ge-(110) and Ge-(111) counterparts.

In addition to the uniform doping profile, our model is also applicable for devices with a steep retrograde doping profile [8]. For an ideal retrograde doping profile with an intrinsic region near the interface (see the inset in Fig. 9), F_S is constant and the potential well is triangular. Therefore, the $E_{0,tri}$ in (8) can be applied to the ground-state eigenenergy for a steep retrograde profile. $X_{0,tri}$ can be derived by $d(E_{0,tri}/q)/dF_S$

$$X_{0,tri} = \left[\frac{2}{3} \left(\frac{\hbar^2}{2m_{ch}} \right)^{\frac{1}{3}} \cdot \left(\frac{9}{8} \pi \cdot q \right)^{\frac{2}{3}} \cdot F_S^{-\frac{1}{3}} - q \cdot \frac{\hbar}{\sqrt{2}} \cdot \left(\frac{\sqrt{m_{di}}}{\sqrt{q\phi_b}} \cdot \frac{1}{m_{ch}} \right) \right]. \quad (11)$$

The DS for a steep retrograde profile can be determined by $X_{0,tri}/(\epsilon_{ch}/\epsilon_{ox})$. Fig. 9 shows that, for a given heavily doped

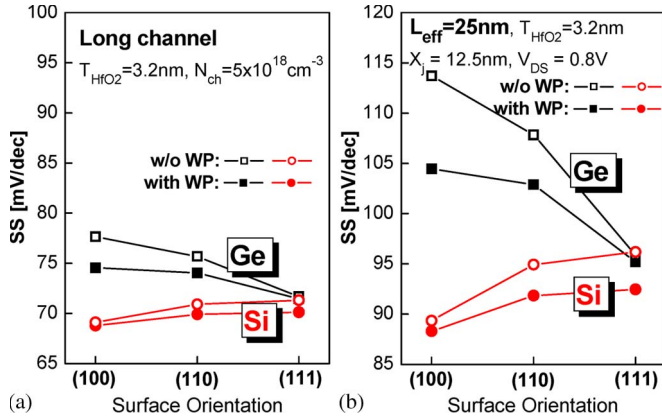


Fig. 10. (a) Comparison of the long-channel SS for Ge nFET and Si nFET with various orientations. (b) Comparison of the short-channel ($L_{\text{eff}} = 25 \text{ nm}$) SS for Ge nFET and Si nFET with various orientations.

substrate doping ($N_{\text{sub}} = 5 \times 10^{18} \text{ cm}^{-3}$), the DS decreases with intrinsic region depth x_s . This is because the F_S near the onset of threshold increases with decreasing x_s . As the uniformly doped channel is similar to a steep retrograde profile with $x_s = 0$, it is shown in Fig. 9 that the DS of the uniformly doped profile is smaller than that of a steep retrograde profile.

With the closed-form DS model, we can assess the SS of Ge devices with high- k dielectric by incorporating $\text{EOT}_e = \text{EOT} + \text{DS}$ in the SS model [2], [7], [17]. In this paper, we use the reported analytical SS model for short-channel bulk devices [17]

$$\text{SS} = \frac{kT}{q} \ln(10) \cdot \left(1 - \frac{\text{EOT}_e}{\varepsilon_{\text{ox}}} \cdot \left(-\frac{qN_{\text{ch}}\Delta W_{\text{dep}}}{\phi_f} + \frac{2\varepsilon_{\text{ch}}X_j}{L_{\text{eff}}^2} \cdot \frac{\Delta\nu}{\phi_f} \right) \right) \quad (12)$$

where L_{eff} and X_j are the effective channel length and the junction depth of source/drain, respectively. The definitions of ΔW_{dep} , $\Delta\nu$, and ϕ_f can be referred to [17]. Fig. 10(a) shows that, for long-channel Ge nFETs, the calculated SS of Ge-(100) is larger than those of the Ge-(110) and Ge-(111) counterparts, as predicted by the DS in Fig. 5. Moreover, the reduction in SS for Ge-(100) due to the WP effect is more significant than that for the Si-(100) counterpart. Fig. 10(b) further shows that this reduction in SS for Ge devices due to the WP effect increases for short-channel devices.

For the Ge devices in this paper, only L-valley is considered in our calculation because other conduction band bottoms such as Γ - and X-valleys have energy offsets of 0.135 and 0.173 eV, respectively, higher than the L-valley [18]. The relative importance of Γ - and X-valleys may increase when the E_0 of Γ - and X-valleys plus the energy offset get close to the E_0 of the L-valley. For the Ge-(100) surface with increasing F_S , although the X-valley possesses larger m_{ch} ($0.27m_0$) than the L-valley ($m_{\text{ch}} = 0.12m_0$) [18], their difference in E_0 is not significant because E_0 is weakly dependent on m_{ch} [see (9)]. Using (9), we have carried out a detailed calculation and found that the difference in the minimum energy between L- and

X-valleys is still larger than $5kT$ under the F_S near the onset of threshold. Therefore, the impact of X-valley is negligible in this paper. As to the Γ -valley, its impact is even smaller than that of the X-valley because of small m_{ch} ($0.062m_0$ [18]).

IV. CONCLUSION

We have proposed a closed-form model of the DS for Ge MOSFETs with high- k gate dielectrics. This model shows accurate dependences on barrier height, surface electric field, and quantization effective mass of the channel and gate dielectric. Our model predicts that the DS decreases with reverse substrate bias and increasing channel doping. Our model can be also used for devices with a steep retrograde doping profile. This physically accurate model will be crucial to the prediction of the SS and the electrostatic integrity of advanced Ge devices.

REFERENCES

- [1] S. Takagi, T. Irisawa, T. Tezuka, T. Numata, S. Nakyharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, "Carrier-transport-enhanced channel CMOS for improved power consumption and performance," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 21–39, Jan. 2008.
- [2] T. Skotnicki, C. Fenouillet-Beranger, C. Gallon, F. Buf, S. Monfray, F. Payet, A. Pouydebasque, M. Szczap, A. Farcy, F. Arnaud, S. Clerc, M. Sellier, A. Cathignol, J.-P. Schoellkopf, E. Perea, R. Ferrant, and H. Mingam, "Innovative materials, devices, and CMOS technologies for low-power mobile multimedia," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 96–130, Jan. 2008.
- [3] [Online]. Available: <http://www.itrs.net/Links/2007ITRS/LinkedFiles/PIDS/MASTAR5/MASTARDownload.htm>
- [4] A. Pacelli, A. S. Spinelli, and L. M. Perron, "Carrier quantization at flat bands in MOS devices," *IEEE Trans. Electron Devices*, vol. 46, no. 2, pp. 383–387, Feb. 1999.
- [5] T. Ezaki, P. Werner, and M. Hane, "Self-consistent quantum mechanical Monte Carlo MOSFET device simulation," *J. Comput. Electron.*, vol. 2, no. 4, pp. 97–103, Dec. 2003.
- [6] Y. Omura, H. Konish, and S. Sato, "Quantum-mechanical suppression and enhancement of SCEs in ultrathin SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 677–684, Apr. 2006.
- [7] T. Skotnicki and F. Boeuf, "How can high mobility channel material boost or degrade performance in advanced CMOS," in *VLSI Symp. Tech. Dig.*, 2010, pp. 153–154.
- [8] Y.-S. Wu and P. Su, "Detailed study of 'dark space' and electrostatic integrity for Ge MOSFETs with high- k dielectric using analytical solution of Schrödinger equation," in *Proc. Silicon Nanoelectron. Workshop*, 2011, pp. 9–10.
- [9] International Technology Roadmap for Semiconductors. [Online]. Available: <http://www.itrs.net/>
- [10] F. Stern, "Self-consistent results for n-type Si inversion layers," *Phys. Rev. B*, vol. 5, no. 12, pp. 4891–4899, Jun. 1972.
- [11] F. Li, S. Mudanai, L. F. Register, and S. K. Banerjee, "A physically based compact gate $C-V$ model for ultrathin ($\text{EOT} \sim 1 \text{ nm}$ and below) gate dielectric MOS devices," *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1148–1158, Jun. 2005.
- [12] M. Shams, K. M. Habib, Q. Khosru, A. Zainuddin, and A. Hanque, "On the physically based compact gate $C-V$ model for ultrathin gate dielectric MOS devices using the modified airy function approximation," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2566–2569, Sep. 2007.
- [13] *ATLAS User's Manual*, SILVACO, Santa Clara, CA, 2008.
- [14] R. Shankar, *Principles of Quantum Mechanics*. New York: Plenum, 1994.
- [15] Y.-C. Yeo, T.-J. King, and C. Hu, "Direct tunneling leakage current and scalability of alternative gate dielectrics," *Appl. Phys. Lett.*, vol. 81, no. 11, pp. 2091–2093, Sep. 2002.
- [16] F. Stern and W. E. Howard, "Properties of semiconductor surface inversion layers in the electric quantum limit," *Phys. Rev.*, vol. 163, no. 3, pp. 816–835, Nov. 1967.

- [17] A. Pouydebasque, C. Charbuillet, R. Gwoziecki, and T. Skotnicki, "Refinement of the subthreshold slope modeling for advanced bulk CMOS devices," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2723–2729, Oct. 2007.
- [18] S. E. Laux, "A simulation study of the switching times of 22- and 17-nm gate-length SOI nFETs on high mobility substrates and Si," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2304–2320, Sep. 2007.



Yu-Sheng Wu (S'09) received the B.S. and M.S. degrees in electronics engineering in 2004 and 2006, respectively, from National Chiao Tung University, Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree at the Institute of Electronics.

His current research interests include design and modeling of advanced CMOS devices.



Pin Su (S'98–M'02) received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, and the Ph.D. degree from the University of California, Berkeley.

From 1997 to 2003, he conducted his doctoral and postdoctoral research in silicon-on-insulator (SOI) devices at Berkeley. He was also one of the major contributors to the unified BSIMSOI model, the first industrial standard SOI MOSFET model for circuit design. Since August 2003, he has been with the

Department of Electronics Engineering, National Chiao Tung University, where he is currently a Full Professor. He is the author or coauthor of more than 130 research papers in refereed journals and international conference proceedings in his areas of interest. His research interests include silicon-based nanoelectronics, modeling and design for exploratory CMOS and low-power memory devices, and device/circuit interaction and cooptimization in nanoscale CMOS.