Investigation of Temperature-Dependent High-Frequency Noise Characteristics for Deep-Submicrometer Bulk and SOI MOSFETs

Sheng-Chun Wang, Pin Su, *Member, IEEE*, Kun-Ming Chen, Bo-Yuan Chen, and Guo-Wei Huang, *Member, IEEE*

***Abstract*—The temperature dependence of high-frequency noise characteristics for deep-submicrometer bulk and silicon-on-insulator (SOI) MOSFETs has been experimentally examined in this paper. With the downscaling of the channel length, our paper indicates that the power spectral density of the channel noise (S_{id}) of the bulk MOSFET becomes less sensitive to temperature due to the smaller degradation of the channel conductance at zero drain bias g_{d0} as temperature rises. We also show that the SOI-specific floating-body and self-heating effects would result in higher white-noise gamma factor. Finally, for both the bulk and SOI MOSFETs, since transconductance g_m significantly decreases as temperature increases, their minimum noise figure $\mathrm{NF}_{\min}$ and equivalent noise resistance R_n would degrade with increasing temperature.**

***Index Terms*—High frequency, MOSFET, noise, temperature dependence, van der Ziel's model.**

I. Introduction

The noise performance of RF MOSFETs is critical to high-frequency applications, particularly to the design of low noise amplifiers, resulting in a need for the accurate noise modeling [1]. It is also well known that both small-signal circuit parameters and noise sources play important roles in the high-frequency noise modeling. There have been many studies on the high-frequency noise characterization and modeling for bulk and silicon-on-insulator (SOI) MOSFETs [1]–[9], and the temperature dependence of their small-signal performances has been also widely discussed [10]–[12]. In particular, Pascht *et al.* have conducted the temperature noise modeling for MOSFETs using the small-signal equivalent circuit with channel noise source [2]. However, the temperature dependences of the channel noise and the four noise parameters have not been presented and discussed. Although the temperature dependences of the channel noise, the induced gate noise, and their cross-correlation noise for a medium-long channel device $(L = 0.36\ \mu\mathrm{m})$ have been investigated in [13], whether the downscaling of channel length will impact the temperature dependence of high-frequency noise behaviors is rarely known and merits further investigation.

In this paper, with emphasis on the impact of channel-length scaling, we experimentally examine the temperature dependence of the power spectral density (PSD) of the channel noise (S_{id}) for both the RF bulk and SOI MOSFETs. In addition, the applicability of the popular van der Ziel model is also verified at different temperatures. Along with the extracted small-signal parameters and white-noise gamma factor, the temperature-dependent minimum noise figure $\mathrm{NF}_{\min}$ and equivalent noise resistance R_n can be also well described.

Manuscript received July 3, 2011; revised October 12, 2011 and November 15, 2011; accepted November 15, 2011. Date of publication January 6, 2012; date of current version February 23, 2012. This work was supported in part by the National Science Council of Taiwan. The review of this paper was arranged by Editor R. Venkatasubramanian.

S.-C. Wang was with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan. He is now with the National Nano Device Laboratories, Hsinchu 300, Taiwan (e-mail: scwang@ndl.narl.org.tw).

P. Su is with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: pinsu@faculty.nctu.edu.tw).

K.-M. Chen and B.-Y. Chen are with the National Nano Device Laboratories, Hsinchu 300, Taiwan.

G.-W. Huang is with the National Nano Device Laboratories, Hsinchu 300, Taiwan, and also with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2177664

II. Devices and Experiments

The RF MOSFETs used in this paper were fabricated using United Microelectronics Corporation (UMC) 0.13-μm bulk and SOI technologies, respectively. All the transistor's finger length, finger number, and group number are fixed to 3.6 μm, 16, and 2, respectively. The SOI MOSFETs are partially depleted, and their thicknesses for gate oxide, SOI layer, and buried oxide are 1.4, 40, and 200 nm, respectively.

The noise parameters of the device up to 10 GHz under different temperatures were measured using the ATN NP5B noise parameter measurement system. The pads and series parasitics were de-embedded to obtain the intrinsic-noise parameters. Then, the intrinsic-noise current sources can be extracted by following the approach presented in [3], which is based on the noise matrix manipulation derived from the two-port noise theorem.

III. High-Frequency Noise Characterization for Bulk MOSFETs

The van der Ziel model widely adopted to characterize the PSDs for the channel noise (S_{id}) can be expressed as follows [7], [14]:

$$S_{\mathrm{id}} = \gamma 4 k_B T g_{d0} \tag{1}$$

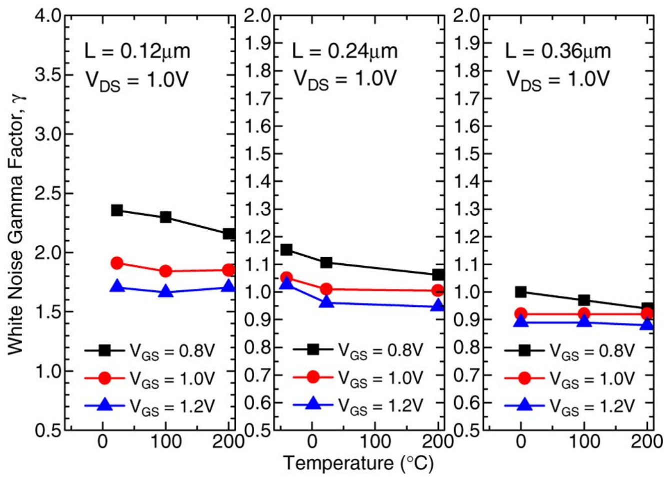


Fig. 1. Temperature dependence of γ for bulk devices with different channel lengths.

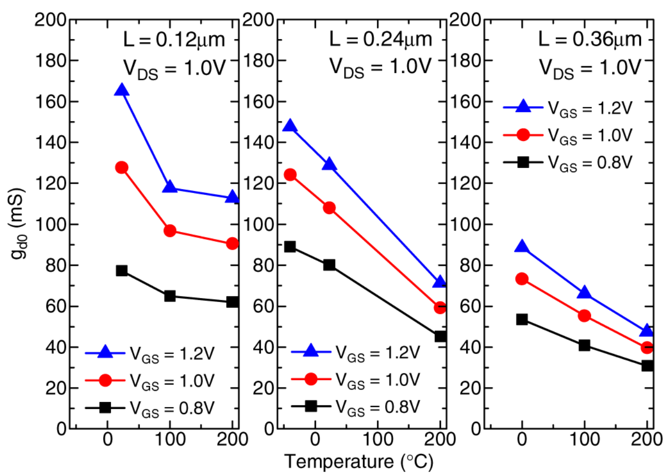


Fig. 2. Temperature dependence of g_{d0} for bulk devices with different channel lengths.

where γ is the white-noise gamma factor, g_{d0} is the channel conductance at zero drain bias, $k_B \approx 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, and T is the ambient temperature in Kelvin. Note that, as compared with the channel noise, since the other two noise sources (the induced gate noise S_{ig} and the correlation noise between them, i.e., S_{igd}) have been shown to play an insignificant role in determining the high-frequency noise behaviors for devices downscaled into/beyond the deep-submicrometer regime [15], we will focus our studies on the channel noise source only.

Fig. 1 shows the temperature dependence of the white-noise gamma factor γ for devices with different channel lengths. One can see that the temperature dependence is weak even for $L = 0.12$ μm device biased at high V_{GS}. This implies that the temperature dependence of g_{d0} is still the major factor determining the temperature dependence of the channel noise S_{id}, as suggested by (1). For $L = 0.12$ μm device, since g_{d0} does not decrease with temperature as much as that for both $L = 0.24$ μm and $L = 0.36$ μm devices, as shown in Fig. 2, instead of decreasing with temperature, the channel noise relatively remains constant over the whole temperature range, as shown in Fig. 3. $\mathrm{NF}_{\min}$ and R_n are two important figures of merit used to judge the noise performance of a device, and they can be respectively written as [15], [16]

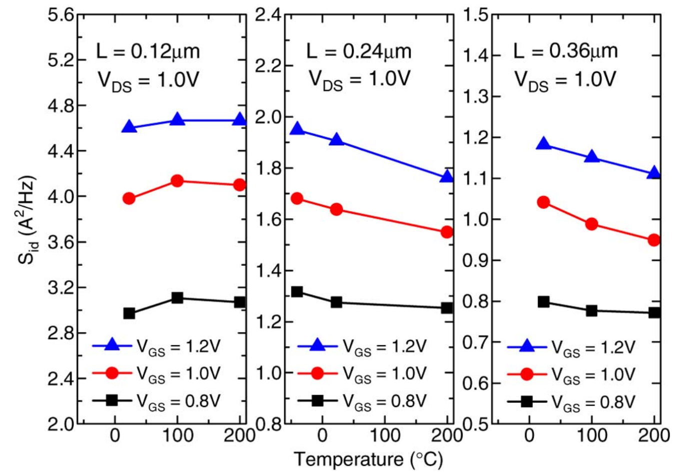


Fig. 3. Temperature dependence of S_{id} for bulk devices with different channel lengths.

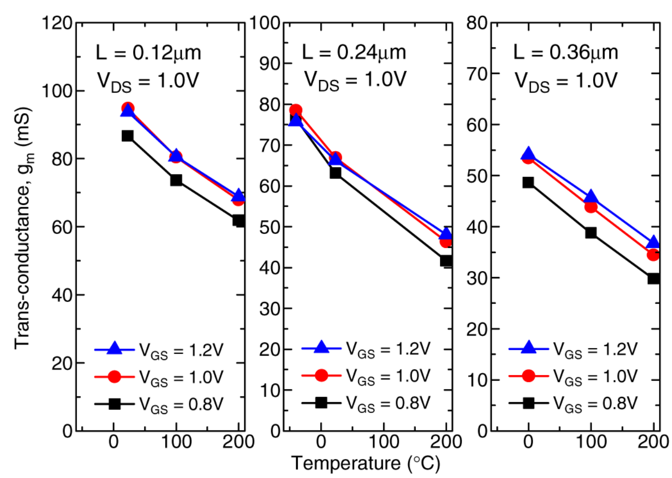


Fig. 4. Temperature dependence of g_m for bulk devices with different channel lengths.

$$\mathrm{NF}_{\min} \approx 1 + \frac{2}{g_m^2}\sqrt{R_g \frac{S_{\mathrm{id}}}{4kT_0}} \times \left\{ \omega C_{\mathrm{gg}} g_m \sqrt{\frac{T}{T_0}} + \omega^2 C_{\mathrm{gg}}^2 \sqrt{R_g \frac{S_{\mathrm{id}}}{4kT_0}} \right\} \tag{2}$$

$$R_n \approx \frac{T}{T_0} R_g + \frac{S_{\mathrm{id}}}{4k_B T_0 g_m^2}. \tag{3}$$

Note that, in the aforementioned derivation, we have neglected the contribution from S_{ig} and S_{igd}.

From (2) and (3), we can see that, except S_{id}, transconductance g_m would play an important role in determining both intrinsic $\mathrm{NF}_{\min}$ and R_n. The temperature dependence of g_m for devices with different channel lengths is shown in Fig. 4. It suggests that g_m decreases with temperature at a rate larger than that for S_{id} (refer to Fig. 2). Therefore, according to (2) and (3), both $\mathrm{NF}_{\min}$ and R_n would tend to become larger with increasing temperature as shown in Fig. 5(a) and (b), respectively.

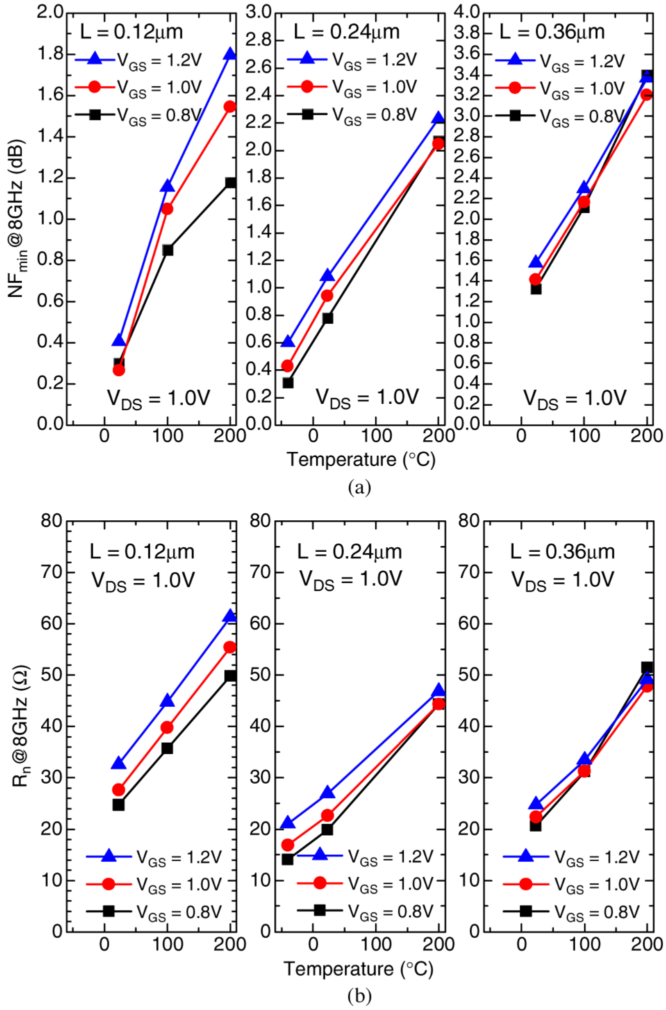


Fig. 5. Temperature dependence of (a) $\mathrm{NF}_{\min}$ and (b) R_n for bulk devices with different channel lengths.

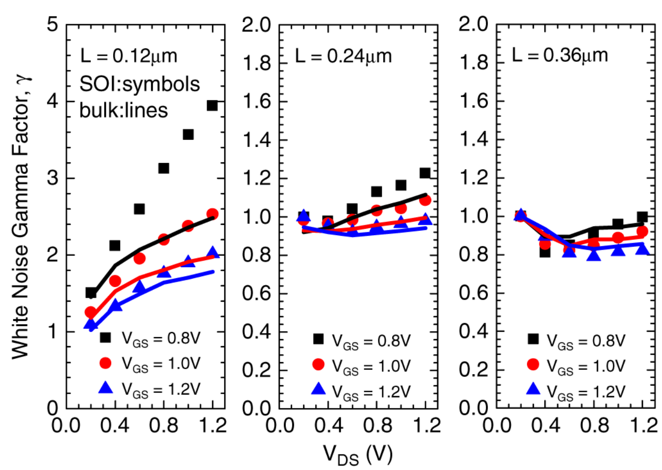


Fig. 6. Noise factor γ for both (symbols) SOI and (lines) bulk devices with different channel lengths.

IV. High-Frequency Noise Characterization for SOI MOSFETs

Fig. 6 shows the white-noise gamma factor γ for both the bulk and SOI devices. It shows that, in the medium-long channel devices ($L = 0.36\ \mu$m) [13], γ seems to remain the same for both SOI and bulk devices. However, the SOI devices would have an increasing γ as the channel length shrinks. Two mechanisms may contribute to this phenomenon, i.e., the floating-body effect (FBE) and the self-heating effect (SHE) [17]. Due to the floating-body structure of the SOI n-channel MOSFET, there is a potential barrier between the source and the body region. Therefore, the holes generated by impact ionization [18] at a high-drain-bias condition can be easily trapped in the body volume, and the body potential can rise [17], [19]. The elevated body potential would, in turn, lower the effective threshold voltage and accordingly increase the gate overdrive voltage $V_{\mathrm{GT}} = V_{GS} - V_T$. Then, a more conductive channel and, hence, larger S_{id} can be expected. According to the van der Ziel model [see (1)], a larger γ can be obtained using lower g_{d0} extracted at zero drain bias, where the FBE is negligible. Aside from that, due to the more substantial impact ionization current induced by the larger maximum channel electric field [18] at lower V_{GS} ($\approx V_{\mathrm{dd}}/2$), the FBE would have a larger impact on the excess noise at lower V_{GS}.

On the other hand, as V_{GS} increases, the dc power and, therefore, the temperature of the SOI MOSFET increases due to the so-called SHE [18], [20]. This effect is caused by poor thermal conductivity of the buried oxide, which is about two orders of magnitude less than that of the silicon [18], [20], and the lattice temperature would play an important role in determining the SOI MOSFET noise characteristics [8]. Aside from that, the noise arising from the neutral-body resistance should be enhanced by the elevated lattice temperature, and its contribution to the channel noise S_{id} may have to be considered. However, since the effective mobility and, hence, the channel conductance should be accordingly decreased, the excess noise caused by the SHE would be partly counterbalanced by the reduction of the channel conductance. This captures the slight increase in γ at high V_{GS} [see (1)]. It is worth noting that, since the SHE may reduce the body potential by inducing more diode leakage [17], the excess noise caused by the FBE at high V_{GS} could be further alleviated.

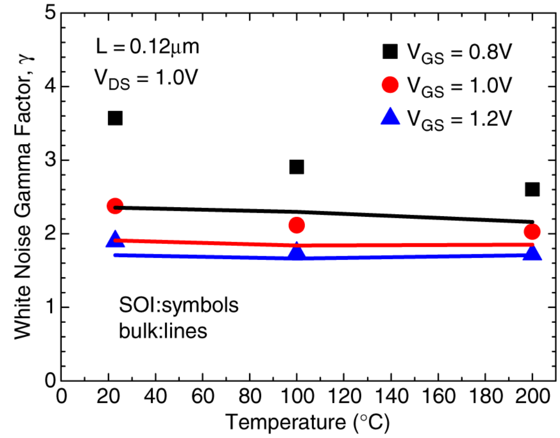


Fig. 7. Temperature dependence of white-noise gamma factor γ for both (symbols) SOI and (lines) bulk devices.

Fig. 7 shows the temperature dependence of γ for both SOI and bulk devices. Since the FBE can be eliminated at high

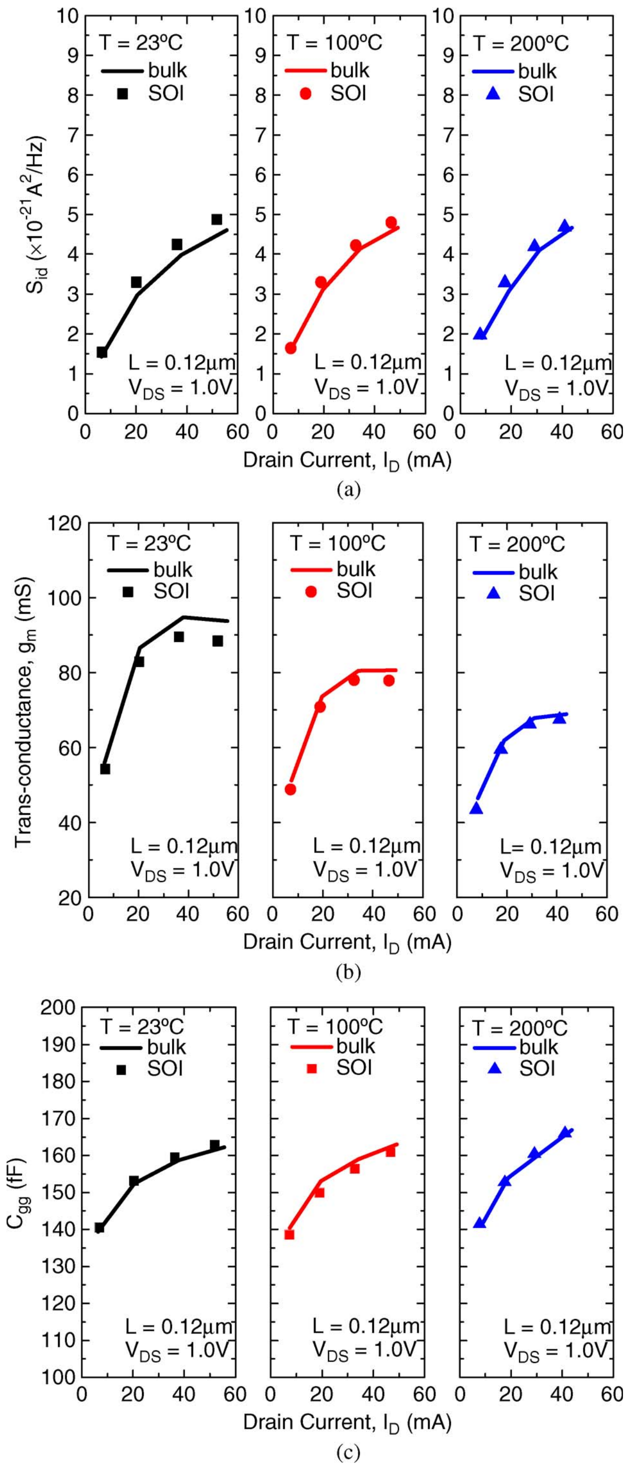


Fig. 8. Comparison of (a) $S_{\rm id}$, (b) g_m, and (c) $C_{\rm gg}$ versus drain current between the bulk and SOI MOSFETs ($V_{DS} = 1.0$ V).

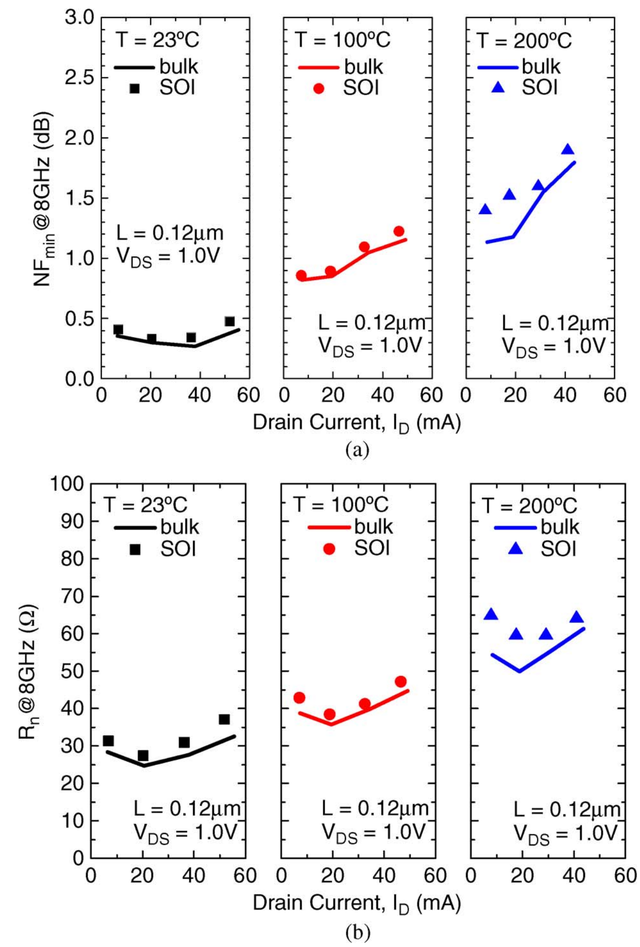


Fig. 9. Comparison of (a) $\mathrm{NF}_{\min}$, and (b) R_n versus drain current between the bulk and SOI MOSFETs ($V_{DS} = 1.0$ V).

TABLE I
EXTRACTED R_s, R_d, AND R_g FOR BOTH THE SOI AND BULK DEVICES. ($L = 0.12\ \mu$m)

	SOI			BULK		
	$R_s(\Omega)$	$R_d(\Omega)$	$R_g(\Omega)$	$R_s(\Omega)$	$R_d(\Omega)$	$R_g(\Omega)$
T = 23 ℃	0.1	1.7	1.9	0.1	1.5	2.0
T = 100 ℃	0.1	1.8	2.2	0.1	1.8	2.2
T = 200 ℃	0.1	2.2	2.3	0.1	2.0	2.5

temperature [19], the channel suffering less FBE would have decreasing γ with increasing temperature. This is particularly obvious at low V_{GS}, where the FBE dominates the excess channel noise behavior. For bulk devices, since they suffer from neither the FBE nor the SHE, they have similar γ over the whole temperature region.

Finally, we compare $\mathrm{NF}_{\min}$ and R_n for the SOI and bulk devices for a given dc power consumption. Fig. 8(a) and (b) show the comparison of $S_{\rm id}$ and g_m, respectively, versus current for a given drain voltage $V_{DS} = 1.0$ V. Because the SOI device has larger $S_{\rm id}$ and lower g_m than the bulk counterparts in our experiments, referring to (2) and (3), it is expected that it would have worse $\mathrm{NF}_{\min}$ and R_n, as shown in Fig. 9(a) and (b), respectively. It is worth noting that the extrinsic parameters, such as gate capacitance and terminal resistances, would not significantly contribute to the deviations, since both devices have been checked to have similar $C_{\rm gg}$ [see Fig. 8(c)] and terminal resistances (shown in Table I) for each temperature.

It should be noted that we have neglected the neutral-body effect on the RF characterization in this experiment. This is because [21] has demonstrated the insignificant neutral-body effect on the RF small-signal characteristics of

SOI MOSFETs except the output admittance. Aside from that, the body transconductance and drain leakage current have been presented to have significant effect mostly on the low-frequency-noise behavior due to its low-pass nature [22]. Note that, at the very high frequency, the neutral-body resistance R_b would be equivalently parallel to the channel resistance and can contribute to the output noise current associated with the drain terminal. However, its thermal noise contribution $4k_BT/R_b$ is at the level of about 1.66×10^{-22} A^2/Hz for $R_b \approx 100\ \Omega$ and can be neglected compared with the extracted S_{id} shown in Fig. 8(a).

V. Conclusion

We have comprehensively investigated the temperature dependence of S_{id} for both the deep-submicrometer bulk and SOI MOSFETs. For bulk MOSFETs, since the decreasing rate of g_{d0} with temperature is lowered as the channel length shrinks, S_{id} would relatively remain constant over a large temperature range.

For SOI MOSFETs, the FBE and the SHE may contribute to the higher white-noise gamma factors, as compared with the bulk counterparts. The FBE dominates at the low V_{GS} regime and can be suppressed by elevating the temperature. At the high V_{GS} regime, where the SHE is significant, the excess noise contribution from the elevated lattice temperature would be partly counterbalanced by the lowered channel conductance. Therefore, as compared with the FBE, its contribution to S_{id} may be less significant.

Aside from that, since the transconductance decreases with temperature at a rate higher than that for S_{id}, both $\mathrm{NF}_{\min}$ and R_n would accordingly increase. Our experiment also shows that the SOI device has worse $\mathrm{NF}_{\min}$ and R_n due to the larger S_{id} and lower g_m than the bulk counterpart.

Acknowledgment

The authors would like to thank UMC for providing the devices used in this paper.

References

[1] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia, “Noise modeling for RF CMOS circuit simulation,” *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 618–632, Mar. 2003.

[2] A. Pascht, M. Grozing, D. Wiegner, and M. Berroth, “Small-signal and temperature noise model for MOSFETs,” *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 8, pp. 1927–1934, Aug. 2002.

[3] C.-H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, “Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements,” *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2884–2892, Dec. 2001.

[4] K. Han, H. Shin, and K. Lee, “Analytical drain thermal noise current model valid for deep submicron MOSFETs,” *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 261–269, Feb. 2004.

[5] K. Han, J. Gil, S.-S. Song, J. Han, H. Shin, C.-K. Kim, and K. Lee, “Complete high frequency thermal noise modeling of short-channel MOSFETs and design of 5.2 GHz low noise amplifier,” *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 726–735, Mar. 2005.

[6] M. J. Deen, C.-H. Chen, S. Asgaran, G. A. Rezvani, J. Tao, and Y. Kiyota, “High-frequency noise of modern MOSFETs: Compact modeling and measurement issues,” *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2062–2081, Sep. 2006.

[7] A. F. Tong, W. M. Lim, K. S. Yeo, C. B. Sia, and W. C. Zhou, “A scalable RFCMOS noise model,” *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1009–1019, May 2009.

[8] W. Jin, P. C. H. Chan, and J. Lau, “A physical thermal noise model for SOI MOSFET,” *IEEE Trans. Electron Devices*, vol. 47, no. 4, pp. 768–773, Apr. 2000.

[9] A. O. Adan, M. Koyanagi, and M. Fukumi, “Physical model of noise mechanisms in SOI and bulk-silicon MOSFETs for RF applications,” *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 872–880, Sep. 2008.

[10] S. M. Nam, B. J. Lee, S. H. Hong, C. G. Yu, J. T. Park, and H. K. Yu, “Experimental investigation of temperature dependent RF performances of RF-CMOS devices,” in *Proc. 6th ICVC*, 1999, pp. 174–177.

[11] Y. S. Lin, “Temperature dependence of the power gain and scattering parameters s11 and s22 of an RF nMOSFET with advanced RF-CMOS technology,” *Microw. Opt. Technol. Lett.*, vol. 44, no. 2, pp. 180–185, Jan. 20, 2005.

[12] M. Emam, D. Vanhoenacker-Janvier, K. Anil, J. Ida, and J.-P. Raskin, “High temperature RF behavior of SOI MOSFETs for low-power low-voltage applications,” in *Proc. IEEE Int. SOI Conf.*, 2008, pp. 139–140.

[13] S.-C. Wang, P. Su, K.-M. Chen, C.-T. Lin, V. Liang, and G.-W. Huang, “Temperature dependence of high frequency noise behaviors for RF MOSFETs,” *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 8, pp. 530–532, Aug. 2008.

[14] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.

[15] S.-C. Wang, P. Su, K.-M. Chen, K.-H. Liao, B.-Y. Chen, S.-Y. Huang, C.-C. Hung, and G.-W. Huang, “Comprehensive noise characterization and modeling for 65-nm MOSFETs for millimeter-wave applications,” *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 4, pp. 740–746, Apr. 2010.

[16] J. Jeon, I. Song, I. M. Kang, Y. Yun, B.-G. Park, J. D. Lee, and H. Shin, “A new noise parameter model of short-channel MOSFETs,” in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2007, pp. 639–642.

[17] P. Su, S. K. H. Fung, S. Tang, F. Assaderaghi, and C. Hu, “BSIMPD: A partial-depletion SOI MOSFET model for deep-submicron CMOS designs,” in *Proc. IEEE Custom Integr. Circuits Conf.*, 2000, pp. 197–200.

[18] P. Su, K.-I. Goto, T. Sugii, and C. Hu, “Enhanced substrate current in SOI MOSFETs,” *IEEE Electron Device Lett.*, vol. 23, no. 5, pp. 282–284, May 2002.

[19] J. G. Fossum, M. Pelella, and S. Krishnan, “Scalable PD/SOI CMOS with floating bodies,” *IEEE Electron Device Lett.*, vol. 19, no. 11, pp. 414–416, Nov. 1998.

[20] L. Su, J. Chung, D. Antoniadis, K. Goodson, and M. Flik, “Measurement and modeling of self-heating in SOI NMOSFETs,” *IEEE Trans. Electron Devices*, vol. 41, no. 1, pp. 69–75, Jan. 1994.

[21] S.-C. Wang, P. Su, K.-M. Chen, C.-T. Lin, V. Liang, and G.-W. Huang, “Radio-frequency silicon-on-insulator modeling considering the neutral-body effect,” *Jpn. J. Appl. Phys.*, vol. 47, no. 4, pp. 2087–2091, Apr. 2008.

[22] W. Jin, P. C. H. Chan, S. K. H. Fung, and P. K. Ko, “Shot-noise-induced excess low-frequency noise in floating-body partially depleted SOI MOSFETs,” *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1180–1185, Jun. 1999.

Sheng-Chun Wang received the B.S. and M.S. degrees in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, in 1999 and 2001, respectively, and the Ph.D. degree in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 2011.

In 2001, he was an Assistant Researcher with the National Nano Device Laboratories, Hsinchu, where he has been an Associate Researcher since 2011. His current research interests focus on the small-signal and noise characterization and modeling for radio-frequency complementary metal–oxide–semiconductor devices.

Pin Su (S'98–M'02) received the B.S. and M.S. degrees in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, and the Ph.D. degree from the University of California at Berkeley, Berkeley.

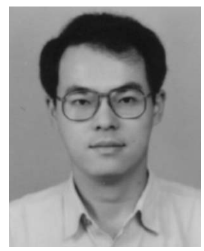
From 1997 to 2003, he conducted his doctoral and postdoctoral research in silicon-on-insulator (SOI) devices with the University of California at Berkeley. He was also one of the major contributors to the unified BSIMSOI model, the first industrial standard SOI metal–oxide–semiconductor field-effect transistor model for circuit design. Since August 2003, he has been with the Department of Electronics Engineering, National Chiao Tung University, where he is currently a Full Professor. He has authored or coauthored over 130 research papers in refereed journals and international conference proceedings in these areas. His research interests include silicon-based nanoelectronics, modeling and design for exploratory CMOS devices, and device/circuit interaction and co-optimization in nano-CMOS.

Kun-Ming Chen received the M.S. degree and the Ph.D. degree in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1996 and 2000, respectively.

In 2000, he was an Associate Researcher with the National Nano Device Laboratories, Hsinchu, where he has been a Researcher since 2007. He was engaged in the research on the microwave device process and characterization.

Bo-Yuan Chen was born in Miaoli, Taiwan, in 1980. He received the M.S. degree in materials science and engineering from the National Dong Hwa University, Hualien, Taiwan, in 2006.

Since 2006, he has been an Assistant Researcher with the National Nano Device Laboratories, Hsinchu, Taiwan. He was engaged in research on III–V compound semiconductors and radio-frequency device characterization.



Guo-Wei Huang (S'94–M'97) was born in Taipei, Taiwan, in 1969. He received the B.S. degree and the Ph.D. degree in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1991 and 1997, respectively.

Since 1997, he has been with the National Nano Device Laboratories, Hsinchu, Taiwan, where he is currently a Researcher and the Manager of the high-frequency technology division. Since August 2011, he has been a joint Professor with the Department of Electronics Engineering, National Chiao Tung University. His current research interests focus on characterization and modeling techniques of high-frequency devices, and characterization and verification of radio-frequency/monolithic-microwave integrated circuits.