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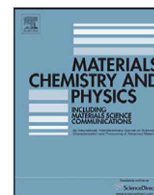

Enhanced performance and reliability of NILC-TFTs using FSG buffer layer

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ABSTRACT

A new manufacturing method for Ni-metal-induced lateral crystallization thin film transistors (NILC-TFTs) using fluorine-silicate-glass (FSG) was proposed. In FSG-TFTs, fluorine ion was implanted into the buffer oxide layer to form FSG before NILC processes. It was found FSG-TFTs exhibit high field-effect mobility, low threshold voltage, low subthreshold slope, high ON/OFF current ratio, low trap state density, low interface trap state density, and good reliability compared with typical NILC-TFTs.

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1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) had been widely used in active-matrix organic light emitting diode (AMOLED) because they exhibit good electrical properties and can be integrated in peripheral circuits on inexpensive glass substrates [1]. Since poly-Si TFTs require glass substrates, intensive studies have been carried out to lower the crystallization temperature of amorphous silicon (a-Si) films. Ni-metal-induced lateral crystallization (NILC) was one of the effective methods that could crystallize at a temperature below 600 °C [2,3]. Unfortunately, poly-Si/oxide interfaces and grain boundaries trap Ni and $NiSi_2$, which increases trap state density, shifts threshold voltage, and lowers field-effect mobility [4,5]. Recently, fluorine ion implantation was employed to improve the electrical performance of TFTs [6,7]. It was found that fluorine atoms effectively minimize the trap state density and improve NILC-TFTs' electrical properties and reliabilities [8].

In early research, fluorine ion was also used to improve TFT performance [9–11]. To avoid implantation damage, fluorine ion was implanted through a pad oxide before into active layer [9,10]. If fluorine ion was implanted directly into active layer (without a pad oxide), the implantation may damage the channel (poly-Si surfaces) and lower fluorine passivation effects [11].

In this paper, fluorinated-silicate-glass (FSG) process was developed to reduce this implantation damage and improve the performance of NILC-TFTs. The TFT devices with FSG buffer layer not only can prevent the implant damage also save a pad oxide fabrication.

2. Experiment

The NILC-TFTs with FSG layer (FSG-TFTs) fabrication process began with capping Si wafers with 500-nm-thick wet thermal oxide. To fabricate FSG-TFTs, the fluorine ion was implanted into the thermal oxide layer to form fluorine-silicate-glass (FSG). The projection range of fluorine ion was set at under the top surface of the FSG layer and the accelerating energy was 30 keV.

To investigate the effect of fluorine content in FSG layer on the performances of TFTs, two types of FSG-TFTs were fabricated. They were denoted as F2E12-TFT (2×10^{12} cm^{-2} dosages) and F2E15-TFT (2×10^{15} cm^{-2} dosages). Next, a 100-nm-thick undoped amorphous silicon (a-Si) layer was deposited by low pressure chemical vapor deposition (LPCVD) at 550 °C. The 5-nm-thick line-patterned Ni was deposited on the a-Si, subsequently annealed at 530 °C for 48 h to form the NILC poly-Si film. After the crystallization of the a-Si, the active regions were defined by reactive ion etching (RIE). The 100-nm-thick TEOS oxide was deposited by plasma-enhanced CVD (PECVD) for gate oxide and 100-nm-thick poly-Si film was deposited by LPCVD for gate electrodes. P^+-ion was implanted at a dose of 5×15 cm^2 to form the source/drain and gate after defining the gate pattern. The activation of the source/drain regions was realized by the thermal furnace under N_2 ambient at 600 °C for 24 h.

For the purpose of comparison, the NILC-TFTs were also subjected to the same processes but without fluorine ion implantation.

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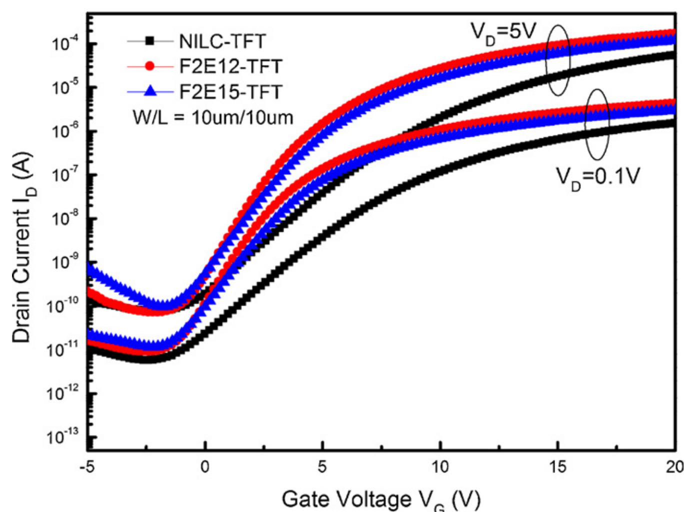

Fig. 1. I_D–V_G transfer characteristics of TFTs.

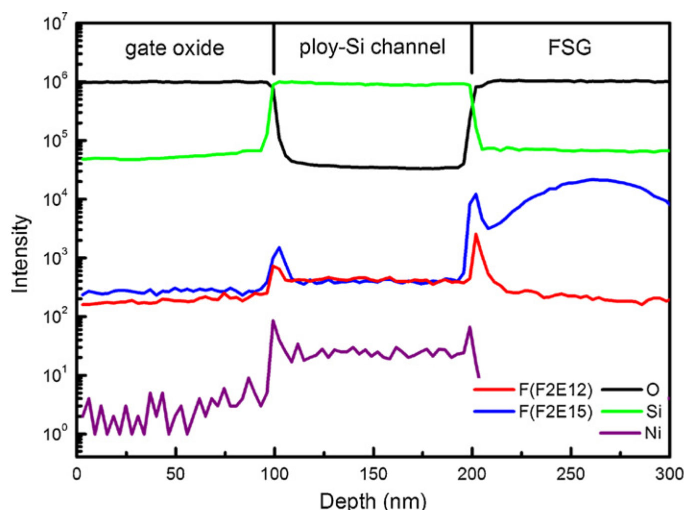

Fig. 2. SIMS depth profile of fluorine, oxygen, silicon and nickel the atoms of F2E12-TFT and F2E15-TFT.

3. Results and discussion

Fig. 1 illustrates the I_D–V_G transfer characteristics of TFTs (W/L = 10/10 μm) with and without FSG. The measured and extracted key device parameters were summarized in Table 1. It was found FSG-TFTs (F2E12-TFT and F2E15-TFT) exhibit high field-effect mobility (μ_{FE}), low threshold voltage (V_{TH}), low subthreshold slope (S.S.) and high ON/OFF current ratio (I_{ON}/I_{OFF}) compared with NILC-TFTs. This indicates the trap state density (N_T) was effectively reduced using FSG.

The trap state density of the TFTs was extracted using Levinson and Proano's method, which can estimate the N_T from the slope of the linear segment of $\ln[I_{DS}/(V_{GS} - V_{FB})]$ vs. $1/(V_{GS} - V_{FB})^2$ at low V_{DS} and high V_{GS}, where V_{FB} is defined as the gate voltage that yields the minimum drain current at V_{DS} = 0.1 [12,13]. As shown in Table 1, the trap state densities of F2E12-TFT and F2E15-TFT were less than those of NILC-TFTs.

In NILC poly-Si, there are two kinds of defects related to trap state density (N_T): (1) grain boundary defects and (2) Ni-related defects. These defects would degrade electric performance because they introduced dangling bonds and strain bonds [4,5]. Secondary-ion mass spectroscopy (SIMS) was used to study the distribution of Ni and F. Fig. 2 shows the depth profile of the F2E12 and F2E15 gate-oxide/poly-Si/buffer-oxide structure. High Ni and high F contents are both present at the poly-Si/buffer-oxide interface. This observation suggested that fluorine atoms have diffused to the interface/boundaries to terminate Ni-related trap states and boundary defects. As a result, the trap state density (N_T) was reduced, and electrical characteristics were improved [6–8]. This F diffusion behavior might be because most of the Ni-related defects (residues) were located at the interface between poly-Si and oxide. As a result, F atoms diffused to interface to passivate these defects, which including dangling bonds and strain bonds by forming strong Si—F bonds [8]. Besides, since the NILC poly-Si film is only 100 nm, F atoms have enough time to reach the interface during the subsequently procedures (including 600 °C, 24 h).

However, the performance of F2E15-TFT was poorer than that of F2E12-TFT, as shown in Fig. 1. This is because F content in the active layer was higher than F solubility ($[F]_{RT}$) in the Si at room temperature. As mentioned earlier, F ions were implanted into the thermal oxide layer. With the subsequently activation process (600 °C, 24 h), F atoms have enough time to diffuse to interface to passivate defects. At the same time, F content in the active layer reached F solubility $[F]_{600\,^\circ C}$, which is much higher than $[F]_{RT}$. As a result, when devices were cooled down to the room temperature, F content in the active layer was higher than the F solubility ($[F]_{RT}$).

This is consistent with our SIMS measurements. As shown in Fig. 2, the F content inside two FSG-TFTs films were almost the same except at interface areas. This is because in both case, F contents reached $[F]_{600\,^\circ C}$. Extra F atoms were trapped at interfaces, where most of Ni-related defects (residues) were. As a result, the excess F atoms in F2E15-TFT segregated and formed fluorine clusters at interfaces. These fluorine clusters would not passivate the trap states but increase the defects and then degrade the electrical performances [8,14]. As shown in Table 1, the N_T of F2E15-TFT was higher than that of F2E12-TFT.

As mentioned earlier, most Ni residues (Ni-related defects) were located at the Si/oxide interface (Fig. 2) and formed trap states. The interface trap state density (N_{it}) near the poly-Si/gate oxide interface could be calculated as:

$$N_{it} = \left[\left(\frac{\text{S.S.}}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{ox}}{q}\right)$$

where C_{ox} was gate oxide capacitance [15]. As shown in Fig. 3, N_{it} of FSG-TFTs was less than those of NILC-TFTs. Besides, N_{it} of TFTs increased with temperature. This increase implies that leakage current increases with the devices working temperature due to the thermal excited trapped carriers [16]. Compared with those of NILC-TFTs, the N_{it} degradation (thermal stability) of FSG-TFTs was improved by FSG processes. This was because of the passivation of dangling bonds and strain bonds at the poly-Si/oxide interface by fluorine atoms.

Table 1
Device characteristics of NILC-TFT, F2E12-TFT and F2E15-TFT.

	μ_{FE} (cm²/Vs)	V_{TH} (V)	S.S. (V/dec)	I_{ON}/I_{OFF} (10^6)	N_T (10^{12} cm^{-2})
NILC-TFT	55.1	6.12	2.13	0.56	4.61
F2E12-TFT	97.5	2.48	1.14	2.36	2.25
F2E15-TFT	79.4	3.00	1.41	1.22	3.23

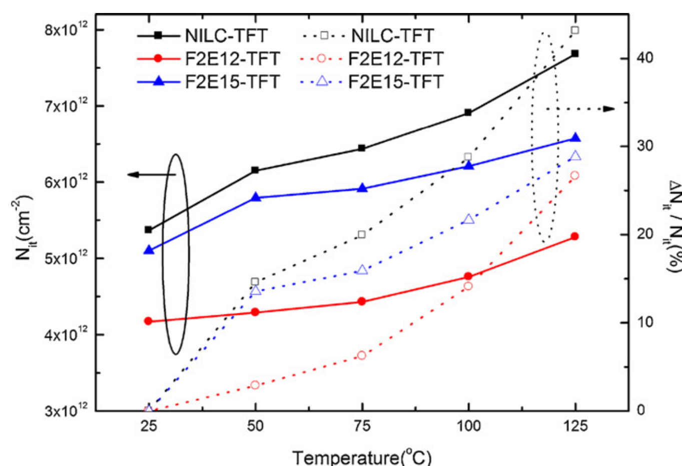

Fig. 3. The interface trap state density and their variation versus temperature for NILC-TFT, F2E12-TFT and F2E15-TFT.

The other important issue of poly-Si TFTs is their reliability, which was examined under hot-carrier stress. The DC stress condition was set gate voltage $V_{G,stress}$ at $V_G - V_{TH}$ = 10 V and drain voltage $V_{D,stress}$ at $I_D = 10^{-4}$ A. The stress time was 10,000 s. As shown in Figs. 4 and 5, the V_{TH} and the I_{ON} of TFTs were degraded. This was because when TFTs were under the DC stress operation, hot-carrier would impact into drain side and create broken bonds due to the weak Si-Si bonds and Si—H bonds. Those broken bonds or dangling bonds would increase the trap state density, leading to the degradation of electrical characteristics [17,18]. Compared with those of NILC-TFTs, the V_{TH} variation and I_{ON} degradations of FSG-TFTs were greatly improved. This was because the weaker Si—Si bonds and Si—H bonds in FSG-TFTs were replaced by the stronger Si—F bonds which appeared excellent electrical endurance against hot-carrier impact.

Although the electrical reliabilities were enhanced by fluorine-ion incorporating in poly-Si, it was also found the electrical degradation of F2E12-TFT was worse than that of F2E15-TFT, as shown in Figs. 4 and 5. On account of the F2E12-TFT has the highest μ_{FE}, the hot-carrier impact effects would be more serious. When TFT devices were under working, the electron will be accelerated by the applied drain electric field. The higher μ_{FE} implies that the less electron scattering while electron transferring from source to drain, so the degradation of electrical performances was greater due to the electron with higher energy [19].

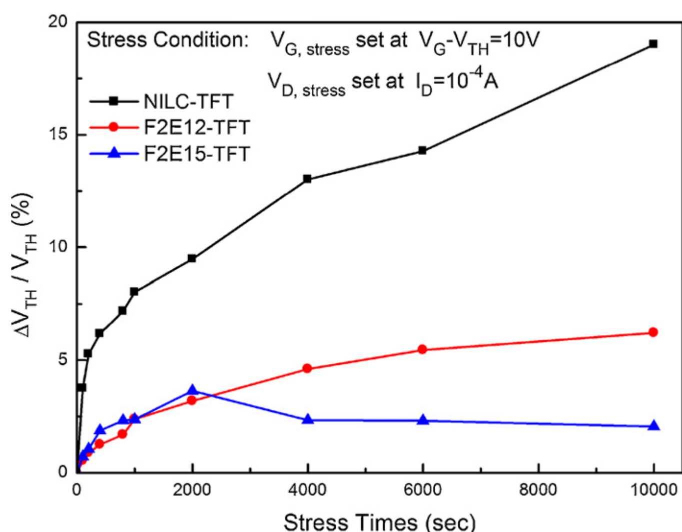

Fig. 4. Threshold voltage variation versus stress time for NILC-TFT, F2E12-TFT and F2E15-TFT.

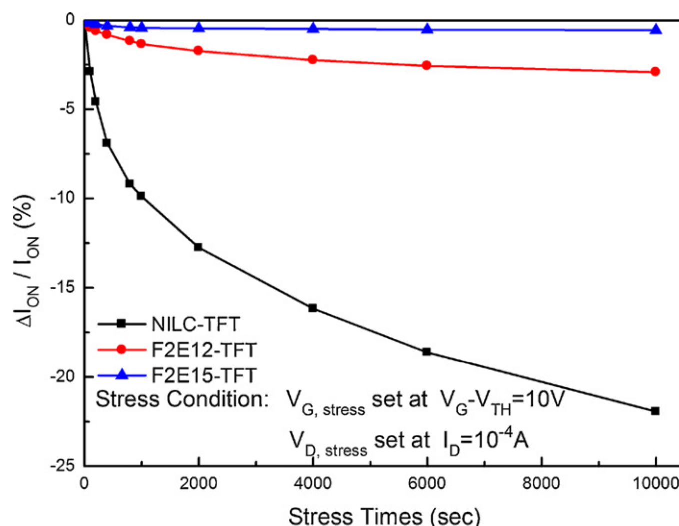

Fig. 5. ON-current degradation versus stress time for NILC-TFT, F2E12-TFT and F2E15-TFT.

4. Conclusion

An investigation of the effects of FSG buffer layer on the electrical characteristics and reliability of NILC-TFTs has led to the development of a simple, effective process for improving the NILC-TFTs electrical properties. This was because F atoms could passivate dangling bonds and strain bonds. It was also found that FSG process could greatly alleviate the threshold voltage and the ON-current degradations under hot-carrier stress. This was due to the weaker Si—H and Si—Si bonds were replaced by stronger Si—F bonds, thus leading to improved electrical reliability. However, the excess fluorine atoms would not passivate the trap states but increase the defects and then degrade the electrical performances.

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Appendix A. Supplementary data

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.matchemphys.2011.11.080.

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