A 0.6-V 30 GHz CMOS Quadrature VCO Using Microwave 1:1:1 Trifilar Transformer

Jin-Siang Syu, *Student Member, IEEE*, Hsi-Liang Lu, and Chinchun Meng, *Member, IEEE*

***Abstract*—A 30 GHz trifilar-transformer-coupled quadrature voltage-controlled oscillator (QVCO) is proposed in this letter using 0.13 μm CMOS technology. The trifilar transformer provides dc decoupling as well as ac mutual coupling from drain, gate, and source nodes. The mutual coupling increases the overall quality factor while the gate/drain-to-source coupling provides quadrature coupling. The proposed 1:1:1 trifilar transformer realization has lower ohmic loss than the conventional trifilar transformer realization and is especially suitable for high-frequency applications. As a result, the proposed 30 GHz QVCO has a -195 dBc/Hz figure of merit (FOM) and a maximum 41.6 dB sideband rejection (SBR) at a 0.6 V supply.**

***Index Terms*—Quadrature voltage-controlled oscillator (QVCO), sideband rejection (SBR), trifilar transformer.**

I. Introduction

A QUADRATURE signal generator is the key component in an RF transceiver, e.g., an I/Q downconverter, a single-sideband upconverter, or a sub-harmonic mixer. A quadrature voltage-controlled oscillator (QVCO) using two identical VCOs with quadrature-phase coupling is a popular method for high-frequency quadrature signal generation. Conventionally, a transistor-coupled QVCO includes parallel [1] and series QVCO structures [2], [3]. Unlike the parallel QVCO with a strong trade-off between the phase noise and phase accuracy, both top-series (TS) and bottom-series (BS) QVCO structures can lessen this trade-off. Further, the BS QVCO has better phase noise performance since the resonator phase shift (RPS), which is the phase angle between the current injected into the tank and the tank voltage, equals 0° while the RPS of the TS QVCO is typically 90° [4]. Unfortunately, this cascode configuration is unsuitable for a low-voltage operation. To replace the BS coupling transistors, a passive transformer had been utilized for the quadrature signal generation [5]. The transformer-coupled QVCO can be treated as a modified version of the BS QVCO with better voltage headroom and eliminates the flicker noise of the coupling devices.

In our previous work [6], a trifilar-transformer-coupled QVCO combining both gate-to-drain Q-enhanced coupling [3] and gate/drain-to-source quadrature-phase coupling [5] was first proposed, as indicated in Fig. 1(a), while the $L_d/L_g/L_s$ are 1.6/0.5/0.5 nH, $k_{gd}/k_{ds}/k_{gs}$ are 0.6/0.6/0.4 and $Q_{\max} = 12/9/9$ at f_{Qmax} of 6/13/13 GHz for drain/gate/source inductors, respectively. However, in a conventional trifilar transformer (with a turn ratio of 2:1:1), metal bending and metal crossing for a multi-turn inductor cause additional ohmic loss and degrade the quality factor of the inductor [7]. Further, the radius should be reduced to have proper inductance at high frequencies but the quality factor of the inductor is then degraded [7]. Thus, a newly proposed 1:1:1-turn-ratio layout in this letter is more suitable for high-frequency applications. A 30 GHz CMOS QVCO is thus demonstrated using the 1:1:1 trifilar transformers and achieves a figure of merit (FOM) of -195 dBc/Hz.

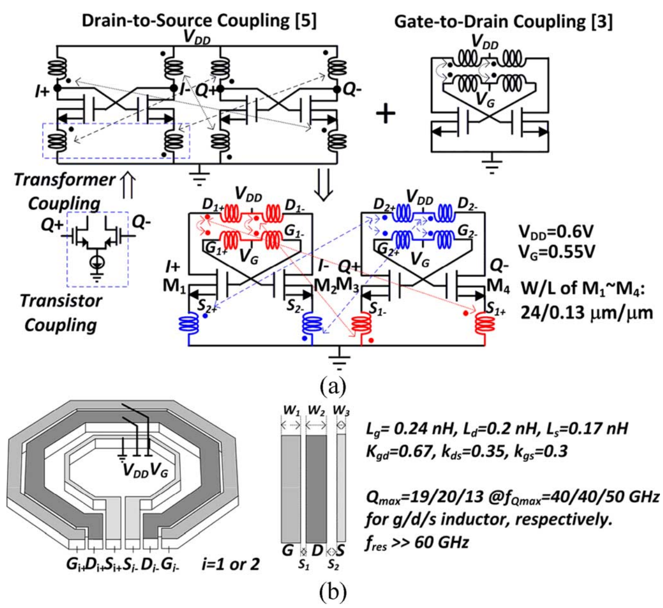

Fig. 1. (a) Schematic of the QVCO using microwave trifilar transformers (b) layout of the 1:1:1 trifilar transformer.

II. Circuit Design

The schematic of the main QVCO core is shown in Fig. 1(a), while Fig. 1(b) shows the layout of the 1:1:1 differential trifilar transformer. In Fig. 1, the $G_{i\pm}/D_{i\pm}/S_{i\pm}$ are the differential ports connected to the gate/drain/source nodes of the VCO core, respectively, where $i = 1$ or 2 for the two identical transformers. Note that, all the signal ports (drain, gate, and source) of the trifilar transformer are at the same side while the three dc bias (ac ground) are fed from the center-tapped nodes, located at the other side. Thus, the wire connections from the trifilar transformer to active devices can be minimized.

The phase noise and phase accuracy of the QVCO can be optimized by using different line width and line spacing for

Manuscript received August 10, 2011; revised October 16, 2011; accepted December 08, 2011. Date of publication January 24, 2012; date of current version February 15, 2012. This work was supported by the National Science Council of Taiwan under Contracts NSC 98-2221-E-009-033-MY3, NSC 99-2221-E-009-049-MY3, and NSC 98-2218-E-009-008-MY3, and by the Ministry of Education (MoE) Aim for the Top University (ATU) Program under Contract 95W803.

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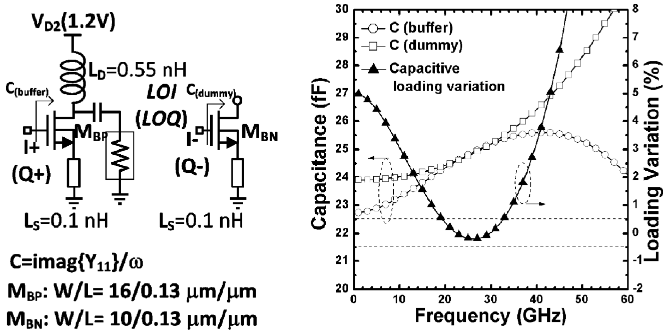
Digital Object Identifier 10.1109/LMWC.2011.2180369



(a) (b)

Fig. 2. (a) Output buffer and dummy buffer (b) simulated equivalent loading capacitances and capacitive loading variation due to buffer.

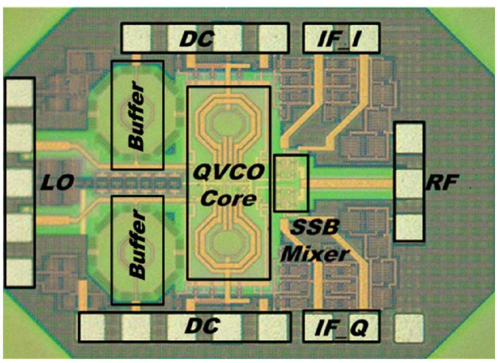
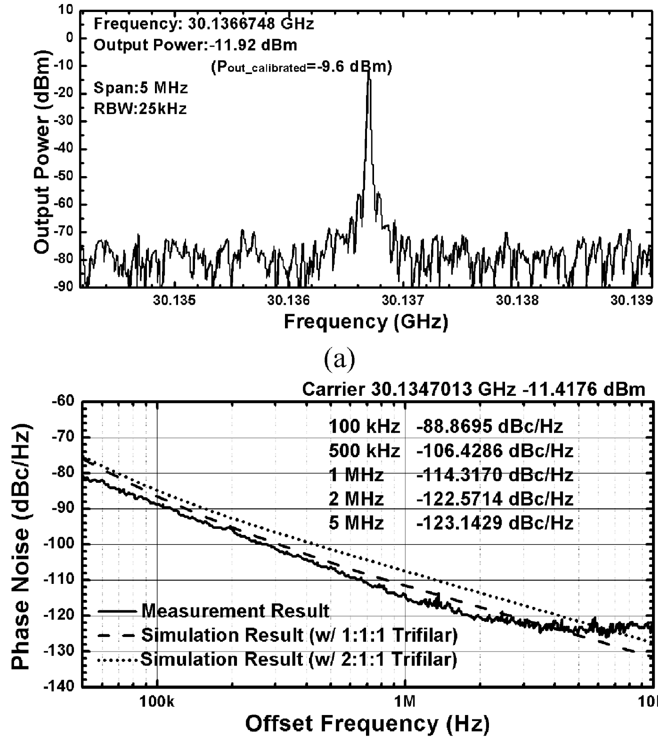


Fig. 3. Die photo of the QVCO using microwave trifilar transformers.



(b)

Fig. 4. (a) Output signal spectrum and (b) phase noise spectrum of the QVCO using microwave trifilar transformers.

suitable coupling strengths, instead of different turn ratios. The gate-to-drain coupling should be high enough to assure of a good inductor quality factor and overall phase noise. However, the gate/drain-to-source coupling provides a mutual coupling between I- and Q-VCOs and suffers from trade-offs between phase error and phase noise properties. Thus, the source line should be designed slightly away from the gate/drain lines to reduce the coupling strength. After fine-tuning, the trifilar transformer has an outer diameter of 140 μm with the metal thickness of 3.3 μm. The line widths ($W_1/W_2/W_3$) are 9/12/3 μm and line spacing (S_1/S_2) are 2/7 μm, respectively, where W_1-W_3 and S_1-S_2 are indicated in Fig. 1(b). The corresponding coupling coefficients k_{gd}, k_{ds}, and k_{gs} are 0.67, 0.35, and 0.3, respectively.

To fairly compare the two different layouts (the conventional 2:1:1 and newly proposed 1:1:1 types), the same oscillation frequency of 30 GHz and similar frequency tuning range are designed. As a result, the equivalent tank parallel resistance $[R_p \approx (1+Q^2)R_s \propto Q^2]$ of the QVCO (at resonance) using the 1:1:1 layout is around 1.6 times higher than that using the 2:1:1 layout. The corresponding simulated phase noise properties are indicated in Fig. 4(b) in Section III. The phase noise is then improved by around 4 dB at 1 MHz offset frequency. Note that, the chosen 2:1:1 trifilar transformer for comparison has the coupling coefficients k_{gd}, k_{ds}, and k_{gs} of 0.5, 0.5, and 0.25, respectively. Different turn ratios of the two cases result in different optimal design of coupling strengths.

A common-source (CS) buffer amplifier with an inductive load is used here to maintain the high-frequency response. For area saving, only one CS amplifier is employed in each I/Q-VCO, say I+ and Q+, as shown in Fig. 2(a). However, this placement may cause significant signal imbalance. Thus, a dummy transistor with an open drain node is employed at the other port of each VCO, *i.e.*, I− and Q−. The simulated load capacitance of both CS buffer and open-loaded dummy are shown in Fig. 2(b). After fine-tuning, at a target-oscillation band of around 20 to 30 GHz, the capacitance loading is minimized. Note that, parasitic capacitance matching can be further improved by connecting the drain bias of the dummy transistor to V_{D2} at the cost of additional power consumption.

A standard single-sideband upconversion passive mixer is implemented to fairly measure I/Q phase error of the QVCO [1] to avoid the measurement inaccuracy resulting from amplitude/phase mismatches in wires and connectors at high frequencies. Besides, assuming the sideband rejection (SBR) in an upconversion is totally dominated by the quadrature phase error (ϕ) of the LO oscillator

$$SBR = -20\log\left|\tan\left(\frac{\phi}{2}\right)\right|. \quad (1)$$

Once the SBR is measured, the equivalent worst-case phase error can be obtained by (1).

III. Measurement Results

Fig. 3 shows the die photo of the QVCO utilizing a pair of microwave trifilar transformers. The die size is 1.1×0.8 mm^2 while the QVCO core only occupies 180×450 μm^2. The supply voltage of the VCO core is 0.6 V with the core current consumption of 13 mA, while each CS buffer consumes 1.6 mA from a 1.2 V supply. Both the output signal spectrum and the phase noise spectrum are measured by Agilent E5052A signal

TABLE I
PERFORMANCE COMPARISON

Reference	Supply (V)	Frequency Range (GHz)	Power Consumption (mW)	Sideband Rejection (dB)	Phase Error	Phase Noise (at 1MHz offset)	FOM[b] (dBc/Hz)	FOM_T[c] (dBc/Hz)	Technology
[5]	1	14.8-17.6	5	38	1.4° [a]	−110 dBc/Hz	−187.6	−192.4	0.18-μm CMOS
[6]	1.2	5.65-5.9	8.64	37.7	1.5° [a]	−125.8 dBc/Hz	−191.6	−184.3	0.35-μm SiGe HBT
[8]	1.45	4.94-5.22	8.7	N.R.	0.65°	−124.6 dBc/Hz	−189.4	−184.2	0.18-μm CMOS
[9]	1.4	5.3-5.44	11.2	N.R.	~5°	−119 dBc/Hz	−183	−171.3	0.18-μm CMOS
[10]	3	22.07-22.9	187.5	N.R.	N.R.	−121.2 dBc/Hz	−185.6	−177	InGaP/GaAs HBT
This Work	0.6	26.8-30.3	7.8	41.6	0.95° [a]	−114.3 dBc/Hz	−195	−196.7	0.13-μm CMOS

[a] calculated from Eqn. (1).
[b] FOM=$PN-20\log(f_0/\Delta f)+10\log(P_{DC}/1\text{mW})$, where PN=phase noise, f_0=center frequency, Δf= offset frequency, and P_{DC}=VCO core power consumption.
[c] $FOM_T= PN-20\log(f_0/\Delta f)-20\log(TP/10\%)+10\log(P_{DC}/1\text{mW})$, where TP=tuning percentage.

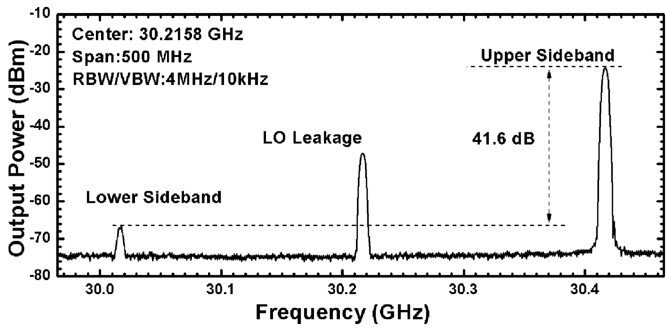
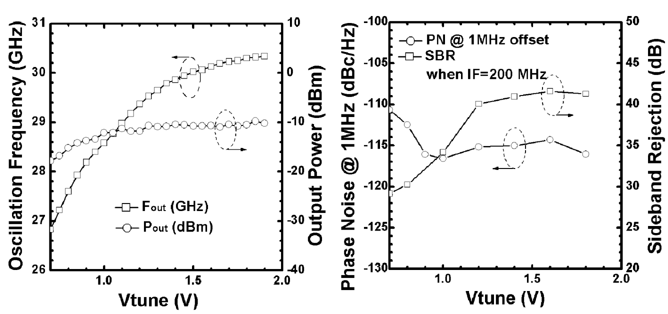


Fig. 5. Output spectrum at RF port of the single-sideband upconverter with a 41.6 dB sideband rejection.



(a) (b)

Fig. 6. (a) Oscillation frequency and output power (b) phase noise at 1 MHz offset and sideband rejection of the proposed QVCO.

source analyzer with Agilent N5507A microwave downconverter (1.5 to 26.5 GHz) and Agilent 11970A (26.5 to 40 GHz) waveguide harmonic mixer modules. Fig. 4(a) shows the output signal spectrum around 30 GHz while the phase noise of the proposed QVCO is -114.3 dBc/Hz at 1 MHz offset frequency, as shown in Fig. 4(b). Note that, the difference between the simulated and measured data may result from the inaccuracy of the CMOS device flicker noise model. Fig. 5 shows the output frequency spectrum measured by Agilent E4448A spectrum analyzer at the RF port of the upconverter with a 41.6 dB sideband rejection (SBR) while the IF frequency is 200 MHz. The differential-quadrature IF signals are generated from off-chip passive quadrature hybrid (SMC DQK-705; 150–300 MHz) and differential transformer baluns (Tyco Electronics H-9; 2–2000 MHz). Besides, phase shifters are also employed to compensate the phase error of the balun, hybrid, and wire connections to probes. As a result, a 41.6 dB SBR is equivalent to a phase error of approximately 0.95° calculated from (1). The LO leakage results from slightly unbalanced buffer loading, phase error in passive IF balun, and also the device mismatches in the QVCO and the upconversion mixer.

The oscillation power and frequency of the proposed QVCO with respect to the tuning voltage are shown in Fig. 6(a). The output power of the QVCO stays around -10 dBm at frequency ranging from 28.5 to 30.3 GHz and falls to -18 dBm at 26.8 GHz. Note that, the simulated output power of the VCO core (without buffers) is -3 dBm. Besides, the phase noise at 1 MHz offset frequency and the SBR with respect to the tuning voltage are shown in Fig. 6(b). As a result, the phase noise at 1 MHz offset frequency is at most -115 dBc/Hz while the maximum SBR is 41.6 dB, and at least 29 dB covering the whole oscillation frequency band. The performance benchmark of the proposed QVCO and the state-of-the-art QVCOs [5], [6], [8]–[10] are summarized in Table I. Thus, both the FOM and $\mathrm{FOM_T}$ of the proposed QVCO are better than that of other QVCOs.

IV. CONCLUSION

A pair of 1:1:1 trifilar transformers in the proposed 30 GHz QVCO are used for high-frequency, low-area, and low-voltage operations. The 30 GHz QVCO achieves -195 dBc/Hz FOM and maximum SBR of 41.6 dB with the VCO core area of only $180 \times 450\ \mu\mathrm{m}^2$.

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