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Unipolar Ni/GeO_x/PbZr_{0.5}Ti_{0.5}O₃/TaN Resistive Switching Memory

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In this study we propose a resistive random-access memory (RRAM) using stacked GeO_x and PbZr_{0.5}Ti_{0.5}O₃ (PZT). Under unipolar-mode operation, the bilayers Ni/GeO_x/PZT/TaN RRAM shows a large resistance window of $>10^2$, for 85 °C retention, and a good DC cycling of 2000 cycles, which are significantly better than those shown by the single-layer Ni/PZT/TaN RRAM without the covalent-bond-dielectric GeO_x.

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1. Introduction

Although the charge-trapping flash nonvolatile memory (NVM)^{1–3} has the lowest switching energy among various NVM types, the degraded endurance from 10^5 to 10^4 cycles with large-scale devices is the basic physical limit, as reported in the *international technology roadmap for semiconductors (ITRS)*.¹⁾ Therefore, several NVM types, such as ferroelectric random-access memory (FeRAM),⁴⁾ magnetic random-access memory (MRAM), and resistive random-access memory (RRAM)^{5–26)} are being investigated. RRAM has attracted much attention for next-generation non-volatile memory applications owing to its simple structure, small cell size, and high speed. Numerous candidate materials for RRAM application exist including perovskite materials, such as Pr_{0.7}Ca_{0.3}MnO₃,⁵⁾ SrTiO₃,^{6,7)} and GeO_x/HfON,⁸⁾ and metal oxides, such as TiO₂,⁹⁾ NiO,¹⁰⁾ TaO_x,¹¹⁾ SiO_x,¹²⁾ and HfO₂,¹³⁾ which have been widely investigated. Unfortunately, the use of a large forming voltage accompanied with an abrupt current to form a filament conductive channel^{14,15)} may damage dielectric robustness and reduce cycling endurance.^{9–12)} To resolve the endurance issue, in this study we propose the ultralow-energy (ULE) RRAM.^{6–8)} A ULE memory with stacked covalent-bound GeO_x^{27,28)} and metal oxide feature both high- and low-resistance-state (HRS and LRS respectively) currents and a long endurance of 10^6 cycles. In this paper we discuss the purely unipolar mode of operation of Ni/GeO_x/PbZr_{0.5}Ti_{0.5}O₃(PZT)/TaN RRAM. In comparison with the control Ni/GeO_x/PZT/TaN RRAM without GeO_x, Ni/GeO_x/PbZr_{0.5}Ti_{0.5}O₃(PZT)/TaN has significantly improved switching and 85 °C retention characteristics; comparable characteristics could not be found in a similar covalent-bound SiO_x RRAM.¹²⁾

2. Experimental Procedure

RRAM devices were fabricated on standard Si wafers. For very-large-scale integration (VLSI) backend integration, the process began with the deposition of a 200-nm-thick SiO₂ layer on a Si substrate. Then, a 100-nm-thick TaN layer was deposited by physical vapor deposition (PVD). After patterning the bottom TaN electrode, a 30-nm-thick PZT film with an Ar/O ratio of 3/1 (PZT31) was deposited on the TaN/SiO₂/Si layer by PVD. An 8-nm-thick GeO_x layer was then deposited to form the stacked structure. Finally, the 50-

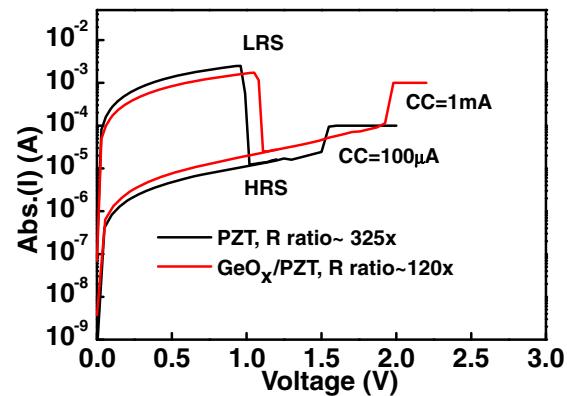


Fig. 1. (Color online) Swept I – V curves of Ni/PZT/TaN and Ni/GeO_x/PZT/TaN RRAM devices.

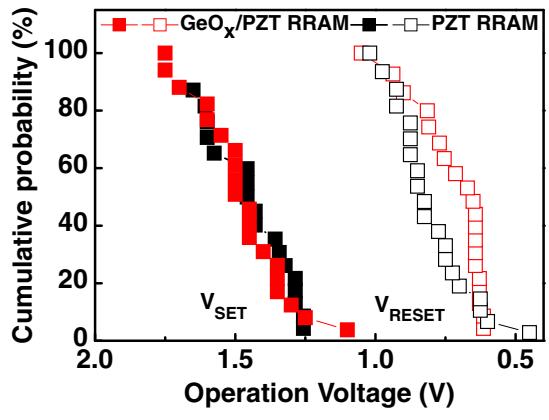
nm-thick Ni was deposited and patterned to form the top electrode with an area of $11300\mu\text{m}^2$. For comparison, a Ni/PZT/TaN RRAM device was also constructed without GeO_x. Ni provides a low-cost solution for fabricating high-work-function electrodes (5.1 eV), which are used in high- κ DRAM capacitors.²⁹⁾

3. Results and Discussion

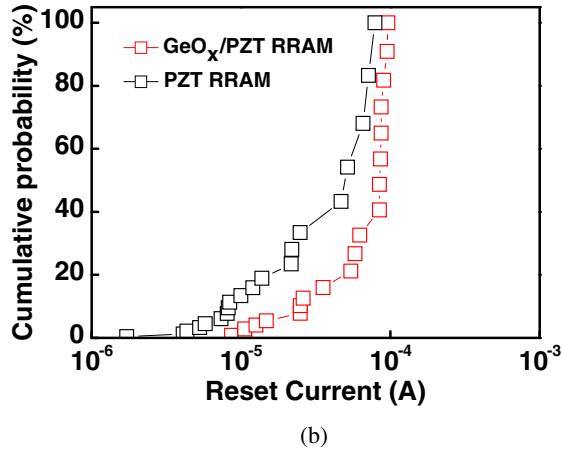
Figure 1 shows the swept current vs voltage (I – V) curves of Ni/PZT/TaN and Ni/GeO_x/PZT/TaN RRAM devices. The single-layer PZT and GeO_x/PZT RRAM devices have HRS/LRS resistance windows of 325 and 120, respectively. The smaller resistance window of Ni/GeO_x/PZT/TaN RRAM is due to the lower set current, although this is crucial for lower power operation. The higher set and reset voltages of the Ni/GeO_x/PZT/TaN RRAM than of the control Ni/PZT/TaN device are related to the extra GeO_x layer. The higher LRS current of the control Ni/PZT/TaN RRAM is ascribed to the conductive filaments. The lower set compliance current of 0.1 mA at 1.55 V for the control RRAM is due to the lower forming energy of filament paths in the vacancy-rich PZT than of filament paths in the stacked Ni/GeO_x/PZT/TaN one. However, a high LRS current and extra filament paths may lead to the serious endurance issue discussed below.

Figures 2(a) and 2(b) show the voltage and current distributions, respectively. The set voltage distributions of the Ni/GeO_x/PZT/TaN and control devices are similar, ranging from 1.7 to 1.1 V. However, the narrow reset voltage

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(a)



(b)

Fig. 2. (Color online) (a) Voltage and (b) current distributions of Ni/GeO_x/PZT/TaN and Ni/PZT/TaN.

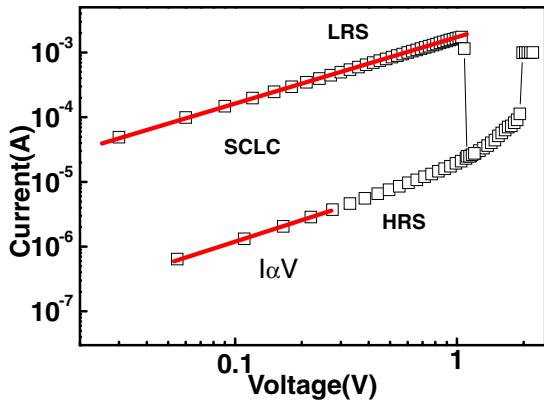


Fig. 3. (Color online) Set and reset I – V curves of Ni/GeO_x/PZT/TaN RRAM fitted using space-charge-limited current conduction mechanism.

distribution of Ni/GeO_x/PZT/TaN RRAM is slightly better than that of the control Ni/PZT/TaN devices. A similarly tighter distribution of reset current is also found in the stacked Ni/GeO_x/PZT/TaN RRAM. Therefore, the stacked GeO_x/PZT RRAM may assist in disrupting the filament paths during the reset operation.

Figure 3 shows the set and reset I – V curves of the Ni/GeO_x/PZT/TaN RRAM. In the low electric field, both the LRS and HRS exhibit trap-controlled space-charge-limited current (SCLC) because the slopes is proportional to V .³⁰

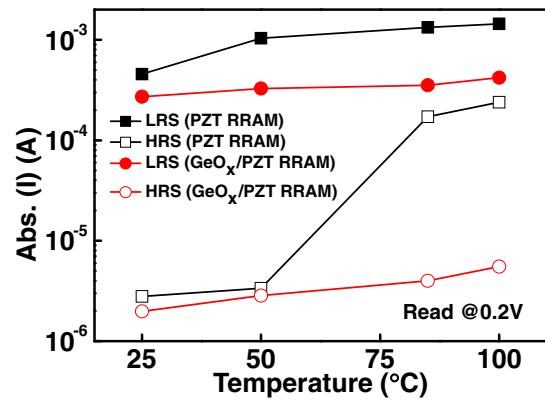
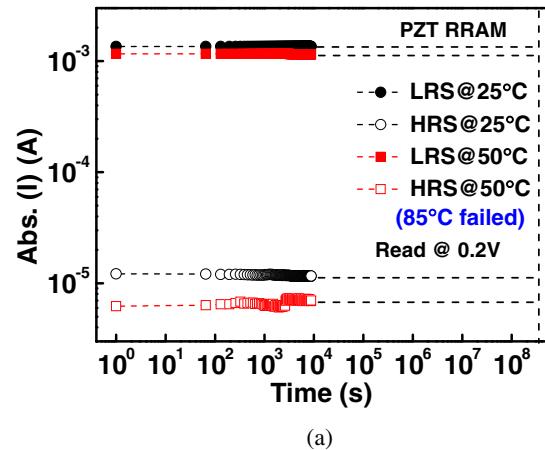
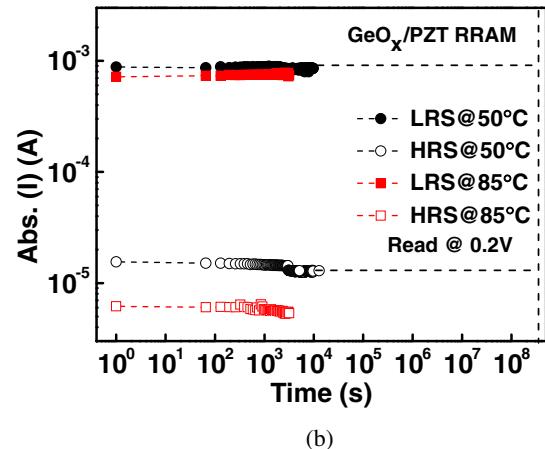


Fig. 4. (Color online) Temperature dependences of currents of Ni/GeO_x/PZT/TaN and Ni/PZT/TaN devices.



(a)



(b)

Fig. 5. (Color online) Retention characteristics of (a) Ni/PZT/TaN RRAM and (b) Ni/GeO_x/PZT/TaN RRAM devices.

Therefore, the filaments may be formed by the migration of oxygen vacancies during resistive switching.

Temperature-dependent I – V switching is crucial for evaluating high-temperature retention performance. As shown in Fig. 4, the Ni/GeO_x/PZT/TaN RRAM shows significantly better temperature stability from 25 to 100 °C than does the control Ni/PZT/TaN RRAM. The fast increase in the reset current of the control PZT RRAM with increasing temperature up to 80 and 100 °C is attributed to the high thermal leakage in the small-energy-bandgap PZT.

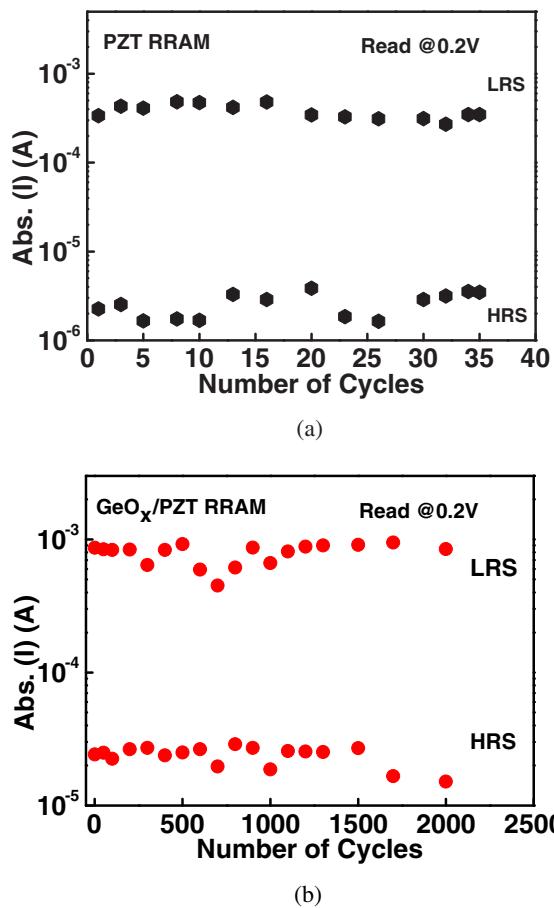


Fig. 6. (Color online) Endurance characteristics of (a) Ni/PZT/TaN RRAM and (b) Ni/GeO_x/PZT/TaN RRAM devices.

The retention characteristics of the control Ni/PZT/TaN and the Ni/GeO_x/PZT/TaN RRAM devices from 25 to 85 °C are shown in Fig. 5(a) and 5(b), respectively. The control Ni/PZT/TaN RRAM is only retained up to 50 °C because the HRS current increases rapidly at 85 °C, as shown in Fig. 4. In contrast, the Ni/GeO_x/PZT/TaN RRAM shows a significantly improved retention at 85 °C, which is related to the large bandgap⁶⁾ and high activation energy of GeO_x.

Endurance characteristics are significant factors of a unipolar RRAM device because of both the high set current and the poor control of filament size after the forming process.^{9–12)} Figures 6(a) and 6(b) show the DC endurance characteristics of the control Ni/PZT/TaN and Ni/GeO_x/PZT/TaN RRAM devices at a read voltage of 0.2 V, respectively. The control Ni/PZT/TaN RRAM device only lasts for 35 DC cycles. Such poor endurance originates from the passage of a large current in the weak conductive filaments of the device. In contrast, the Ni/GeO_x/PZT/TaN RRAM is considerably robust for cycling with a significantly high endurance of 2000 cycles. This improved endurance and data retention demonstrate the benefits of adding a large-energy-bandgap GeO_x to the unipolar-mode RRAM. Table I shows a summary of the pertinent data of various unipolar RRAM devices. The Ni/GeO_x/PZT/TaN RRAM device proposed in this study features the ideal low set/reset voltages, a resistance window of >10², suitable 85 °C retention, and good endurance characteristics among unipolar RRAM devices.^{6,9–12)}

Table I. Comparison of pertinent data of various RRAM devices under unipolar mode of operation.

	GeO _x /STO ⁶⁾	TiO ₂ ⁹⁾	NiO ¹⁰⁾	TaO _x ¹¹⁾	SiO _x ¹²⁾	GeO _x /PZT (This study)
I _{SET}	1 mA	1 mA	0.4 mA	1 mA	1 mA	1 mA
at V _{SET}	at 0.8 V	at 1.2 V	at 3.9 V	at 2.3 V	at 5.5 V	at 1.9 V
I _{RESET}	0.8 mA	70 mA	6 mA	0.1 mA	5 mA	1.7 mA
at V _{RESET}	at 0.2 V	at 1 V	at 1.5 V	at 0.7 V	at 1.5 V	at 1 V
On/off ratio	700×	~10 ³	50×	80×	~10 ⁵	125×
Retention	—	—	—	2.4 × 10 ⁴	10 ⁴	3000
Cycling	—	75	95	100	55	2000

4. Conclusions

In this study we demonstrate stable resistive switching behaviors in a Ni/GeO_x/PZT/TaN device. Compared with the control Ni/PZT/TaN RRAM, Ni/GeO_x/PZT/TaN device showed markedly improved retention and endurance. The Ni/GeO_x/PZT/TaN device could be a potential candidate for unipolar mode operations.

Acknowledgement

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