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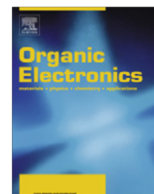

Facile synthetic route to implement a fully bendable organic metal–insulator–semiconductor device on polyimide sheet

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ABSTRACT

Triblock copolymer surfactant, $HO(CH_2CH_2O)_{20}(CH_2CH(CH_3)O)_{70}(CH_2CH_2O)_{20}H$ (i.e. P123)-based nanocrystalline (nc)-TiO_2 thin film had been synthesized on organic flexible polyimide (PI) sheet for their application in organic metal–insulator–semiconductor (MIS) device. The nc-TiO_2 film over PI was successfully deposited for the first time by a systematic solution proceeds dip-coating method and by the assistance of triblock copolymer surfactant. The effect of annealing temperature (270 °C, 5 h) on the texture, morphology and time-induced hydrophilicity was studied by X-ray diffraction (XRD), atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS) and contact angle system, respectively, to examine the chemical composition of the film and the contact angle. The surface morphology of the semiconducting layer of organic pentacene was also investigated by using AFM and XRD, and confirmed that continuous crystalline film growth had occurred on the nc-TiO_2 surface over flexible PI sheet. The semiconductor–dielectric interface of pentacene and nc-TiO_2 films was characterized by current–voltage and capacitance–voltage measurements. This interface measurement in cross-link MIS structured device yielded a low leakage current density of 8.7×10^{-12} A cm^{-2} at 0 to -5 V, maximum capacitance of 102.3 pF at 1 MHz and estimated dielectric constant value of 28.8. Furthermore, assessment of quality study of nc-TiO_2 film in real-life flexibility tests for different types of bending settings with high durability (c.a. 30 days) demonstrated a better comprehension of dielectric properties over flexible PI sheet. We expected them to have a keen interest in the scientific study, which could be an alternate opportunity to the excellent dielectric–semiconductor interface at economic and low temperature processing for large-area flexible field-effect transistors and sensors.

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1. Introduction

Flexible technology in electronics production has attracted considerable attention for a wide-range of applications because it is a new process of creating electronic circuits on a roll of plastic sheets. This is a new technology, which is expected to meet the growing demand for low-cost, large-area, flexible and lightweight devices, such as roll-up displays, e-papers, connectors, and keyboards [1,2]. Being a novel technique, much attention has been paid to the development of electronic circuits on flexible substrates since the end of 20th century. An important consideration for active devices is the isolation between an input and output signal. Insulators are widely used to provide this isolation [3]. Subjected to fabricate the flexible devices over plastic substrates, it is necessary to grow gate dielectrics at relatively low temperature compared with those of conventional silicon (Si) substrate based devices owing to temperature stringency associated with plastic

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sheets. Organic/polymer materials [4,5] have attracted a lot of attention for building large-area and mechanically flexible electronic devices. These materials are widely pursued since they offer numerous advantages for easy-processing (e.g., spin-coating, printing, and evaporation), good compatibility with a variety of substrates including flexible substrates, and great opportunity for structural modifications. Owing to the limitations in development of flexible devices, the present mainstream strategy is an attempt in achieving bendable electric devices and is not to develop new materials, but instead is to engineer new structures from established materials. Apart from the above, as shown in the International Technology Roadmap for Semiconductors (ITRS) guidelines, interlayer metal insulating materials need to have dielectric constants of about 20–30 to effectively isolate devices having sizes <100 nm [6]. Thus, much attention has been given to the research and development of new materials with high-*k* value and new deposition processes. Titanium-dioxide (TiO_2, titania) is the most promising candidate used as gate dielectric material for its high efficiency, safety, cleanness and low cost [7,8]. In general, researchers concentrate on one aspect to improve the performance of the electronic devices by improving the dielectric efficiency at low temperature. The highly hydrophilic property presents interesting applications of TiO_2 films such as anti-fogging and self-cleaning [9,10]. There is also a strong desire for microelectronic industry to develop advanced and large-scale techniques that can meet the growing demand of low temperature (ca. 25 °C) deposition processing on flexible substrates, miniaturization, and which should be easy-to follow. But researchers have had little success in making ultrathin films at low temperature by using spin-coating [11] or printing techniques [12]. However, limitations in such existing approaches to interoperation at the network transport and application levels are observed for the flexible devices. A major goal for the realization of flexible electronics is the development of solution processing and functional materials that afford both direct deposition of electronic components (including resistors, diodes, capacitors, transistors and interconnects) and high performance devices. The dip-coating technology [13,14] is exceptionally promising because patterns can be generated without any material waste, which could lead to drastic reductions in production costs and in environmental impact. In our previous study, we have assessed the use of specific sol–gel preparation to obtain useful spin coated high-k HfO_2 film to be used as dielectric layer in organic thin-film transistor [15]. However, the spin coating technique is not suitable for fabricating the TiO_2-based metal–insulator–semiconductor device on polyimide sheet due to the cracking problem on the film surface.

In present study, for the first time, we present an interestingly new and easy-to-follow synthesis procedure to prepare triblock copolymer surfactant $HO(CH_2CH_2O)_{20}(CH_2CH(CH_3)O)_{70}(CH_2CH_2O)_{20}H$-based nanocrystalline (nc)-film dielectric layer at room temperature via the dip-coating solution process. The electrical insulating properties of fully bendable MIS device prepared employing nc-TiO_2 film as a dielectric layer and pentacene as semiconductor layer, exhibited low leakage current density, and good capacitance with high durability. We realized that the dip-coating technique provides a uniform thin film deposition level on flexible substrate at low temperature than other standard thin film deposition techniques. This new synthesis process to fabricate nc-TiO_2 at low temperature demonstrated good stability when using in electronic device as dielectric layer, and exhibited excellent results in comparison with other high-k dielectric materials. We expect that these important features will allow this novel synthesis route and deposition method to be used at large scale in flexible electronic device applications.

2. Experimental section

2.1. Chemicals and materials

Pluronic® P123 hydrocarbon surfactants [triblock copolymer with molecular weight of 5800 Da and formula of $HO(CH_2CH_2O)_{20}(CH_2CH(CH_3)O)_{70}(CH_2CH_2O)_{20}H$, abbreviated as P123] was purchased from BASF Corporation. Ethanol (C_2H_5OH, 99.5% Aldrich)) and titanium chloride ($TiCl_4$) were obtained from Sigma–Aldrich Chemie Gmbh. Deionized water (DI water) used was purified with filters, reverse osmosis and deionized system until the resistance was more than 18 $M\Omega\,cm^{-1}$. DI water was used to clean, wash and as a solvent. Chromium shots (Cr, 99.999%) with size of 3–5 mm, aluminum shots with size of 3–5 mm (Al, 99.999%) and gold shots with size of 1–2 mm (Au, 98.999%), were purchased from Admat Inc. (Norristown, PA, USA). All chemicals were used without further purification. Pentacene as the organic semiconductor material was purchased from Seedchem Pty Ltd. (Electronic Grade, South Africa). DuPont™ Kapton® Polyimide (abbreviated as PI) film (38-μm thickness of PV9100 series) was used as substrate to fabricate the device.

2.2. The nc-TiO_2 film preparation

To deposit nc-TiO_2 thin film, a synthesis solution was prepared by dissolving 2.0 g P123 into mixture solution of 20 g C_2H_5OH and 1.0 g DI water; depicted in Scheme 1a. Then, poured slowly 1.5 g of $TiCl_4$ to the solution as shown in Scheme 1b. Proper caution should be taken during the addition of $TiCl_4$ into mixed solution of C_2H_5OH/H_2O/P123, because of the exothermic reaction takes place in situ. It is then vigorously stirred for 24 h in an ice-water bath. For the first day, the color of the solution was yellowish-green and almost after 5 days, the color of the solution disappeared and colorless solution was obtained as shown in the photographs given in the Scheme 1b. This colorless solution remains stable for several weeks at room temperature. Before coating the film, the solution was aged at 60% relative humidity for 2 h at room temperature, and then thin film was deposited by dip-coating the PI sheet rapped over glass substrate at a constant withdrawal rate of 1 mm/s, a home-made instrument for film deposition via dip-coating process is shown in image below the Scheme 1c. After dip-coating, aging the film for another 5 min at 80 °C, the evaporation of C_2H_5OH, HCl, H_2O and a disorder-to-order transition occurred (Scheme 1d). Finally, as-synthesized

Scheme 1. (a–e) Schematic illustration of the proposed synthetic solution and dip-coating approach for the uniform preparation of the nc-TiO_2 film throughout this work.

film was subsequently calcined by annealing in presence of O_2-flow at 270 °C for 5 h (Scheme 1e). This thermal treatment produced uniform nc-TiO_2 film further in device fabrication and material characterizations.

2.3. Device fabrication

The process steps in fabrication of MIS device over PI including its bending structured formation is described in Fig. 1a and b; plastic 38-μm thick DuPont Kapton® PI sheet was used as flexible substrate for the fabrication of MIS capacitor. The PI film was cleaned ultrasonically with ethanol (Fluka; water content: <0.1%) for 30 min and DI water and then high-pressure N_2 gas was used to remove the water and any remaining particles from the PI surface. PI substrate was annealed at 200 °C for 15 min in vacuum to achieve a relative thermal stability, and enhancement of the adhesion strength. After cleaning up a PI substrate, a 50-nm thick Cr as adhesion layer and 100-nm thick Au were deposited sequentially on the PI substrate by thermal coater. The Cr layer was used as the adhesion layer between the PI substrate and the Au film. Au was deposited for the gate electrode onto Cr-coated PI. The 25-nm TiO_2 film from organic–inorganic blend via dip-coating process was fabricated as dielectric layer; the thickness of the above film was measured by spectroscopic ellipsometry techniques. And then, pentacene film of 50-nm as a semiconductor layer was deposited by using a thermal coater with substrate maintained at the room temperature. At the end of the experiments, 200-nm thick Al film was pattered as the top electrode by using shadow mask and a thermal coater. Fig. 1c shows a photograph of an array of MIS devices (c.a. 80 devices) patterned on area of

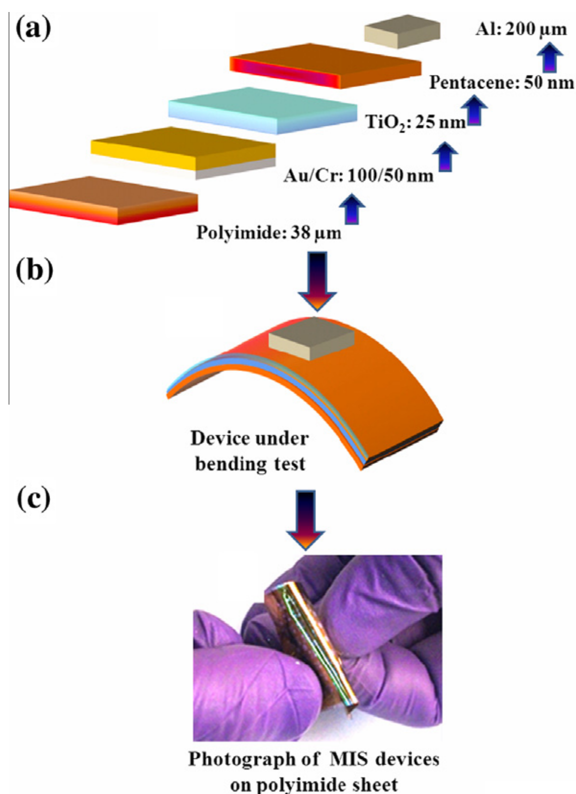

Fig. 1. (a) Schematic representation of fabrication steps for an MIS device where a high-k TiO_2 thin film from organic–inorganic blend and the organic pentacene as semiconductor layer on PI substrate; (b) MIS device featuring a bending test; (c) photograph of an array of MIS devices patterned on area of 5 × 5 cm^2 on the flexible PI sheet.

5×5 cm^2 fabricated on the fully flexible PI substrate under a large surface strain.

2.4. Film characterizations and device measurements

The surface morphology of the TiO_2 thin film from organic–inorganic blend over PI was evaluated by AFM, (Digital Instruments Nanoscope, D-5000) at scan size of $2\ \mu m \times 2\ \mu m$ and a scan rate of 1 Hz. XRD patterns were obtained by using a Rigaku D/max-IIIB diffractometer under Cu Kα radiation (λ = 1.5406 Å). In addition, the surface morphology of pentacene film was also evaluated by AFM at a scan size of $3\ \mu m \times 3\ \mu m$ and a scan rate of 1 Hz, and the XRD analysis as described above. We used XPS to analyze the chemical bonding of the elements of interest under various treatment conditions for TiO_2 film. The hydrophilicity of the nc-TiO_2 surface was evaluated from contact angle measurement system. Deionized water was used as the water source for the contact angle determination. The contact angles measured for 5 min after the drop has made contact with the film surface of interest. Measurements for leakage current and capacitance of the device were performed by an Agilent-4156 probe station and an HP-4284A capacitance–voltage (C–V) analyzer, respectively. We tested two additional features for our MIS device fabricated on PI flexible substrate to explore the feasibility for the purpose of practical application. A sequential flexibility test including of convex and concave under different radii of curvatures was acquired. Prior to manufacturing process, a foil was used as a substrate support to provide these specific bending conditions in convex and concave settings for different radii of curvatures varies from 1.5 to 4.0 cm. Finally, we performed the real life flexibility tests for one array of flexible MIS devices repeatedly crumpled in the palm of a hand and then electrical performance was measured.

3. Results and discussion

3.1. Film quality and surface roughness of nc-TiO_2

The prepared and annealed samples of TiO_2 thin films on clean Au/Cr coated PI substrate are subjected to surface analysis by AFM. The texture and surface morphology of nc-TiO_2 films were investigated for as-deposited then baking at 80 °C and annealing in O_2-flow at 270 °C for 5 h, as shown in Fig. 2a and b, respectively. The scans were carried out in a tapping mode for $2\ \mu m \times 2\ \mu m$ scales. The images on the right are from their three dimensional images from films of as-deposited and annealed. Fig. 2a clearly shows particles with almost uniform size in the calcined nc-TiO_2 thin film and the film surface is crack-free in nature. Another important observation is the TiO_2 crystallites grown on Au/Cr coated PI tend to arrange into somewhat self-assembled uniform structures with minimum distance between them. However, when the calcinations temperature is increased to 270 °C for 5 h, aggregation of the TiO_2 crystallites occurs more specifically; which can be seen clearly from Fig. 2b. It was found that there is no pronounced increase in the crystal size as the calcinations temperature mentioned at 270 °C is only for 5 h or more. We cannot test the temperature near or above 300 °C because of low thermal compatibility of PI film.

The respective root-mean-square (rms) values of the surface roughness of as-deposited and annealed films are 2.34 and 2.18 nm. This observation could be ascribed to the fact that only a minority of primary TiO_2 crystallites aggregate to larger secondary particles when the calcination temperature is increased. Thus, 270 °C could be considered to be the optimum reaction temperature range for obtaining nc-TiO_2 thin films with uniform morphology and particle size from Fig. 2b. The thickness of as-deposited film is 28 nm from the measurement of ellipsometry techniques, while the thickness of the annealed film is 25 nm. There is only a small decrease in thickness for dip-coated film annealed at 270 °C for 5 h, but without degrading the surface smoothness. This observation confirms that the P123 surfactant plays an important role to smooth the crystalline film of TiO_2 via surface dip-coating process on PI. The observed small change in the thickness is consistent with the relatively small volume of Triblock copolymer P123 surfactant present, which favors particle–particle contact in the multilayers prior to calcination. Therefore, there is only a small decrease in the film thickness after the evaporation and removal of the Triblock copolymer P123. The nanoparticles of TiO_2 seem not to collapse on one another, and demonstrate smooth film surface as shown in Fig. 2b.

3.2. XRD analysis

The identification of the phase structure of TiO_2 film calcined at temperature 270 °C in O_2^- ambient was investigated by XRD analysis and the result is shown in Fig. 3. As can be seen, the XRD result of the as deposited then baked at 80 °C for 5 min TiO_2 film is considerably the amorphous phase. There was hardly any peak observed for baking at 80 °C treatment condition. However, the amorphous phase is turned into a stable grained nanocrystalline anatase phase under a temperature of 270 °C for 5 h, and this structure does not alter on subsequent cooling to room temperature. The XRD patters for annealed at 270 °C treatment condition features the six intensity diffraction peaks in the range of 25.3°–62.8°. Those are indexed as (1 0 1), (0 0 4), (2 0 0), (1 0 5), (2 1 1), and (2 0 4) diffraction peaks. They showed the typical patterns for the anatase structure of Joint Committee on Power Diffraction Standards (JCPDS) No. 21-1272. The crystallite size was estimated for the broadening of the diffraction peaks by using the Scherrer equation: $D = 0.89\lambda/\beta\cos\theta$, where D is the crystallite size, λ is the wavelength of the X-ray radiation (λ = 1.5406 Å), β is the peak width at half-maximum height after subtraction of the equipment broadening, $2\theta = 25.3°$ for anatase (1 0 1), and 0.89 is the Scherrer constant. As calculated from the Scherrer equation by using the (1 0 1) diffraction peak of anatase for sample annealed at 270 °C, the average crystalline size was 8.0 nm. It was found that there is a pronounced phase change for TiO_2 surface as the calcination temperature increases, which attributed to the growth of crystalline TiO_2 surface. It is of interest to note that for Au/Cr/PI system, the inclusion of Au and Cr in the deposits was almost completely suppressed under suitable condi-

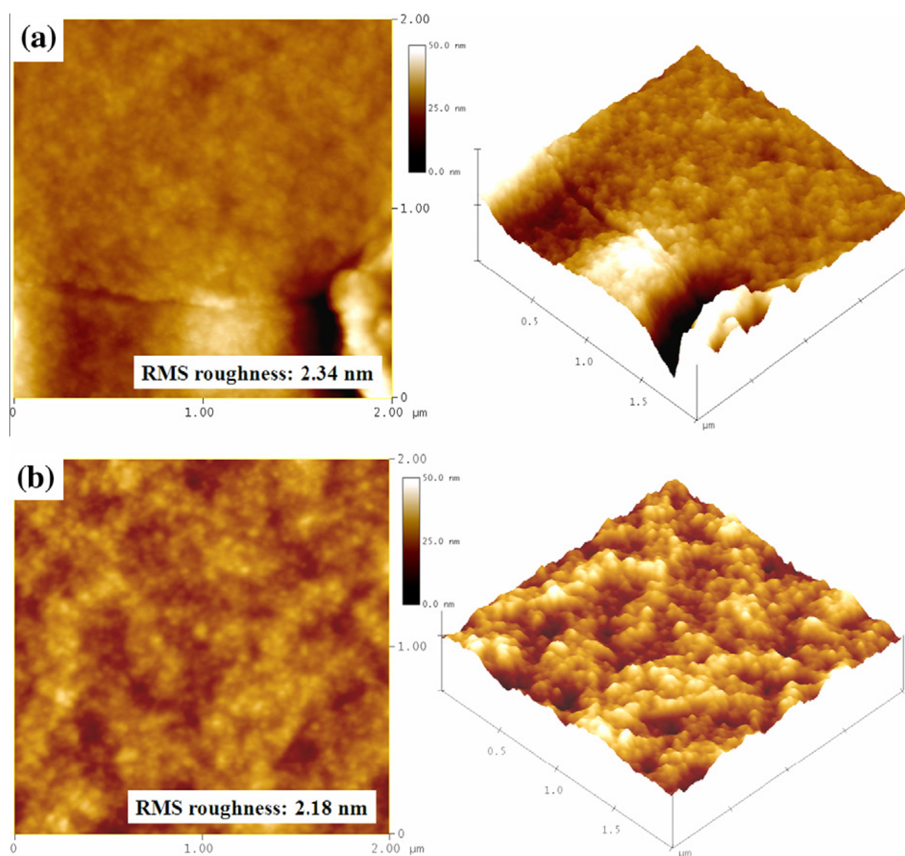

Fig. 2. AFM images from thin film of nc-TiO_2 coated on Au/Cr/PI surface calcined at different temperatures conditions for (a) as-deposited then baking at 80 °C for 5 min, and (b) annealed in O_2 flow at 270 °C for 5 h.

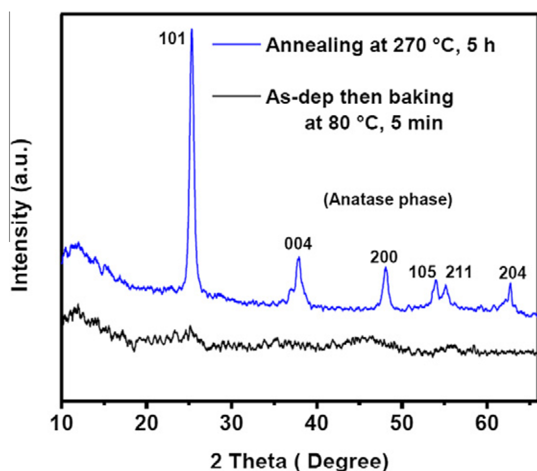

Fig. 3. XRD patterns (intensity in arbitrary units, but the intensity scale is identical for both patterns.) from TiO_2 film sintered at 80 °C baking for 5 min and annealed at 270 °C for 5 h, respectively.

tions. Here, the gold and chromium shots contained in the tungsten crucible were thermally evaporated in a high vacuum chamber by heating it to near its evaporated point. The resulting treats with the spray vapor of chromium and gold layers deposited on a flexible PI substrate. It may depends on several factors, notably the temperature of the substrate during growth, the temperature after growth and the length of time the substrate is held at that temperature, the flux of chromium and gold atoms striking the substrate, the flatness and cleanliness of the substrate, and the ambient environment of the substrate during and after growth.

3.3. XPS analysis

Quantitative XPS analysis was performed for both as deposited and the annealed nc-TiO_2 films on the Au/Cr/PI substrate. We performed the XPS measurement over Au/Cr/PI substrate because of matching the similar conditions as in MIS device demonstrated over Au/Cr/PI substrate. Typical survey for low-resolution spectra is presented in Fig. 4a. The observed binding spectra of the TiO_2 film contain the Ti 2p and O 1s peaks of the titanium dioxide and a small amount of contaminating carbon; no other impurities (e.g., chloride ions) were present on the film surface. The survey spectrum of the film surface also contains C 1s and Au 4f, Au 4d peaks in addition to the Ti 2p and O 1s peaks, confirming the presence of the titanium oxide surface modifier. Cr peak is hardly observed at peak posi-

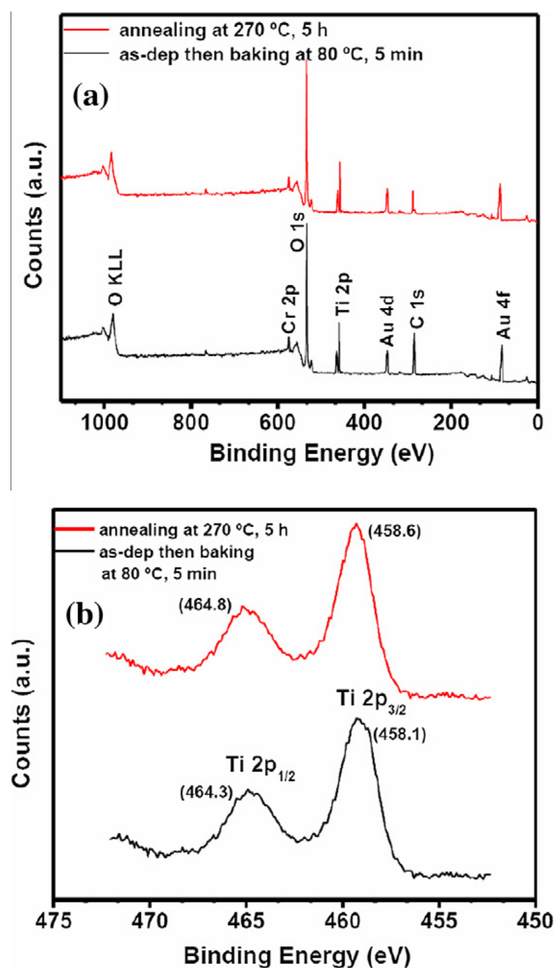

Fig. 4. (a) Low resolution XPS spectra for dip-coated nc-TiO_2 film over Au/Cr/PI surface, and (b) high-resolution XPS spectra of the Ti 2p energy levels subjected to respective treatment of 80 °C baking for 5 min or 270 °C annealing for 5 h.

tion 74.8 eV for Cr 2p, because the emitted photoelectron cannot diffuse out of the TiO_2 and Au films. The spectrum for as-deposited sample contains C 1s peak at 284.8 eV, may be associated with hydrocarbon bond or other carbon contaminated particles in the presence of surfactant triblock copolymer Pluronic P123 over film surface. Furthermore, it was observed that the peak intensity of C 1s was decreased as the sample annealed at 270 °C for 5 h in O_2-ambient. While the O 1s peaks at 531.8 (as-deposited) and 532.2 eV (annealed at 270 °C, 5 h) confirm the presence of the surface modifier as peak shifts to higher binding energy (BE) site. The other components near the binding energies of 531.8 and 532.2 eV may mainly correspond to hydrated bonds or carbonate caused by contamination on the film surface. The triblock copolymer Pluronic P123 is the uniform-structure-directing agent to prepare nc-TiO_2 film in an aqueous solution and it has been evaporated and removed when the sample heated in O_2-flow at 270 °C for 5 h.

In order to understand the formation mechanism, the effect of P123 on the morphology was examined first. In an aqueous solution, triblock copolymer micelles tend to form a core–shell structure by the segregation of insoluble blocks into the core and hydrophilic blocks into the shell. From the XPS results, we concluded the that P123 could confine and direct the growth of pure TiO_2 surface observed over flexible PI by dip-coating solution process, which enhance the property of the MIS device. Fig. 4b displayed high-resolution spectra of the Ti 2p energy levels for as-deposited then baked at 80 °C for 5 min and annealed at 270 °C for 5 h samples. For the baking-only treatment, the spin–orbital splitting of Ti $2p_{1/2}$ (464.3) and Ti $2p_{3/2}$ (458.1) peaks was observed with a separation of 6.2 eV. After annealing-only treatment, these binding energies were raised to 464.8 and 458.6 eV, and with the same separation of 6.2 eV. These binding energies shifted towards higher BEs, which observation implied that, during the annealing in presence of O_2, oxygen molecules reacted with the Ti dangling bonds to form stronger Ti–O bonds and converting the as deposited film into the pure TiO_2 film. This observation was in good agreement with the reported literature [16,17]. From this result, it was clear that the TiO_2 film by dip-coating process was successfully deposited over PI substrate. The shift toward higher BE for the Ti–O bonds suggested that annealing treatment introduced some oxidation of the Ti atoms.

3.4. Water contact angle measurements for nc-TiO_2 film

Self-cleaning properties of TiO_2 film are very desirable, and potentially has various advantages. For example, it can defog glass, and it can also enable oil spots to be swept away easily with water. The effect of calcination temperatures (the as-synthesized samples were calcined at different temperatures) on the physical parameters for time-induced hydrophilicity of TiO_2 film was investigated in this study. The contact angles of water droplets were measured for both the as-synthesized then baking at 80 °C and annealing at 270 °C samples under ambient conditions. The observed trends can be easily found from Fig. 5a, a noticeable decrease in the water contact angles does not occur upon increase of time. The behavior of contact angle, for sample of as-synthesized then baking at 80 °C, is probably due to presence of polymer surfactant P123 species. In this case, temperatures are not high enough to promote decomposition of P123, and micelles may be formed because of both organic and inorganic components. It seemed that structural migration of the residual polymer surfactant P123 may affect the contact angle change at the surface of TiO_2 film because the P123 material has amphiphilic nature. For the waiting period of 5 min, no dramatic change (only from 88° to 63° in contact angle) was found over 10 cycles of continuous wetting. The as synthesized then baking only sample showed stable surface with some extent of hydrophobic character, which is probably due to the balance of both polymer surfactant P123 and precursor of TiO_2.

Meanwhile, we performed contact angle measurement for nc-TiO_2 film annealed at 270 °C for 5 h in O_2-ambient over 10 cycles of continuous wetting and drying. It was pointed out that the water contact angles of nc-TiO_2 thin films were dramatically decreased with time for 5 min. On the contrary, the sample showed liable hydrophilic

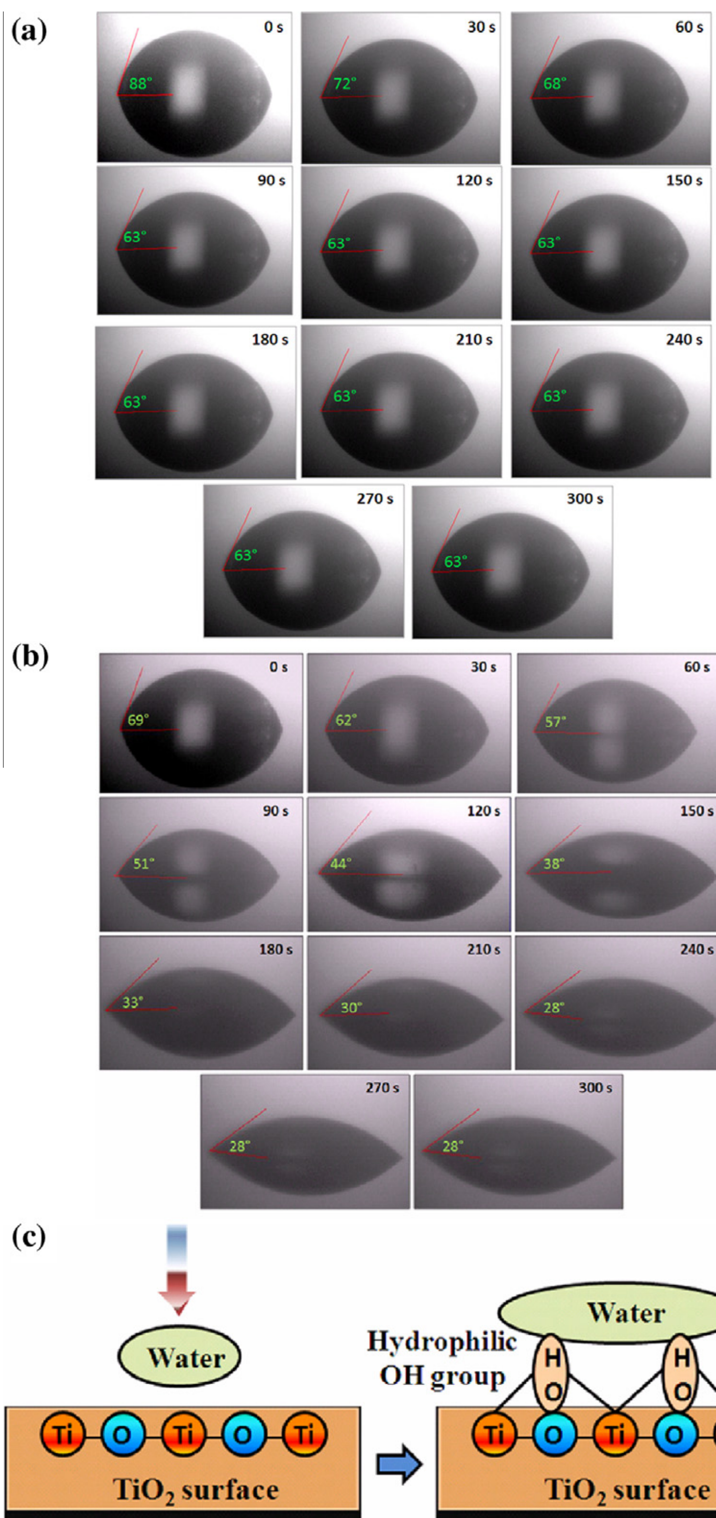

Fig. 5. (a) Time-dependant change in contact angle of water droplet on as synthesized TiO_2 thin film dip-coated over Au/Cr/PI surface, (b) time-dependant change in contact angle of water droplet on nc-TiO_2 thin film (annealed at 270 °C for 5 h in O_2-ambient) dip-coated over Au/Cr/PI surface, and (c) a schematic for the water drop exposed to the above TiO_2 surface.

nc-TiO_2 film surface, probably due to evaporation of P123. Fig. 5b shows the time-dependent change of water contact of nc-TiO_2 film coated over Au/Cr/PI surface. For nc-TiO_2 film, the water contact angle decreased progressively with

the number of cycles. After five cycles, the water contact angle started decreasing and gradually decreased from 69° (some extent of hydrophobic character) to about 28° (hydrophilic character), while performing the process for 5 min. A fast decrement in the contact angle occurs for the first 180 s and then the contact angles gradually decrease and remained constant. The concentration of OH groups available on the surface of nc-TiO_2 film results into time-induced hydrophilicity. Furthermore, our obtained nc-TiO_2 thin film presents more hydrophilic nature than previously reported sol–gel nc-TiO_2 thin film [13]. It is significantly interesting that the discovery of the time-induced superhydrophilicity of TiO_2 films has generated numerous exploring issues for future applications such as antifogging, self-cleaning, antibacterial and stain-proofing agents in advanced nanoelectronics. Fig. 5c depicts the possible surface structure route for sample of nc-TiO_2 film annealed at 270 °C for 5 h in O_2-ambient. Initially, the sample surface exhibits some extent of hydrophobic character due to the fabrication sample from P123-assisted dip-coating. However, once the surface contacts with the water drop, the extra surface hydrophilic OH group is formed and the interaction with water drop is gradually increased [18]. How to apply this surface character from both types of samples is an important issue for future study.

3.5. Surface analysis study for organic pentacene film

AFM and XRD experiments were performed in order to investigate the effects of the surface properties of the pentacene on the surface morphology of gate dielectric. Fig. 6a shows the XRD pattern and AFM image of 50 nm-thick-pentacene layer grown on as-deposited TiO_2 surface. The structure of pentacene layer was elucidated by XRD in reflection mode at 20 kV and Cu Kα radiation (λ = 1.5406 Å) with a coupled (θ–2θ) scans configuration. The corresponding XRD pattern contains a series of sharp (00k) peaks indicating that the pentacene film is highly ordered. The first peak at 5.7° (thin-film phase) corresponds to a lattice parameter of 15.6 Å. XRD analysis reveals that pentacene film on TiO_2-Au/Cr coated PI have a better crystal quality. The estimated grains size for pentacene film using Scherrer formula for the broad peak at 5.7° is about 500 nm.

Moreover, the grain size and morphology of pentacene film was observed by AFM to assess the crystalline quality, as shown in Fig. 6b. It is well known that the root-mean-square surface roughness (R_{rms}) of a film influences the electrical characteristics of electrical devices. The R_{rms} evaluated from AFM of pentacene is 4.82 nm as indicated in Fig. 6b. The AFM images of pentacene layer on as-deposited TiO_2 surface also revealed a dendritic structure with a grain size of about 500 nm. The data suggested a robust and pinhole-free TiO_2 film, where the growth morphology of pentacene was similar to those prepared on silicon or glass substrate [19,20]. After analyzing the surface morphology of pentacene film by using XRD and AFM, we confirmed that the deposited pentacene was crack-free, uniform, and well adhered onto the surface of TiO_2–Au/Cr/PI. Thus, the pentacene had uniform morphological surfaces.

3.6. Electrical measurements from pentacene/TiO_2-Au/Cr/PI structured MIS device

The good quality of an interface between an insulator and a semiconductor layer is extremely crucial for practical device operation and application. The leakage current and capacitance measurements allow the extraction of material parameters, such as dielectric constant and interface density. Here, the MIS structured devices were fabricated over flexible PI substrate for both conditions of as-deposited and annealed films. The dielectric properties of nc-TiO_2 film were evaluated via quantitative current density and capacitance measurements. Fig. 7a shows typical current density–voltage (J–V) plots for MIS geometry as shown in Fig. 1 with TiO_2 as insulator layer and pentacene as semiconductor layer.

As Fig. 7a displayed, the leakage current density of TiO_2 film for as deposited then baked at 80 °C is of the order of

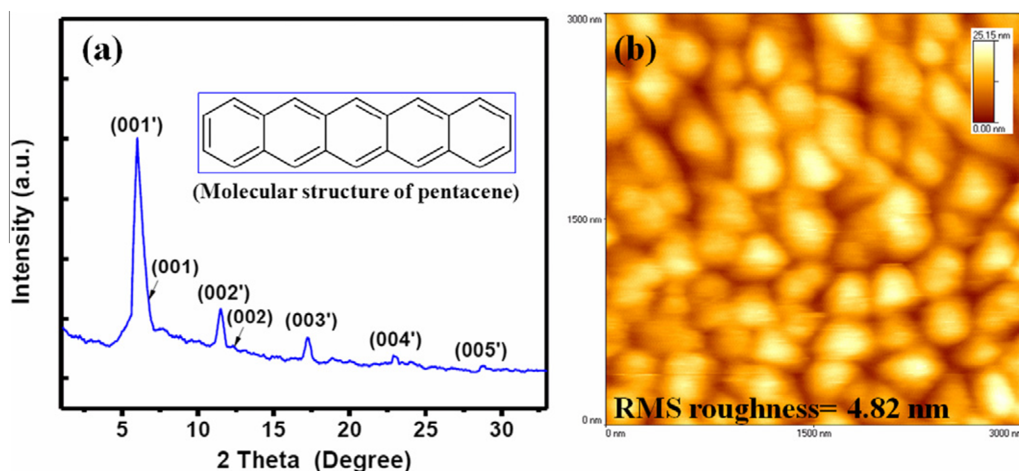

Fig. 6. (a) X-ray diffraction pattern of the pentacene deposited over TiO_2–Au/Cr/PI. Inset: molecular structure of pentacene, (b) AFM image (3 μm × 3 μm) of the pentacene over TiO_2–Au/Cr/PI.

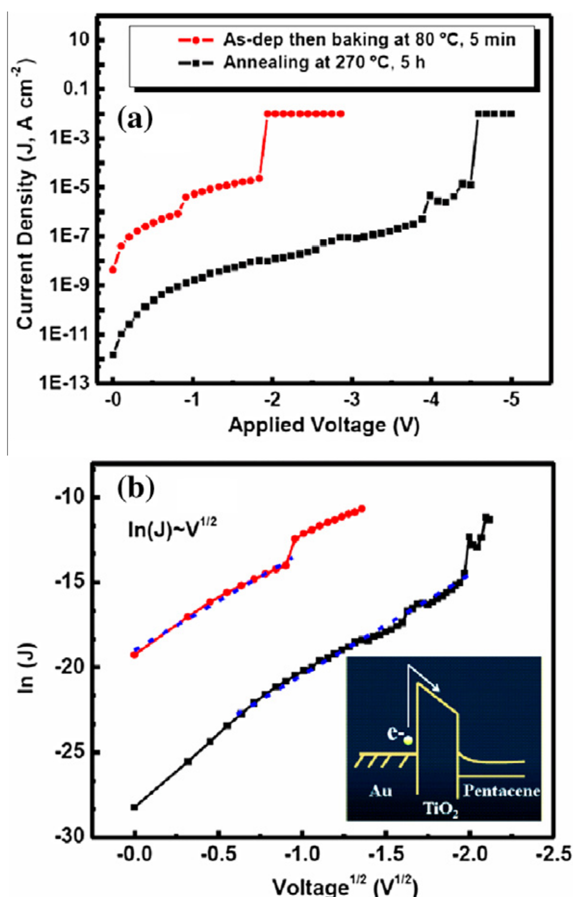

Fig. 7. (a) J–V characteristic when negative voltage applied, (b) Schottky emission ln(J) versus the square root of the electric field ($V^{1/2}$); inset: a schematic energy band diagram.

10^{-8} A cm^{-2} at applied negative voltage of 0–3 V. After annealing at 270 °C for 5 h, it decreased to the order of 10^{-11} A cm^{-2} at negative voltage of 0–5 V. As compared with the silicon based devices under high thermal process, the devices in Fig. 7a were achieved on relatively low temperature budget. Hence, the dielectric property of nc-TiO_2 film in the soft device would be expected to affect from some remaining carbon materials and lack of uniformity over nc-TiO_2 surface. However, we noted that the device with nc-TiO_2 film of 25-nm thickness deposited by dip-coating process exhibited superior insulating properties than the conventional silicon based MOS capacitor [19–24]. Table 1 [24–28] listed various deposition methods, deposited film thicknesses, dielectric constants, leakage current densities and processing temperature on our PI substrate and other silicon-based devices. In general, our soft device with P123-assisted nc-TiO_2 film demonstrated the superior property for low temperature processing issue and low leakage current. The J–V characteristics were measured by inject electron from bottom Au layer to TiO_2 layer (negative bias). Fig. 7b presents a plot of ln(J) with respect to the square root of the applied voltage ($V^{1/2}$). For standard Schottky–Richardson (SR) emission, the plot of ln(J) versus $V^{1/2}$ should be linear; which can be expressed as [29]:

$$J = A^{*}T^{2} \exp\left[\frac{-q(\phi_B - \sqrt{qV/4\pi\varepsilon d})}{KT}\right]$$

where A^* was the effective Richardson constant, ϕ_B was barrier height, ε was the dynamic electric permittivity, and d was the thickness of the dielectric layer. The plot between ln(J) and $V^{1/2}$ demonstrated a linear behavior under negative bias. Thus, due to the fact that the conduction mechanism of the MIS device is Schottky emission, this device had threshold voltage which blocked the leakage current through insulator layer. SR emission induced by the thermionic effect was caused by electron transport across the potential energy barrier, as indicated in the inset of Fig. 7b; it was independent of traps and dominates the conduction mechanism.

Fig. 8 displayed capacitance–voltage (C–V) measurements for TiO_2 films for as deposited then baked at 80 °C for 5 min and after annealed at 270 °C for 5 h. As viewed by inset of Fig. 8, the capacitance for as deposited then baked TiO_2 film at 1 MHz was very low. Reasonable capacitance was not observed, which means the property could not afford to minimum requirement of MIS devices. On the contrary, good capacitance characteristic in Fig. 8 was obtained for device with film annealed at 270 °C in O_2 ambient for 5 h. According to the capacitance and thickness data, we obtain the dielectric value of the annealed sample of nc-TiO_2 film for specific area. The capacitance, C_{MIS} is calculated analogously to the plate capacitor [30].

$$C_{MIS} = \varepsilon_0 k \cdot \frac{A}{d}$$

where, k was the insulator's dielectric constant, ε_0 was the permittivity of the vacuum, A was the area, d was the thickness of insulator layer. For specific area (0.01 mm^2),

Table 1
Comparison of various TiO_2 film deposition methods (dip-coating, atomic layer deposition/ALD, spin-coating, chemical vapor deposition/CVD, liquid phase deposition/LPD and sputtering) with respective to thickness, dielectric constant, leakage current, substrate type and growth temperature.

Reference	Deposition process	Film thickness (nm)	Dielectric constant[a]	Leakage current density (A/cm^2)	Temperature (°C)	Substrate
This work	Dip-coating	25	28.8	8.7×10^{-12}	270	Polyimide
[24]	ALD	70	83	10^{-6}–10^{-8}	250	Silicon
[25]	Spin-coating	70	23	10^{-9}–10^{-10}	700	Silicon
[26]	CVD	50	50	5.0×10^{-5}	600	Silicon
[27]	LPD	73	29.5	1.1×10^{-6}	450	Silicon
[28]	Sputtering	15.5	22	2.8×10^{-6}	350	Silicon

[a] Calculated from equation $C_i = \varepsilon_0 kA/d$ (where k is the dielectric constant, ε_0 the vacuum permittivity, A the capacitor's surface area and d the insulator thickness).

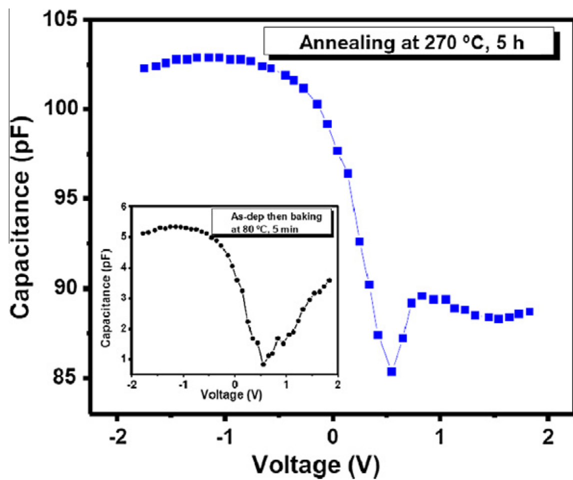

Fig. 8. C–V plot for MIS structures fabricated with nc-TiO_2 as dielectric film and pentacene as semiconductor layer: inset shows C–V plot for as-deposited sample.

thickness of TiO_2 layer (25 nm) and maximum capacitance (102.3 pF), the calculated dielectric constant was 28.8. This calculated value of k was lower than the standard k-value of TiO_2, but the obtained dielectric constant was consistent with previous published dielectric constant for TiO_2 on silicon substrate [27,31,32]. In Table 1, the dielectric constant obtained from our nc-TiO_2 film deposited over PI by dip-coating process was similar and equivalent to some of TiO_2 films deposited over silicon substrate. We expected that the good capacitance and high k-value for our flexible MIS device by using TiO_2 as dielectric layer would allow future flexible nanoelectronic devices to be operated in the low voltage and low temperature regime.

3.7. Real-life flexibility tests

We estimated the leakage current density for sample treated with annealing (270 °C, 5 h) in different convex and concave types of bending stages to confirm the possibility for using in advanced flexible electronic devices during real life operation. During the manufacturing process, a foil was used to provide these specific bending structures. Both convex (Fig. 9a) and concave (Fig. 9b) settings were measured, and the radii of curvature (denoted by R_c) were varied from 1.5 to 4.0 cm. Fig. 9 revealed the corresponding current density with respect to radius of curvature from 4.0 to 1.5 cm for the device. All of the bending conditions

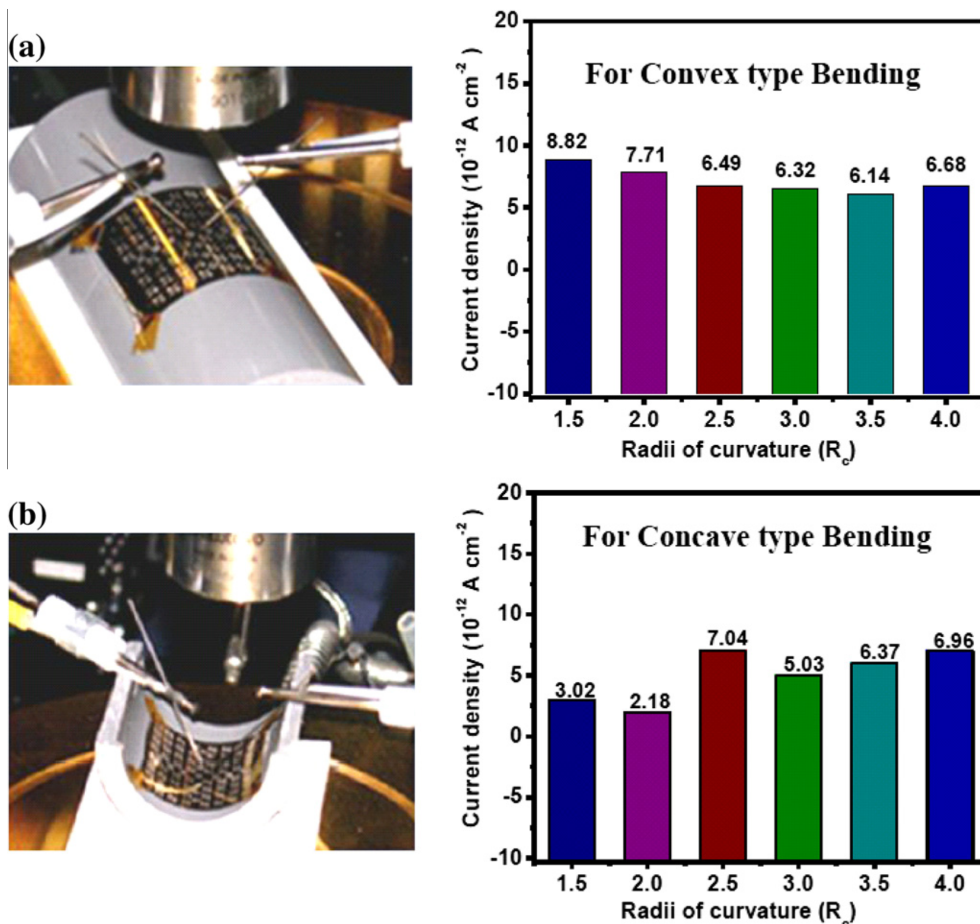

Fig. 9. Plots for J-R_c measurement from our MIS device fabricated with nc-TiO_2 film; (a) convex shape test, and (b) concave shape test.

exhibited the lowest leakage current densities were found to be about 10^{-12} A cm^{-2} at applied voltage of 0–5 V under stressing of negative biasing conditions. The soft device retained its low leakage current density even under the most bending condition of radius of curvature of 1.5 cm. In convex type bending shape (Fig. 9a), only a minor change was measured among different bending curvatures, but this subtle variation is still acceptable. We also measured the current density for radius of curvature from 1.5 to 4 cm in concave stages as shown in Fig. 9b. Again, we observed the lowest leakage current densities under negative biasing conditions for TiO_2–Au/Cr/PI substrate, which were about 10^{-12} A cm^{-2} at 0–5 V.

As PI sheet was bent into convex and concave shapes, the outer surface experienced a tensile strain and the inner surface experienced a compressive strain [2]. During device for convex case, MIS device located on the PI surface suffered tensile strain. In contrast, the device on PI surface suffered compressive strain while concave case. The observed strain effect for MIS device on PI exhibited according to the shift direction of substrate. Thus for many flexible electronic devices, the induced strain could be calculated by the following simple approximation of the relationship between film strain of MIS device (ε_{MIS}) and radius of curvature [33,34],

$$\varepsilon_{MIS} = \frac{t}{2R_c}$$

where t was the thickness of the substrate and R_c was the radius of curvature. The maximum strain was estimated to be 0.126% for MIS device on PI substrate of thickness of 38-μm under an extreme curvature (R_c) of 1.5 cm. At this strain value, our MIS device functioned well without any failure mode. We observed that our flexible MIS device was exceptionally stable against various bending stresses and were bendable, rollable, wearable and foldable; demonstrating no deteriorated effect at maximum tensile strain of 0.126%. In addition, the device fabricated from dip–coating, where nc-TiO_2 film was dielectric layer and pentacene was semiconductor layer, exhibited very stable electrical properties.

After the success of bending test in convex and concave type stages, we also performed a folding test as shown in Fig. 10. To observe the foldable behavior of our flexible MIS device, a fabricated flexible array containing 80 MIS devices patterned on an area of 5 × 5 cm^2. This flexible array was repeatedly crumpled within the palm of the hand, and sequential folding images were depicted in Fig. 10. A portion of flexible MIS device restored its initial electrical performance after crumpled within the palm of the hand for number of times. Even during this severe mechanical stress, about 50% devices operated well with high durability (c.a. 30 days). Some failed devices after mechanical test were attributed to the cracking of the electrode, semiconductor film or insulator film. This test confirmed the developed technique can fabricate the soft device from the simple and cost-effective dip-coating process. The real life test for flexible devices opened up further application in future electronic field.

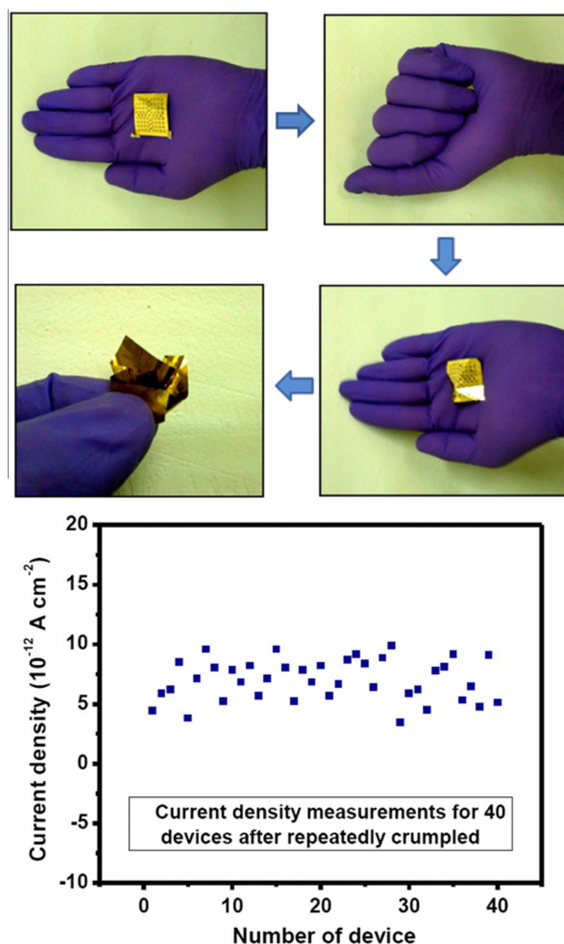

Fig. 10. Demonstration of the foldable test, one array of flexible MIS devices repeatedly crumpled in the palm of a hand, and the current density measurement for 40 devices.

4. Conclusion

We successfully fabricated a fully bendable, dip-coated and solution-processed nc-TiO_2 thin film based MIS device over flexible PI sheet. The triblock copolymer P123 was used as a uniform-structure-directing agent for TiO_2 film formation. Various analytical methods such as XRD, AFM, XPS and electrical characterization confirmed that the unprecedented flexibility of the device from solution-deposited dip-coating process. For the prepared nc-TiO_2 thin film surface, over five cycles of continuous wetting and drying were used to measure the contact angle to further explore applications such as antifogging, self-cleaning, antibacterial and stain-proofing agents in advanced nanoelectronics. Our flexible MIS device was exceptionally stable against various bending stresses and is bendable, rollable, wearable and foldable for waiting period of 30 days; demonstrated no degradation at tensile strains up to 0.126%. Thus, the MIS device on flexible PI substrate exhibited high dielectric constant, low leakage current and good capacitance, which is sufficient for the future practical applications. It should be noted that this dip-coating

solution process was effective to MIS devices and demonstrated the production capability for low-temperature and large-area flexible electronic devices.

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