Proportional Compensated Buck Converter With a Differential-In Differential-Out (DIDO) Error Amplifier and Load Regulation Enhancement (LRE) Mechanism

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***Abstract*—A differential-in differential-out error amplifier and a load regulation enhancement mechanism are proposed in the buck converter that aims to improve load regulation and noise immunity. By using the proportional compensator in the proposed converter, there is no need of external compensation components in this design. As a result, a compact-size and high-performance dc–dc buck converter can be guaranteed. Experimental results show that load regulation can be improved from 0.5 to 0.025 mV/mA. The test chip was fabricated by 0.25 μm CMOS process and occupied 1.65 mm^2 active silicon area.**

***Index Terms*—Current-mode operation, dc–dc converter, differential-in differential-out (DIDO) amplifier, load regulation, system compensation.**

I. Introduction

In recent years, portable devices involve several integrated chips (ICs) with different functionality into the same printed circuit board (PCB) for achieving various functions. It needs a highly integrated power-management module to reduce the volume and weight in order to keep up with the trend of compact size. Unfortunately, the off-chip inductor and capacitors for the high-efficiency switch-mode dc–dc converters occupy the large PCB area, which results in the extra manufacture cost and the problem for system-on-a-chip (SoC) integration. In addition, the parasitic inductive or capacitive coupling path generated from the bonding wire forms a harmful interference, which can be eliminated by integrating the off-chip components as many as possible. In other words, a highly integrated power-management module is necessary for achieving high performance and small footprint area in today's power-management design.

Fig. 1 shows the structure of a conventional current-mode buck converter. A differential-in and single-ended (DISO) error amplifier with high gain aims to obtain better regulated output voltage compared to the control only with a comparator.

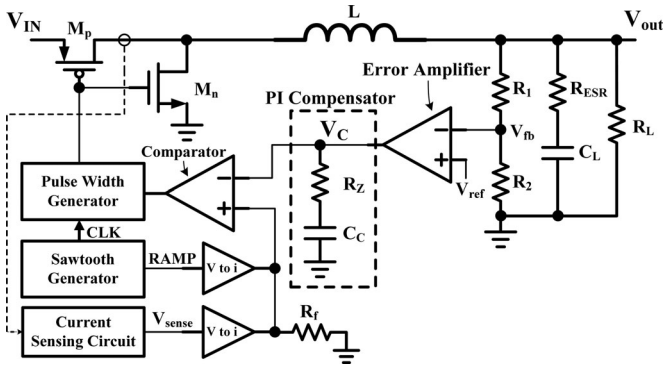

Fig. 1. Conventional structure of a current-mode control buck converter.

However, the characteristic of high gain in the DISO error amplifier needs to be compensated by the *RC* filter, which can contribute a large time constant. Generally speaking, the *RC* filter is composed of a compensation resistor R_Z and a compensation capacitor C_C in series to generate a pole–zero pair for achieving proportional-integral (PI) compensator. These implementations can stabilize the current-mode buck converter to provide a constant output voltage with high-efficiency power conversion. However, owing to the current-mode operation, the system pole of the current-mode buck converter can be varied according to the different output load conditions. Thus, to fit the worst case of the load condition, the compensation components R_Z and C_C must be implemented with large values, which is hard to be integrated into a chip. That is to say, the increase in the expense of a power-management module can lead to the less attractive utilization in portable applications due to the large compensation components integration.

Nevertheless, some prior arts can integrate the compensation components into the chip by using the current-operated miller capacitance method [1]–[3]. It can magnify a small on-chip compensation capacitor into a large one for ensuring the system stability. As a result, the number of external pins and compensation components can be decreased for achieving a compact-size solution. Moreover, the compensation resistance of the PI compensator proposed in [1] can be dynamically adjusted according to the different output load conditions. Thus, the dynamic compensation scheme carries out the smooth soft start and fast transient response, simultaneously. However, the implementation of the capacitor multiplier technique still needs the compensation

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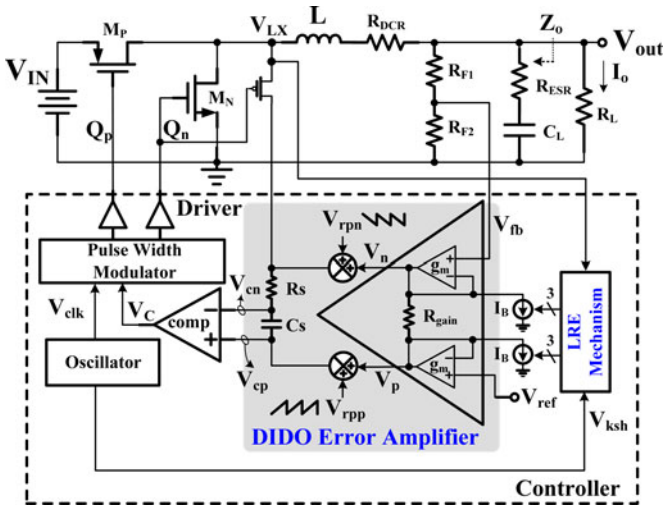


Fig. 2. Architecture of the proposed buck converter with the LRE mechanism.

network with an on-chip small-size capacitor and medium-size resistor, respectively. The overall power dissipation of the mechanism is large in order to sustain a wide stable operation of the system. In addition, the offset and noise problem have an impact on the performance of the capacitor multiplier technique that must be designed carefully. To simultaneously eliminate large volume-compensation components and maintain the system stability, this paper presents a differential-in differential-out (DIDO) error amplifier with a proportional (P) compensator to operate a current-mode buck converter, which aims to achieve the fast transient response and the stable operation without the need of any system-compensation components [4], [5]. Moreover, the load regulation enhancement (LRE) mechanism is proposed to enhance the regulation performance. Consequently, the compact size and enhanced load regulation in the dc–dc current-mode buck converter can be achieved at the same time to meet the requirement of high-quality portable devices.

The organization of this paper is as follows. The system operations containing the DIDO error amplifier and the concept of the LRE mechanism for improving poor load regulation are illustrated in Section II. The frequency response in the proposed current-mode buck converter with the P compensator is introduced in Section III. Besides, the transfer function derived by the mathematic tool MATLAB can prove the stable system operation based on the proposed DIDO error amplifier. Circuit implementation of the DIDO error amplifier and the LRE mechanism are described in Section IV. The measurement results of the proposed converter are shown in Section V. Finally, a conclusion is made in Section VI.

II. System Operation

Fig. 2 shows the architecture of the proposed current-mode buck converter with the DIDO error amplifier and the LRE mechanism. To eliminate the compensation components, the DIDO error amplifier with low-gain structure is used to replace the work of the high-gain DISO error amplifier in the conventional current-mode buck converter. The output voltage condition can react to the DIDO error amplifier through the voltage divider, i.e., R_{F1} and R_{F2}. The voltage difference between the feedback voltage V_{fb} and the reference voltage $V_{\rm ref}$ is amplified by the DIDO structure to generate the differential error signals, i.e., V_p and V_n. Owing to the DIDO structure, the switching noise coupled from the voltage divider at the output node can be filtered out easily. Thus, a nearly noiseless error signal is derived through this structure. In addition, the compensation ramp signals must be differentially added to the positive and negative outputs of the DIDO amplifier to achieve the slope compensation. That is, a pair of differential ramp signals V_{rpp} and V_{rpn} is added to V_p and V_n, respectively, to suppress the subharmonic oscillation in the current-mode control. The current-sense circuit is easily implemented by using the small on-chip R_S and C_S. The resistor R_s and the capacitor C_s are connected between the V_{LX} and the output of the DIDO amplifier to yield the current sensing signal. In addition, the LRE mechanism circuit will sense the inductor current to obtain the output load condition to ensure the output voltage regulation. The sensing operation is controlled through the sampling phase signal V_{ksh}. Moreover, the comparator can decide the control duty V_C through the differential signal V_{cp} and V_{cn}. Finally, the pulse width modulator and driver generate the control signals Q_p and Q_n to achieve the energy distribution at power stage to transfer energy from $V_{\rm IN}$ to $V_{\rm OUT}$.

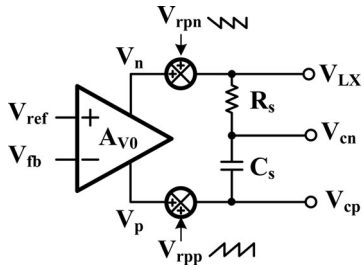


Fig. 3. Simplified structure of a DIDO amplifier.

The simplified structure of the DIDO amplifier with the current sensing function is shown in Fig. 3. The low-frequency gain of the DIDO error amplifier is defined as A_{V0}. The value of A_{V0} is set to a low value considering the stability of the system. This part would be discussed in Section III. Neglecting the slope-compensation ramp voltages, the differential error signals V_{cp} and V_{cn} can be depicted in (1) and (2), respectively. The DIDO error amplifier would carry out an error signal variation Δv shown in (3) through the voltage gain A_{V0} and the voltage difference between $V_{\rm ref}$ and V_{fb}:

$$V_{cp} \cong V_p - \Delta v \tag{1}$$

$$V_{cn} \cong V_{LX} + \Delta v \tag{2}$$

where

$$\Delta v = A_{V0}(V_{\rm ref} - V_{fb}). \tag{3}$$

The two error signals V_{cp} and V_{cn} will be sent to the input of the comparator to generate the duty cycle for the regulation of output voltage. However, the values of V_{cp} and V_{cn} cannot be forced to be approximately equal by the negative feedback

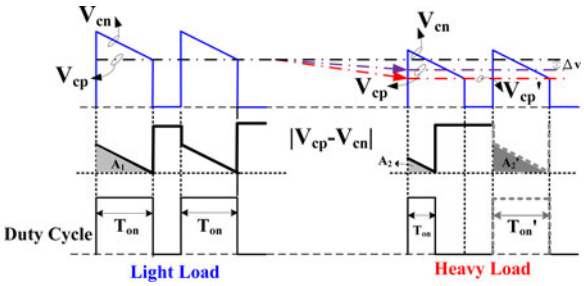


Fig. 4. Steady-state waveforms of V_{cp} and V_{cn} and duty cycle under different load conditions.

control owing to the low gain of the DIDO amplifier. As a result, the difference voltage between V_{cp} and V_{cn} should be considered and expressed as

$$V_{cp} - V_{cn} \cong V_p - V_{LX} - 2\Delta v. \tag{4}$$

Assuming that the on-resistance of the high-side power MOSFET, i.e., $R_{DS(\mathrm{ON})}$, is almost unchanged under different load conditions, then the slope of $|V_{cp}-V_{cn}|$ in Fig. 4 can be kept with a constant value during the on-time period T_{on}. Besides, the area A_1 should be kept with a constant value since the duty cycle is unchanged between different load conditions. However, the dc level variation of V_{cn} is derived from V_{LX}, which has slight voltage variation resulted from the different load conditions owing to the constant $R_{DS(\mathrm{ON})}$ resistance of the power MOSFET. Besides, when the load transient response occurs, the dc level variation of V_{cp}, which is represented by the small signal voltage Δv depicted in (4), is merely small due to the low-gain structure of the proposed DIDO amplifier. That is, V_{cp} is varied within a small range under the different load conditions as shown in Fig. 4. As a result, the duty cycle will decline obviously when the load current changes to the high current conditions. It results in that the area A_1 derived under a low load current condition is unequal to the area A_2 derived under high load current condition so as to cause poor voltage regulation performance. Fortunately, the proposed LRE mechanism can help redeem this problem. As shown in Fig. 4, the differential error signal V_{cp} can be adjusted to V'_{cp} at the high load current condition through the LRE mechanism. Thus, the area A'_2 can be equal to A_1. Both the duty cycle and the on-time period can be kept as of the same value at the different output load condition. That is, the LRE mechanism can roughly adjust the dc level of the signal V_{cp} to form the rough duty cycle modulation according to the load condition, and the low-gain DIDO error amplifier can be used to achieve a fine duty cycle modulation.

With the proposed low-gain DIDO error amplifier, the output voltage V_{out} of the current-mode buck converter can be approximated as (5) based on the basic negative feedback control:

$$V_{\mathrm{out}} \approx V_{\mathrm{ref}}\frac{1}{\beta} - I_o Z_o, \quad \text{where} \quad Z_o = \frac{Z_{o(\mathrm{open-loop})}}{1 + A_{V0}\beta} \quad \text{and}$$
$$\beta = \frac{R_{F2}}{R_{F1} + R_{F2}}. \tag{5}$$

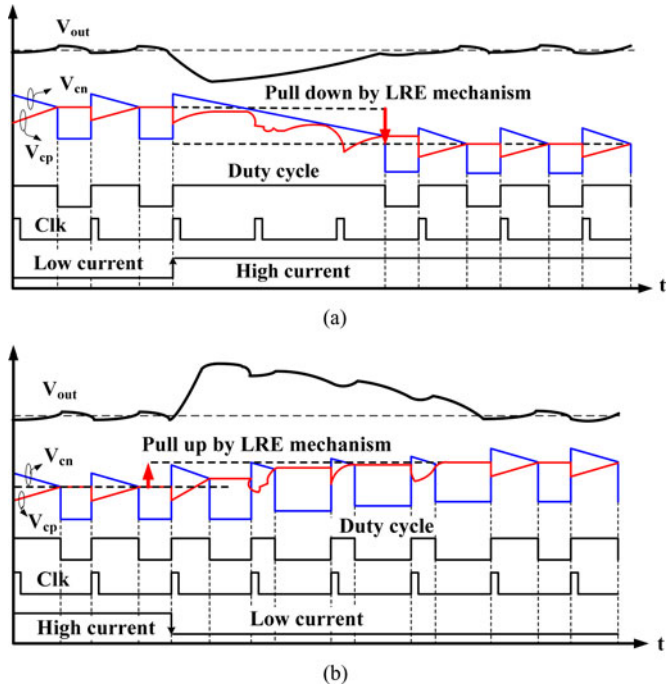


Fig. 5. Load transient response with the LRE mechanism. (a) Load current changes from low to high current. (b) Load current changes from high to low current.

Obviously, the second term in the aforementioned equation is considered as the voltage droop when load current increases. In the conventional buck converter design, the value of A_{V0} is usually large enough to eliminate the effect of closed-loop output impedance Z_o on V_{out}. However, the high dc loop gain in the conventional buck converter increases the volume and complexity of compensation network and occupies a large footprint area. As a result, there is a tradeoff between the volume of compensation network and the load regulation. The proposed LRE mechanism is used to improve the load regulation without the need of a large compensation network for minimizing the silicon area. It can enhance the load regulation performance in the case of load current variation and guarantee the system stability at the same time. That is, the LRE mechanism can keep the voltage difference derived in (4) as a constant value under different load conditions, which can be regarded as the compensation of a low-gain DIDO error amplifier for good load regulation.

The timing diagram in Fig. 5 can depict the operation concept of the proposed LRE technique. In Fig. 5(a), V_{out} drops in the beginning of the load transient response when the load current changes from low to high current. Owing to the characteristic of a low-gain DIDO error amplifier, the voltage variation of the error signal V_{cp} is small, which is inadequate to generate a sufficient duty cycle. Therefore, the LRE mechanism can help pull down the value of V_{cp} to maintain the system duty cycle as well as the output voltage level of the current-mode buck converter. Consequently, V_{out} can be regulated with a proper load regulation performance. Similarly, if the load current changes from high to low current, the LRE mechanism shown in Fig. 5(b) can pull up V_{cp} to derive the proper system duty cycle that would

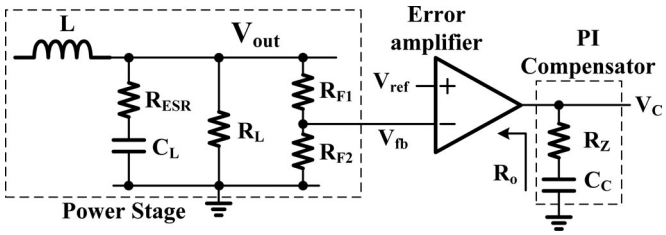


Fig. 6. Power stage in the conventional buck converter compensated by the PI compensator.

enhance load regulation of the buck converter. As a result, the combination of the DIDO error amplifier and the LRE mechanism can ensure the voltage regulation performance at the output node of a buck converter and eliminate the implementation of system-compensation components, simultaneously.

III. System Stability Analysis

A. PI Compensator in a Conventional Current-Mode Buck Converter

In conventional current-mode buck converter design, the PI compensator is commonly used to assure the system stability. Fig. 6 shows a simple sketch of the power stage in a buck converter with feedback resistors and error amplifier. The PI compensator is implemented at the output node of the error amplifier and produces a pole–zero pair to stabilize the system. The pole ω_{P1} generated by the compensation capacitor C_C and the large output impedance R_o of the error amplifier contribute the dominant pole of the system. In addition, the zero ω_Z derived from the compensation capacitor C_C and the compensation resistor R_Z is utilized to cancel the output pole ω_{PL} at the output node. The location of ω_{P1}, ω_Z, and ω_{PL} can be expressed as

$$\omega_{P1} \approx \frac{1}{C_C R_o}, \quad \omega_Z = \frac{1}{C_C R_Z}, \quad \text{and} \quad \omega_{PL} \approx \frac{1}{C_L R_L}. \tag{6}$$

Owing to the existence of a low-frequency dominant pole ω_{P1}, the low-frequency system loop gain can be designed high to achieve good voltage regulation, as well as adequate system crossover frequency. However, the exact location of pole–zero cancellation, achieved by ω_Z and ω_{PL}, would be distinct at different load conditions since ω_{PL} is a system's load-dependent pole. Therefore, the compensation components R_Z and C_C must be designed to a larger value in order to meet the worst condition, which is the low load current condition in the current-mode buck converter. In addition, the equivalent series resistance (ESR) on the output capacitor can contribute a high-frequency zero $\omega_{\rm esr}$ as shown in (7). Another system pole ω_{PL2} related to both the slope of compensation ramp and the switching frequency is also derived at high frequency [6]–[9]. Fortunately, the zero and pole are located over the system's crossover frequency that would have no influence on system stability:

$$\omega_{\rm esr} \approx \frac{1}{C_L R_{\rm esr}}. \tag{7}$$

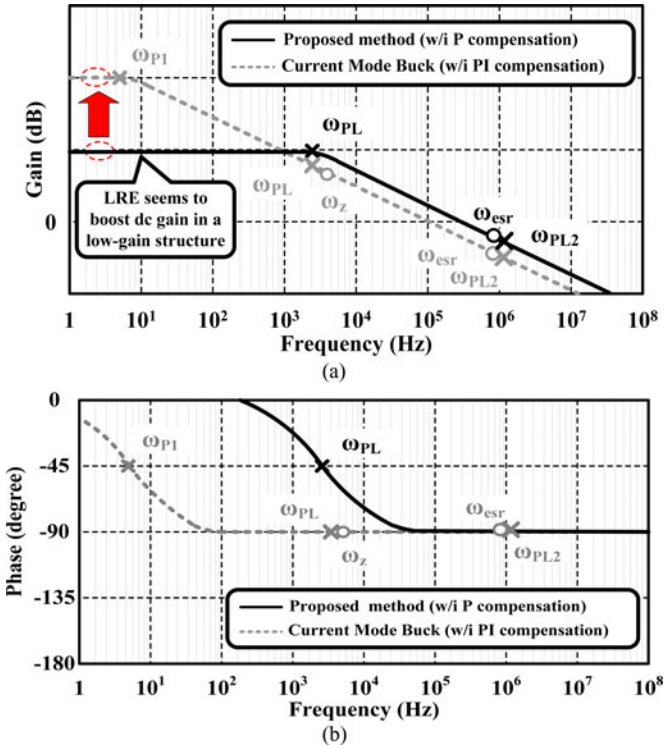


Fig. 7. Open-loop transfer function's comparative Bode plot between the buck converter with the PI compensator and the buck converter with the P compensator. (a) Magnitude. (b) Phase.

B. Stability Illustration in the Proposed Work

To eliminate the use of system-compensation components, the DIDO error amplifier with the LRE mechanism is proposed to achieve the stable system operation, as well as the good output voltage regulation. The system output pole ω_{PL} depicted in (6) is regarded as the system dominant pole without the need of any low-frequency poles and zeros in the proposed design. Thus, the implementation of the DIDO error amplifier can be considered as the P compensator. Since ω_{PL} is higher than the pole ω_{P1} generated by the PI compensator, the low-frequency loop gain of the proposed converter cannot be designed with a high value considering the system stability. Thus, the DIDO error amplifier is implemented with low voltage gain to ensure system stability, but sacrifice the performance of voltage regulation. As a result, the proposed LRE mechanism is utilized to enhance the regulation performance of the proposed converter. As depicted in Fig. 7, it is obvious that the low-frequency gain of the open-loop transfer function with the P compensator is lower than that with the PI compensator. The usage of the P compensator removes the need of large size compensation components but suffers from poor load regulation. Therefore, the LRE mechanism targets to compensate the low dc gain as depicted in Fig. 7 to enhance the poor load regulation caused by low dc gain. That is, LRE can achieve the common-mode adjustment in the outputs of the DIDO error amplifier according to the output load conditions for enhancing the load regulation. This operation seems to boost the dc gain of the proposed low-gain structure as the illustration in Fig. 4. As a result, the proposed LRE mechanism can meet

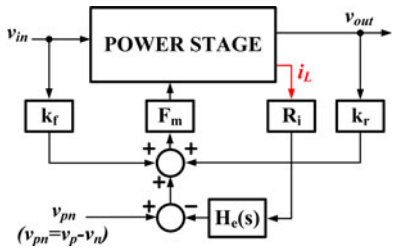


Fig. 8. Equivalent small-signal model of the current-mode buck converter.

the requirement of load regulation and achieve the compact size solution, simultaneously.

C. Small-Signal Analysis

The small-signal model of the proposed current-mode buck converter is shown in Fig. 8. R_i is the linear gain of the current sensing network. In addition, the current-sampling operation in the current-mode control can be modeled as a second-order continuous transfer function $H_e(s)$ as expressed in (8) [6]. Thus, R_i will be multiplied by $H_e(s)$ for representing the current feedback. Moreover, the remaining gain factors of the proposed buck converter are illustrated in (9). The feedback gain factors of k_f and k_m are created when the current feedback loop is closed. These two gain factors yield the feedforward of the voltages across the inductor during the on-time and off-time of the converter, respectively. F_m is the modulator gain for the duty cycle realization. T_S and D are the switching period and the duty cycle, respectively. The parameter S_n is the slope of the compensation ramp and S_e indicates the on-time slope of the current sensing waveform:

$$H_e(s) = 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \quad \text{where} \quad \omega_n = \frac{\pi}{T_s}, \quad Q_z = \frac{-2}{\pi} \tag{8}$$

$$k_f = -D\frac{R_i T_s}{L}[1 - 0.5D], \quad k_r = \frac{R_i T_s}{2L}$$

and

$$F_m = \frac{1}{(S_n + S_e)T_s} = \frac{1}{m_c S_n T_s} \quad \text{where}$$

$$m_c = 1 + \frac{S_e}{S_n}. \tag{9}$$

As a result, the simplified control-to-output transfer function $G_{vc}(s)$ for the proposed current-mode buck converter is given as

$$G_{vc}(s) = \frac{v_{\text{out}}}{v_{\text{pn}}} \cong \frac{R_L}{R_i} \cdot \frac{1}{1 + (R_L \cdot T_s/L)\,[m_c D' - 0.5]} \cdot F_p(s) \cdot F_h(s) \tag{10}$$

where

$$F_p(s) = \frac{1 + sC_L R_C}{1 + (s/\omega_p)}$$

and

$$\omega_p = \frac{1}{R_L C_L} + \frac{T_s}{LC_L}(m_c D' - 0.5) \tag{11}$$

$$F_h(s) = \frac{1}{1 + (s/\omega_n Q) + (s^2/\omega_n^2)}$$

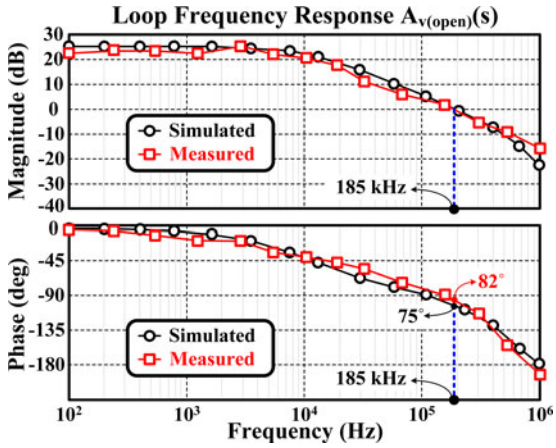


Fig. 9. Loop frequency response of $A_{v\,(\text{open})}$ including both simulated and measured results.

where

$$Q = \frac{1}{\pi(m_c D' - 0.5)}. \tag{12}$$

Here, $F_p(s)$ includes the system's dominant pole ω_p, which is produced by the load resistance R_L, output capacitor C_L, inductor L, switching period T_S, and the complement of the duty ratio D' as shown in (11). Besides, the zero is formed by the ESR R_c and the output capacitor C_L. $F_h(s)$ manifests the current sensing behavior in the current feedback loop [6] as depicted in (12). The slope of the compensation ramp m_c can control the value of Q with a small value in order to reduce the high peaking effect. It can prevent the subharmonic oscillation problem at the power stage when the system duty cycle exceeds the half of the switching period.

The open-loop transfer function of the proposed buck converter $A_{v\,(\text{open})}$ can be expressed as

$$A_{v(\text{open})} = \beta G_{vc}(s) G_{\text{com}}(s). \tag{13}$$

Here, β is the sensor gain determined by the voltage divider. $G_{\text{com}}(s)$ indicates the transfer function of the P compensator. In the design of the P compensator, the transfer function $G_{\text{com}}(s)$ contributes a constant voltage gain without any poles or zeroes in the low-frequency range. Thus, the definition of $G_{\text{com}}(s)$ can be shown as follows:

$$G_{\text{com}}(s) = G_{\text{com}0}. \tag{14}$$

As the consideration of system stability, there is a tradeoff between the value of $G_{\text{com}0}$ and the phase margin. A large value of $G_{\text{com}0}$ may deteriorate the system phase margin due to the existence of the high-frequency complex poles near the crossover frequency. However, a lower value of $G_{\text{com}0}$ may derive a poor load regulation performance at output. Therefore, the value of $G_{\text{com}0}$ would have influence on the performance of load regulation and the system stability. To attain an adequate system phase margin, $G_{\text{com}0}$ should be carefully designed to guarantee the system stability for achieving good transient response.

The loop frequency response $A_{v\,(\text{open})}$ is shown in Fig. 9. With the parameters listed in Table I for demonstrating the work

TABLE I.
PARAMETERS IN THE OPEN-LOOP TRANSFER FUNCTION

R	3.6 Ω	R_i	0.2 Ω
T_s	1 μs	L	4.7 μH
C	10 μF	R_C	30 mΩ
D	1.8/3.3	m_c	2.2

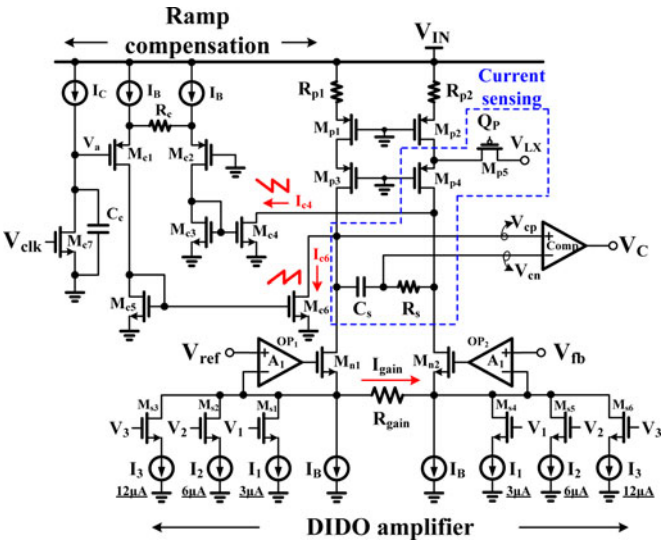


Fig. 10. Proposed DIDO error amplifier and the slope-compensation circuit.

of P compensator, the value of $G_{\mathrm{com}0}$ in the proposed design is chosen as the factor of 4. Both the simulated and the measured results of the loop frequency response can guarantee the stable operation owing to the adequate system phase margin. However, the small value of $G_{\mathrm{com}0}$ would result in the poor voltage regulation performance at output that is necessary to compensate through the utilization of the LRE mechanism. Fortunately, the small-signal model still remained since the LRE mechanism is used to modulate the bias current of the DIDO error amplifier. Consequently, the parameters in the small-signal model can be easily designed and has no effect of using the LRE mechanism.

IV. CIRCUIT IMPLEMENTATION

A. DIDO Error Amplifier With the Slope-Compensation Circuit

The proposed DIDO error amplifier and the slope-compensation circuit are shown in Fig. 10 to generate the system control signal and avoid the subharmonic oscillation, respectively. The slope-compensation circuit is composed of the transistors M_{c1}–M_{c7}, the resistor R_c, and the capacitor C_c. During the inductor charging period, the constant current I_C would charge the capacitor C_c and thus the voltage at V_a can be raised. Therefore, the voltage difference between the gates of transistors M_{c1} and M_{c2} will generate a current through the auxiliary resistor R_c. It causes the current flowing through M_{c4} and M_{c6} to have the saw-tooth waveform in the opposite direction, which can be added to the DIDO amplifier for avoiding the subharmonic oscillation.

The DIDO error amplifier carries out a small-signal current I_{gain} from the reference signal V_{ref} and the feedback signal V_{fb} through the use of operational amplifiers and flying resistor R_{gain}. Thus, the transconductance of the proposed DIDO amplifier is expressed as

$$G_m = \frac{1}{R_{\mathrm{gain}}}. \tag{15}$$

In addition, the output resistance at V_{cp} of the DIDO error amplifier is related to the aspect ratio of transistors M_{p1}–M_{p4} and the voltage gain of the operational amplifier A_1. Therefore, the voltage gain of the proposed DIDO amplifier is expressed as

$$A_{v,\mathrm{DIDO}} = G_m\left[(A_1 g_{m,Mn1} r_{o,Mn1} r_{o,I_B})\|(R_{p1} + R_{Mp1} + R_{Mp3})\right]. \tag{16}$$

The parameters $g_{m,Mn1}$ and $r_{o,Mn1}$ are the transconductance and the output resistance of M_{n1}, respectively. $r_{o,IB}$ is the output resistance of the current source I_B. R_{Mp1} and R_{Mp3} are the equivalent resistances of the transistors M_{p1} and M_{p3}, respectively.

When the voltage difference is derived from the reference voltage V_{ref} and the feedback signal V_{fb}, the two output voltages of the DIDO error amplifier V_{cp} and V_{cn} can be expressed as (17) and (18) with the neglect of the slope-compensation signal, respectively. The voltage difference between V_{cp} and V_{cn} and the voltage variation Δv on both V_{cp} and V_{cn} are shown in (19):

$$V_{cp} \cong V_{\mathrm{IN}} - I_B(R_{p1} + R_{\mathrm{on},M_{p1}} + R_{\mathrm{on},M_{p3}}) - \Delta v \tag{17}$$

$$V_{cn} \cong V_{LX} - I_B(R_{\mathrm{on},M_{p4}}) - \Delta v = (V_{\mathrm{IN}} - I_L R_{\mathrm{on},P}) - I_B R_{\mathrm{on},M_{p4}} + \Delta v \tag{18}$$

$$V_{cp} - V_{cn} \cong I_L R_{\mathrm{DS(ON)}} - I_B R_{eq} - 2\Delta v$$

$$\text{where} \quad R_{eq} = R_{p1} + R_{\mathrm{on},M_{p1}} \quad \text{and}$$

$$\Delta v = A_{v,\mathrm{DIDO}}(V_{\mathrm{ref}} - V_{fb}). \tag{19}$$

Here, I_L is the value of inductor current and $R_{DS(\mathrm{ON})}$ is the on-resistance on high-side on-resistance of the high-side power MOSFET. The difference of V_{cp} and V_{cn}, $|V_{cp}-V_{cn}|$ helps derive the inductor current information for the duty cycle determination. Moreover, $|V_{cp}-V_{cn}|$ is independent of the supply voltage V_{IN} since the effect of input voltage variation can be naturally eliminated by the proposed DIDO error amplifier structure.

On the other hand, unlike the conventional structure using the high-gain error amplifier to obtain good line transient response, the DIDO error amplifier structure can properly suppress the disturbance from input. As the detailed circuit shown in Fig. 10, the variation from the supply voltage V_{IN} can be eliminated by the DIDO amplifier. That is, the V_{IN} variation can be regarded as the common-mode signal for the comparator's input, and that will not affect the result on the signal V_C for duty determination,

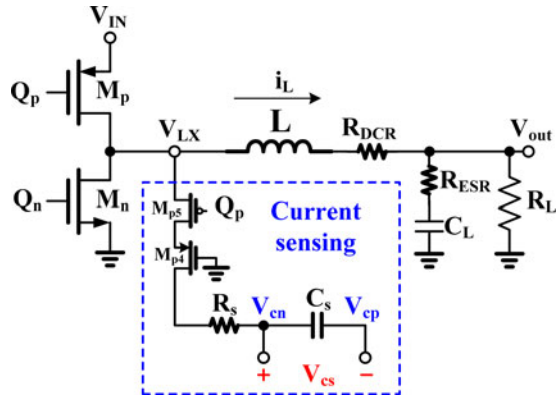


Fig. 11. Current sensing circuit.

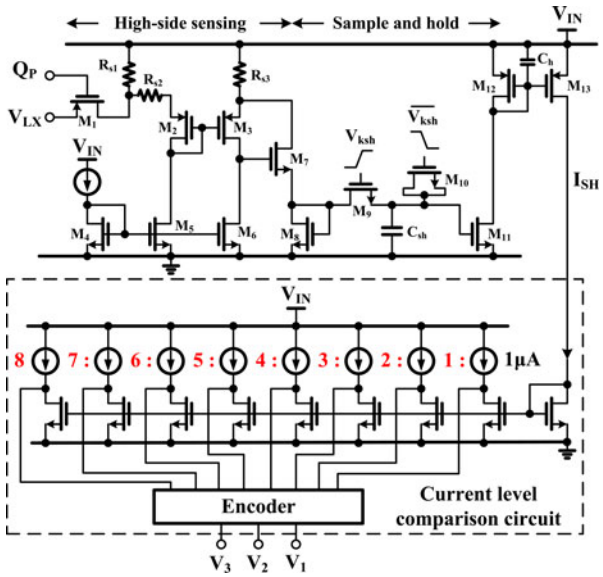
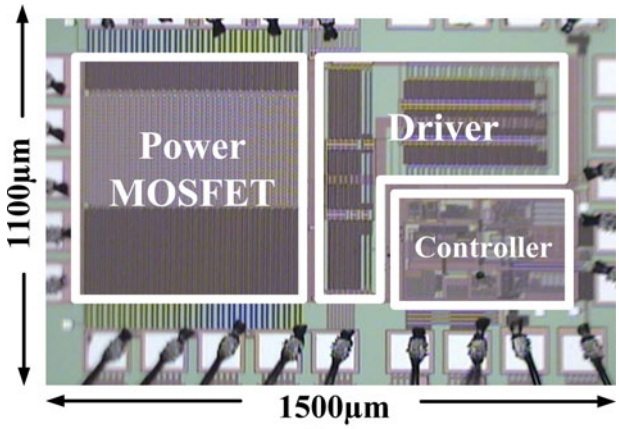


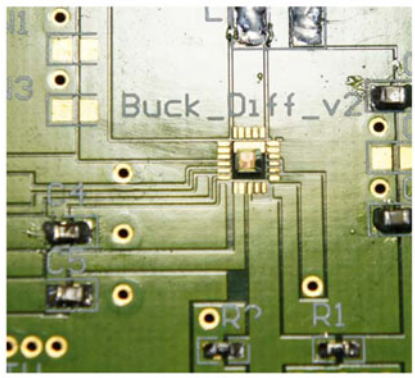
Fig. 12. LRE mechanism circuit.

so as to obtain the good line transient response. Moreover, the sensitivity of the reference voltage and the output voltage is mainly affected by the offsets from operational amplifiers OP_1 and OP_2 in Fig. 10, and the layout matching of the DIDO amplifier. Thus, the trimming method can be used to ensure the circuit matching of the DIDO amplifier as well as compensate the unwilling offset about 30 mV from the operational amplifiers in the 0.25 μm process by adjusting the resistor values of R_{p1} or R_{p2} in the DIDO amplifier.

As the illustrations depicted in Section II, the voltage difference between V_{cp} and V_{cn} must be a constant value under different load conditions in order to obtain the good voltage regulation. Nevertheless, the DIDO error amplifier with low voltage gain is inadequate to ensure the constant voltage difference between V_{cp} and V_{cn}. As a result, the LRE mechanism is proposed to maintain the output voltage regulation through the adjusting of current sources I_1, I_2, and I_3.

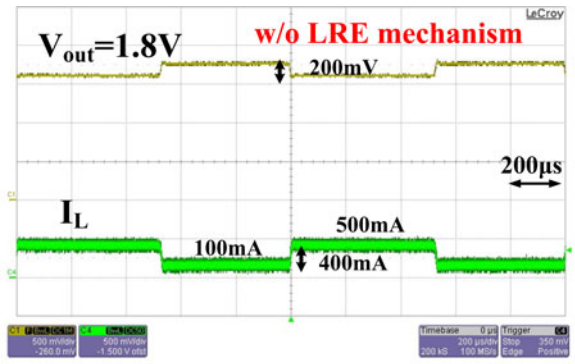


(a)

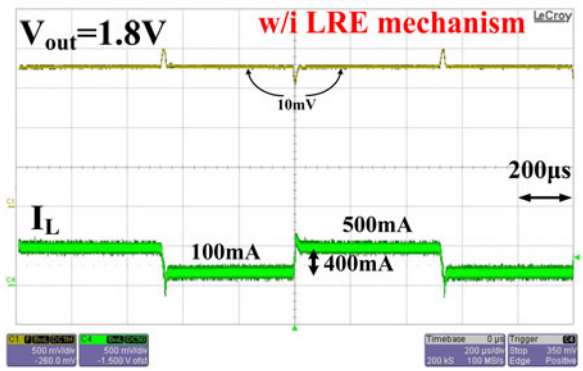


(b)

Fig. 13. (a) Chip micrograph. (b) Prototype of the proposed converter.



(a)



(b)

Fig. 14. Measured load transient response of a 400-mA load step. (a) Without the LRE mechanism. (b) With the LRE mechanism.

TABLE II.
SUMMARY OF THE DIGITAL CODES OF THE PROPOSED LRE MECHANISM

Load current \ Digital code	V_3	V_2	V_1
I_o < 150mA	0	0	0
150mA < I_o < 200mA	0	0	1
200mA < I_o < 250mA	0	1	0
250mA < I_o < 300mA	0	1	1
300mA < I_o < 350mA	1	0	0
350mA < I_o < 400mA	1	0	1
400mA < I_o < 450mA	1	1	0
I_o > 450mA	1	1	1

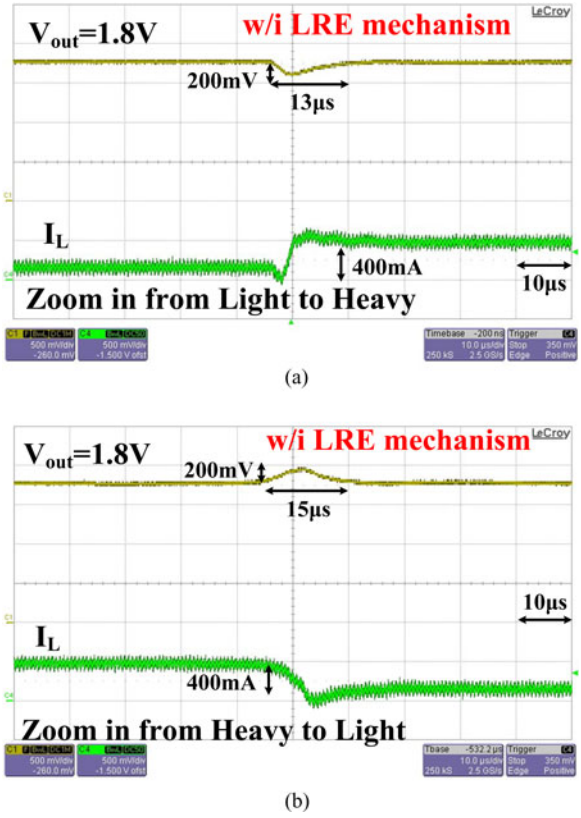


Fig. 15. Measured roomed in the waveform of the load transient response with the LRE mechanism. (a) Load changes from low to high current. (b) Load changes from high to low current.

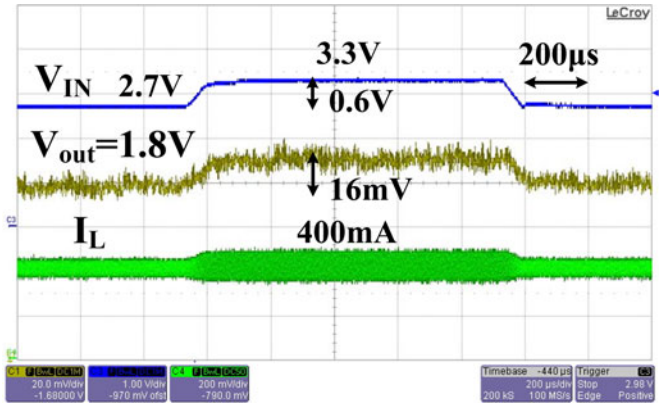


Fig. 16. Measured line transient response when $I_L = 400\,\text{mA}$.

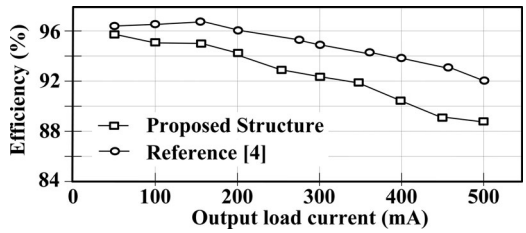


Fig. 17. Comparison of the power-conversion efficiency.

B. Current Sensing Circuit

As depicted in Fig. 11, a simple *RC* low-pass filter is used to accomplish the current sensing function [10]–[15]. The following equation indicates the voltage drop across the inductor L in series with the direct current resistance (DCR) R_{DCR}:

$$V_{LX} - V_{\text{out}} = i_L R_{\text{DCR}} \left(1 + s\frac{L}{R_{\text{DCR}}}\right). \tag{20}$$

The current sensing signal V_{cs} can be expressed in (21). Therefore, by substituting (20) into (21), the current sensing signal across the capacitor C_S, which attains the current sense function is related to the inductor current:

$$V_{cs}(s) = (V_{LX} - V_{cp}) \cdot \frac{1/sC_s}{(1/sC_s) + R_s} \tag{21}$$

$$V_{cs}(s) = (V_{\text{out}} - V_{cp})\frac{1}{1 + sC_sR_s} + i_L R_{\text{DCR}}\frac{1 + s(L/R_{\text{DCR}})}{1 + sC_sR_s}$$

$$\xrightarrow{s=0} V_{cs}(0) = (V_{\text{out}} - V_{cp}) + I_L R_{\text{DCR}}. \tag{22}$$

The dc inductor current level represents the output load condition in the buck converter. The current sensing signal V_{cs} shown in (22) is proved to be proportional to the dc inductor current I_L at the power stage. As a result, the output loading information can be easily yielded by this current sensing mechanism. In addition, the ratio of the two time constants L/R_{DCR} and C_sR_s have an influence on the sensing signal V_{cs} at the medium or the high frequency [16]. The optimal implementation is forcing L/R_{DCR} and C_sR_s to be equal that would ensure the correct operation in the current-mode control.

C. LRE Mechanism

Fig. 12 shows the schematic of the proposed LRE mechanism. The high-side sensing circuit is used to acquire the output load condition at the power stage. The sample and hold (SH)

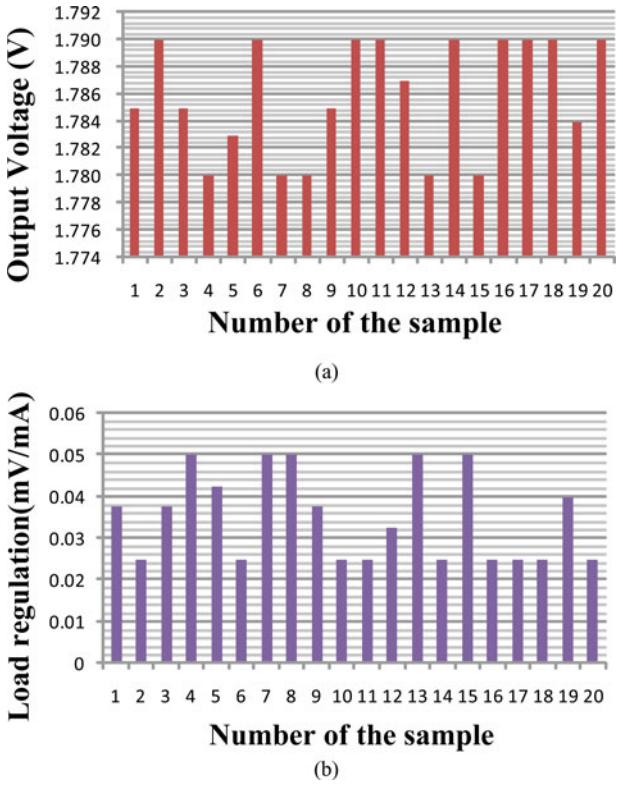


Fig. 18. Statistical reports of the proposed structure of 20 samples. (a) Statistical report of the output voltage. (b) Statistical report of the load regulation.

circuit with the sampling signal V_{ksh} obtains the average inductor current to derive the load current condition. Besides, the transistor M_{10} in the SH circuit is designed to avoid the charge injection problem for improving the accuracy [17]. Thus, the sampling current $I_{\rm SH}$ will flow through the current level comparison circuit to determine the bias current level for the DIDO error amplifier to improve the load regulation of the buck converter [18].

The current level comparison circuit generates the 3-bit digital code, which is composed of V_1, V_2, and V_3. The 3-bit digital code is sent to the DIDO amplifier to control the auxiliary switches in Fig. 10. Thus, the voltages of V_{cp} and V_{cn} in the DIDO error amplifier can be pulled up or down under different load conditions. To enhance the load regulation of the buck converter, the LRE mechanism adds a load-dependent offset voltage $V_{\rm offset}$ to the error signals V_{cp} and V_{cn}. Owing to the bias currents, which can be modulated by the switches M_{s1}–M_{s6} shown in Fig. 10 through the digital code V_1, V_2, and V_3 in the LRE circuit, the drawback of the low gain DIDO error amplifier can be redeemed. As a result, the voltage regulation of the buck converter can be enhanced under different load conditions.

With the LRE mechanism, the output voltage $V_{\rm out}$ in (5) can be redefined as (23) with load-proportional offset voltage $V_{\rm offset}$, which is obtained from the LRE mechanism:

$$V_{\rm out} \approx V_{\rm ref}\frac{1}{\beta} - I_o Z_o + V_{\rm offset} \text{ where } Z_o = \frac{Z_{o(\rm open-loop)}}{1 + A_{V0}\beta} \text{ and } \beta = \frac{R_{F2}}{R_{F1} + F_{F2}}. \quad (23)$$

Therefore, the voltage variation caused by the output impedance of the low gain structure can be compensated to achieve the good voltage regulation.

The operation procedure during the load transient response of the proposed buck converter is demonstrated as follows. When a load transient occurs, the average inductor current must be changed. At this time, the encoder can produce a 3-bit digital code based on the sampling current $I_{\rm SH}$ to adjust the offset voltage $V_{\rm offset}$ to modulate both V_{cp} and V_{cn}. The offset voltage $V_{\rm offset}$ would be decreased to cancel the variation of V_{LX}, i.e., keeping (19) as a constant value when the step-up load transient occurs. On the other hand, when the stepdown load transient response occurs, the increase of $V_{\rm offset}$ can eliminate the variation of V_{LX} to obtain a good voltage regulation result. As the illustration in (23), the voltage variation resulted from the output load current I_o and the output impedance of the current-mode buck converter Z_o can be compensated by the proposed LRE mechanism in the proposed work.

V. Measurement Results

The proposed current-mode dc–dc buck converter with the DIDO error amplifier and the LRE mechanism was fabricated by the 0.25 μm BCD process. The off-chip inductor and output capacitor are 4.7 μH and 10 μF, respectively. The switching frequency is 1.5 MHz. The output voltage is 1.8 V in a typical application with the Li-ion battery-powered input voltage from 2.7 to 4.3 V. Fig. 13 shows the chip micrograph and the prototype of the proposed converter. The active silicon area is 1.65 mm^2.

Fig. 14 shows the measured load transient response. When a load changes from 100 mA to 500 mA, the output voltage difference between the two loads is 200 mV without the LRE mechanism as shown in Fig. 14(a). The load regulation is 0.5mV/mA. It resulted from the small voltage gain of the DIDO error amplifier. Although the use of the system-compensation components is unnecessary, the poor voltage regulation performance is hard to apply to the realistic power-management module, especially, for the portable devices. On the other hand, the voltage variation can be minimized to 10 mV with the LRE mechanism as shown in Fig. 14(b) when a 400 mA load step occurs. As a result, the load regulation can be enhanced to 0.025mV/mA with an improvement of 20 times achieved by the LRE mechanism. Moreover, without the need of large system-compensation components of resistors and capacitors, a fast transient and compact size solution can be achieved in the proposed structure. The digital codes of the proposed LRE mechanism are summarized in Table II. Fig. 15 shows the measured enlarged waveform of the load transient response. The recovery time is shorter than 15 μs. It can surely demonstrate both the correct and stable operation of the proposed structure. Fig. 16 shows the measured line transient response. With the input voltage variation of 0.6 V, a 16-mV voltage variation is derived at the output node. The power-conversion efficiency is shown in Fig. 17. Furthermore, Fig. 18 shows the statistical reports of the output voltage and the load regulation with 20 samples of the proposed structure. It can demonstrate the work of the LRE mechanism in the proposed current-mode buck converter with the DIDO error

TABLE III.
DESIGN SPECIFICATIONS

Technology	0.25 μm CMOS process
Inductor (off-chip)	4.7 μH
Capacitor (off-chip)	10 μF
Input voltage	2.7 V ~ 4.3 V
Output voltage	1.8 V (Typical application)
Switching frequency	1.5 MHz
Maximum load current	500 mA
Recovery time (Load from 100 mA to 500 mA or vice versa)	20 μs
Current consumption in controller	120 μA (DIDO amplifier: 55μA, LRE circuit: 35μA, Osc: 30μA)
Load Regulation	0.025 mV/mA with LRE mechanism @ V_{IN} = 3.3 V, V_{out} = 1.8 V
Chip Area	1500 μm*1100 μm (Including test pads)

TABLE IV
COMPARISONS OF THE PRIOR ARTS

	This work	[6]	[19]	[20]
Technology	0.25 μm CMOS	0.6 μm CMOS	0.6 μm CMOS	0.6 μm CMOS
Inductor	4.7 μH	4.7 μH	4.7 μH	N/A
Capacitor	10 μF	10 μF	10 μF	N/A
Input voltage	3.3 V	3.6 V	3.6 V	1.2 V
Output voltage	1.8 V	2.5 V	2.1 V	1 V
Switching frequency	1.5 MHz	1.1 MHz	500 kHz	500 kHz
Control mechanism	Current Mode PWM Control	Current Mode PWM Control	Current Mode PWM Control	Current Mode PWM Control
Compensation components	None	C_{FB}=22pF	C_C=1nF R_z<100kΩ	With C_C and R_z
Load regulation	0.025 mV/mA (w/i LRE) 0.5 mV/mA (w/o LRE)	0.02 mV/mA	N/A	0.31 mV/mA

amplifier. The implementation of the DIDO amplifier with the LRE mechanism can achieve good load regulation with small power overhead compared to the conventional current-mode buck converter with a high-gain error amplifier proposed in [6]. The detail design specifications are listed in Table III and the comparisons of the prior arts are listed in Table IV.

VI. CONCLUSION

The proportional compensated buck converter with the DIDO error amplifier and the LRE mechanism is proposed in this paper. The DIDO error amplifier can guarantee system modulation and strengthen noise immunity. In addition, the LRE mechanism is applied in the DIDO error amplifier to enhance load regulation. Moreover, it achieves the system stability without the need of compensation components and yields the fast transient response. The load regulation can be improved to 0.025 mV/mA with an improvement about 20 times owing to the LRE mechanism.

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REFERENCES

[1] Y.-H. Lee, S.-J. Wang, C.-Y. Hsieh, and K.-H. Chen, "Current mode dc–dc buck converters with optimal fast transient control,," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2008, pp. 3045–3048.

[2] K.-H. Chen, C.-J. Chang, and T.-H. Liu, "Bidirectional current-mode capacitor multipliers for on-chip compensation," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 180–188, Jan. 2008.

[3] H.-W. Huang, K.-H. Chen, and S.-Y. Kuo, "Dithering skip modulation, width and dead time controllers in highly efficient dc–dc converters for system-on-chip applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2451–2465, Nov. 2007.

[4] J. Fan, X. Li, S. Lim, and A. Q. Huang, "Design and characterization of differentially enhanced duty ripple control (DE-DRC) for step-down converter," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2714–2725, Dec. 2009.

[5] E. Fuentealba Vidal, I. Eidt Colling, and I. Barbi, "An exact current-mode PFM boost converter with dynamic stored energy technique,," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 1129–1134, Apr. 2009.

[6] R. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.

[7] R. B. Ridley, "A new continuous-time model for current-mode control with constant frequency, constant on-time, and constant off-time, in CCM and DCM," in *Proc. IEEE Power Electron. Spec. Conf.*, 1990, pp. 382–389.

[8] J. A. Morales-Saldaa, J. Leyva-Ramos, E. E. Carbajal-Gutierrez, and M. G. Ortiz-Lopez, "Average current-mode control scheme for a quadratic buck converter with a single switch,," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 485–490, Jan. 2008.

[9] H. Chen, Z. Qian, S. Yang, and C. Wolf, "Finite-element modeling of saturation effect excited by differential-mode current in a common-mode

choke," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 873–877, Mar. 2009.
[10] H. P. Forghani-zadeh and G. A. Rincon-Mora, "Current-sensing techniques for dc–dc converters," in *Proc. IEEE Midwest Symp. Circuits Syst.*, 2002, pp. II-577–II580.
[11] E. Dallago, M. Passoni, and G. Sassone, "Lossless current sensing in low-voltage high-current dc/dc modular supplies," *IEEE Trans. Ind. Electron.*, vol. 47, no. 6, pp. 1249–1252, Jun. 2000.
[12] S. Ziegler, R. C. Woodward, H. H. C. Iu, and L. J. Borle, "Lossless inductor current sensing method with improved frequency response,," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1218–1222, May 2009.
[13] S. Saggini, D. Zambotti, E. Bertelli, and M. Ghioni, "Digital autotuning system for inductor current sensing in voltage regulation module applications," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2500–2506, Sep. 2008.
[14] G. Eirea and S. R. Sanders, "High precision load current sensing using online calibration of trace resistance,," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 907–914, Mar. 2008.
[15] R. P. Singh and A. M. Khambadkone, "Giant magneto resistive (GMR) effect based current sensing technique for low voltage/high current voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 915–925, Mar. 2008.
[16] L. Hua and S. Luo, "Design considerations of time constant mismatch problem for inductor DCR current sensing method," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 2182–2188.
[17] B. Razavi, *Design of Analog CMOS Integrated Circuits*. Boston, MA: McGraw-Hill, 2001.
[18] B. Linares-Barranco and T. Serrano-Gotarredona, "On the design and characterization of femtoampere current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1353–1363, Aug. 2003.
[19] C. F. Lee and P. K. T. Mok, "A monolithic current-mode CMOS dc–dc converter with on-chip current-sensing technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 3–14, Jan. 2004.
[20] C. Y. Leung, P. K. T. Mok, K. N. Leung, and M. Chan, "An intergrated CMOS current-sensing circuit for low-voltage current-mode buck regulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 7, pp. 394–397, Jul. 2005.

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