

WiT: Optimal Wiring Topology for Electromigration Avoidance

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Abstract—Due to excessive current densities, electromigration (EM) may trigger a permanent open- or short-circuit failure in signal wires or power networks in analog or mixed-signal circuits. As the feature size keeps shrinking, this effect becomes a key reliability concern. Hence, in this paper, we focus on wiring topology generation for avoiding EM at the routing stage. Prior works tended towards heuristics; on the contrary, we first claim this problem belongs to class P instead of class NP-hard. Our breakthrough is, via the proof of the greedy-choice property, we successfully model this problem on a multi-source multi-sink flow network and then solve it by a strongly polynomial time algorithm. Experimental results prove the effectiveness and efficiency of our algorithm.

Index Terms—Algorithms, electromigration (EM), global routing, integrated circuit reliability, linear programming.

I. INTRODUCTION

As technology advances, the shrinking feature size results in an increasing current density¹ [1]. When the current density of a wire exceeds the process limitation, a mass of atoms inside the metal (e.g., copper or aluminum) are forced to migrate along the electron flow and the gradual transport eventually causes a permanent failure (e.g., open- or short-circuit defect). This phenomenon is referred to as electromigration (EM). Since this wear-out failure is triggered after a circuit has been operating for months, or even years, EM reliability is measured in terms of the mean time to failure (MTF), depending on the current density and the working temperature of a wire [2]. Hence, in modern analog and mixed-signal designs, EM has become a prevalent reliability issue for signal or power lines. EM reliability has attracted great attention in recent literature, e.g., [3]–[20].

EM reliability relies on the following two techniques.

- 1) *EM Simulation/Analysis*: Because EM manifests itself only after a circuit has been used for a period of time, the defect chips cannot be filtered out during product testing. A superior EM simulator/analyzer is desired to characterize the realistic current values for each terminal/wire and to identify the wires that are potentially threatened by EM [3]–[7], [19].
- 2) *Wiring Topology for EM*: To diminish the EM risk, a thin wire should be widened according to its current density. Conventional EM fixing is applied at the post-layout stage, which may consume tremendous routing resources and induce a large amount of layout change [20]. On the contrary, if a good wiring topology considering EM is applied to a router, we may immune EM with much fewer routing resources [8]–[11].

Typically, the routing resource is measured by the total wire area.² Under EM consideration, the wire width should vary according to its current density. Consider an instance created by [10]—a signal net with three current sources and four current sinks—as shown in Fig. 1(a). The current value of each current source/sink is indicated by a positive/negative value. In this example, for simplicity, the allowable current in a unit width wire is normalized to 1. If the minimum wirelength routing is applied, followed by EM fixing by widening wires at post-layout, Fig. 1(b) depicts the result of area 182. (The number/arrow indicates the current value/direction of each wire segment.) The post-layout modification may consume a high routing resource and even produce DRC errors. Although we can refine it, a significant amount of layout change is inevitable. Considering EM during routing instead, prior works [10] and [11] propose heuristics and have the lower wire area 154 [see Fig. 1(d)] and 144 [see Fig. 1(f)], respectively. In fact, we find there is an optimal solution of area 142 [see Fig. 1(h)].

Hence, based on this case, it would be beneficial to consider EM at routing. This task is accomplished by wiring topology generation first and then detailed routing [8]–[11]. The wiring topology determines the connection among all terminals, gives the current-correct wire widths and minimizes the wire area. The detailed router converts each two-terminal connection to a detailed rectilinear routing path and composes them together. If the consumed routing resource of the detailed route can be abstracted into the wiring topology, then an optimal wiring topology implies a good routing result.

In this paper, therefore, we focus on the wiring topology for EM avoidance problem: Given the maximum tolerable current over a unit-area wire for each layer, a set of current sources and

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¹The current density is the current per unit area of cross section.

²The wire area of each wire segment is the product of its wirelength and its width. Here, the wirelength is measured by its Manhattan distance.

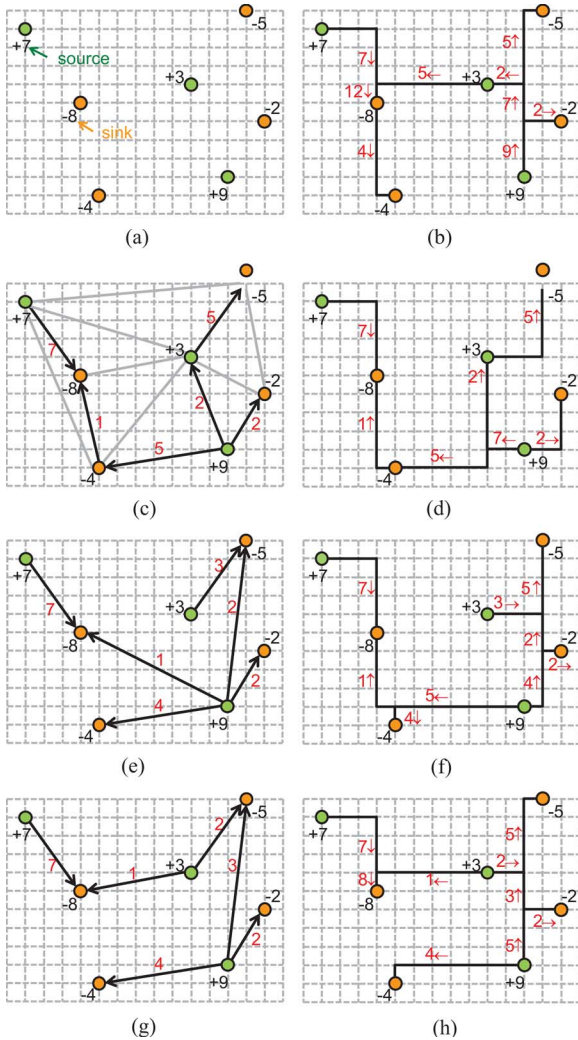


Fig. 1. EM routing: wiring topologies and detailed routes. (a) Three sources and four sinks. (b) Minimum WL: area = 182. (c) Reference [10]'s wiring topology. (d) Reference [10]: area = 154. (e) Reference [11]'s wiring topology. (f) Reference [11]: area = 144. (g) Our optimal wiring topology. (h) Ours: area = 142 (optimal).

a set of current sinks, sources/sinks are associated with characterized current values (e.g., DC, AC, RMS currents), our goal is to find a wiring topology that can offer a sufficient current for each wire segment and consumes the least wire area.

Prior works of wiring topology generation tended towards heuristics [8]–[11]. Among them, [10] and [11] deliver the best results so far. In [10], Lienig and Jerke first construct the Delaunay triangulation³ (DT) to connect all sources and sinks. Second, they grow a routing tree by greedily selecting DT edges. Fig. 1(c) illustrated the wiring topology and DT done by [10]. Since the tree edges can be provided only from DT edges, this method fails if the solution must include a non-DT edge. On the other hand, Yan and Chen iteratively and greedily assign the wire width to the source-sink pair with the largest area gain in [11]. Fig. 1(e) illustrates the wiring topology given by [11]. However, [11] does not consider the competition among

³Given a set of points, the Delaunay triangulation is a triangulation of the point set with the property that no point falls in the interior of the circumcircle of any triangle in the triangulation [21].

all sources and the area gain computation is time-consuming. Moreover, checking the corresponding detailed routes shown in Fig. 1, a good wiring topology indeed leads to a good detailed route.

Unlike prior works, after exploring the complexity of this problem, we *first* claim this problem belongs to class P instead of class NP-hard.⁴ Our breakthrough is, via the proof of the greedy-choice property [22], we successfully model this problem on a multi-source multi-sink flow network and then solve it in a strongly polynomial running time.⁵ Table I summarizes the comparison between our algorithm and state-of-the-art works.

Experimental results prove our theoretical contribution. Our algorithm converges to the global optimal solution generated by linear programming. Compared with the state-of-the-art works [10], [11], our algorithm outperforms them by large margins in terms of effectiveness and efficiency, especially for large-scale cases.

The remainder of this paper is organized as follows. In Section II, we briefly introduce EM and currents. Section III describes the wiring topology generation problem to be solved in this paper and gives the properties. We reformulate this problem as a linear program and then solve it on a flow network in Section IV. We extend our approach to consider IR drop, nonuniform temperature distribution and wire spacing in Section V. Section VI shows the experimental results. Finally, we summarize this paper in Section VII.

II. PRELIMINARIES

In this section, we introduce EM and how different types of currents affect EM.

A. Electromigration

The EM effect is a major reliability issue for analog and mixed-signal circuits. EM⁶ occurs when an extremely dense electron flow, so called electron wind, knocks off atoms within the copper or aluminum wire and moves them away from their original positions. This transport leaves a gap at one end and increases the stress at the other, eventually leading to open- and short-circuit failures.

Black proposed an empirical model of the mean time to failure (MTF) of a wire due to EM; MTF has a squared relationship with the current density J

$$\text{MTF} = AJ^{-2} \exp\left(\frac{\phi}{kT_{\text{em}}}\right) \quad (1)$$

where A is a cross-sectional area related coefficient, ϕ is the activation energy, k is the Boltzmann constant, T_{em} is the working temperature [2], [18]. Based on (1), to last MTF, physical design

⁴A problem belongs to class P if it can optimally be solved in a polynomial running time. Although most of Steiner tree problems are proven NP-hard [22], the wiring topology for EM problem belongs to class P.

⁵The running time of a strongly polynomial-time algorithm for a network problem is bounded by the numbers of nodes and edges and not by the magnitudes of the edge costs or capacities.

⁶When the force of the electron wind is much greater than the force of the electrical field, ionized atoms are swept along with the flow of electrons. These atoms accumulate at grain boundaries thus forming hillocks (short-circuit defects) and leaving voids (open-circuit defects) at their original positions [2].

TABLE I
COMPARISON BETWEEN STATE-OF-THE-ART WORKS ON WIRING TOPOLOGY GENERATION

		Theoretical contribution	Approach	Capability	Runtime
Lienig & Jerke [10]		-	Delaunay triangulation	Heuristic	Medium
Yan & Chen [11]		-	Greedy width assignment	Heuristic	Slow
Ours	LP	Greedy-choice property	Linear programming	Optimal	Medium
	WiT		Negative-cycle detection in flow network	Optimal	Fast

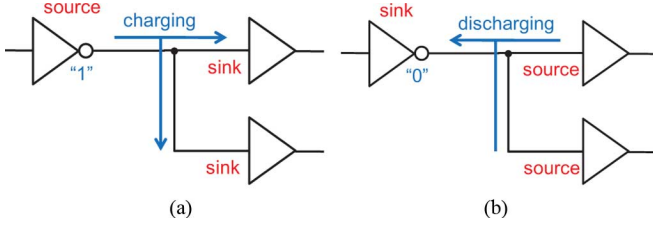


Fig. 2. AC currents for EM analysis. The source in (a) becomes a sink in (b) and vice versa.

must ensure that the actual current density J within the wires does not exceed the limit characterized by the expected working temperature T_{em} .

B. Currents

The current flow is composed of direct and alternating components

$$I = I_{DC} + I_{AC} \quad (2)$$

where I_{DC} is the direct current (DC) representing the average value and I_{AC} is the alternating current (AC) representing the variant value [23]. The (unidirectional) DC component provides a constant electron wind to accumulate atoms and has a critical impact on EM. On the other hand, the (bidirectional) AC component pushes the atoms back and forth. If the frequency of the AC component is low, the induced transport could be unnegligible like the DC component. A high-frequency AC component does not directly trigger EM, but it consumes power and may generate heat. The root-mean-square (RMS) AC current—the quadratic mean—is usually used to indicate the consumed power and the heating up temperature difference. Typically, the technology file defines the layer-specific process limit for each current component (DC and AC) and constrains the RMS value to control the temperature.

In addition, in analog and mixed-signal designs, most of device terminals serve as either current sources or sinks all the time. In some cases, e.g., a push pull output stage, the device terminal periodically changes its role as a source and as a sink. Especially, a set of current sources corresponds to a set of sinks. Due to the periodical changing behavior, we may analyze one situation and obtain the results for the other by reversing the current direction. For example, as shown in Fig. 2, sources and sinks form a group and charging and discharging take turns.

III. PROBLEM FORMULATION AND PROPERTIES

This section gives the problem formulation, derives the properties that help us to abstract the routing resource of a detailed route and proves the greedy-choice property.

A. Problem Formulation

In this paper, we consider the wiring topology for EM avoidance (TEA) problem as follows. In addition, our problem formulation is equivalent to that in [10], [11].

Problem: Wiring TEA: Given the maximum tolerable current density J_{max} for each current component and for each routing layer/via, a set $S = \{s_1, s_2, \dots, s_m\}$ of m current sources, a set $T = \{t_1, t_2, \dots, t_n\}$ of n current sinks, where each current source s_i (respectively, sink t_j) is associated with a flow f_{s_i} (respectively, f_{t_j}), construct a wiring topology to connect all current sources and sinks defined in sets S and T such that the current for each wire segment is bounded by J_{max} , the total wire area is minimized and Kirchhoff's current conservation law is satisfied everywhere.

As mentioned in Section II, J_{max} for each current component and for each layer (via) can be provided by the technology file. On the other hand, without loss of generality, let the thickness h of a wire be a constant for a layer (via). To minimize the routing resource (wire area), we can fully utilize J_{max} for each layer (via)

$$J_{max} = \frac{I}{A} = \frac{f}{wh} \Rightarrow f = J_{max}wh = (J_{max}h)w \Rightarrow f \propto w. \quad (3)$$

Since J_{max} and h are constant for a certain current component and for a specific layer (via), the flow (current value) f is proportional to the wire width w . Hence, for a unit length wire, the wire width offering one unit current consumes routing resource $1/J_{max}$. Based on (3), area optimality can be achieved by minimizing not only the wirelength of a wire segment but also the flow within it.

Let f_{opt} be the optimal flow assigned. Based on (2), since the DC current is unidirectional and the AC current is bidirectional, f_{opt} of a wire segment should be computed for DC and AC separately, i.e., $f_{DC,opt}$ and $f_{AC,opt}$. Then these two values are added up, i.e.,

$$|f_{opt}| = |f_{DC,opt}| + |f_{AC,opt}|. \quad (4)$$

According to Kirchhoff's current conservation law, a legal TEA problem instance must satisfy the following criterion, i.e., the total current values from sources equal those to sinks for DC or AC:

$$\sum_{i=1}^m f_{s_i} + \sum_{j=1}^n f_{t_j} = 0. \quad (5)$$

This criterion can be verified at the very beginning.

Since our goal is to dispatch all currents generated from sources and to maintain a balance, in some cases, the resulting topology forms a forest; we may add some dummy wires in between trees if necessary.

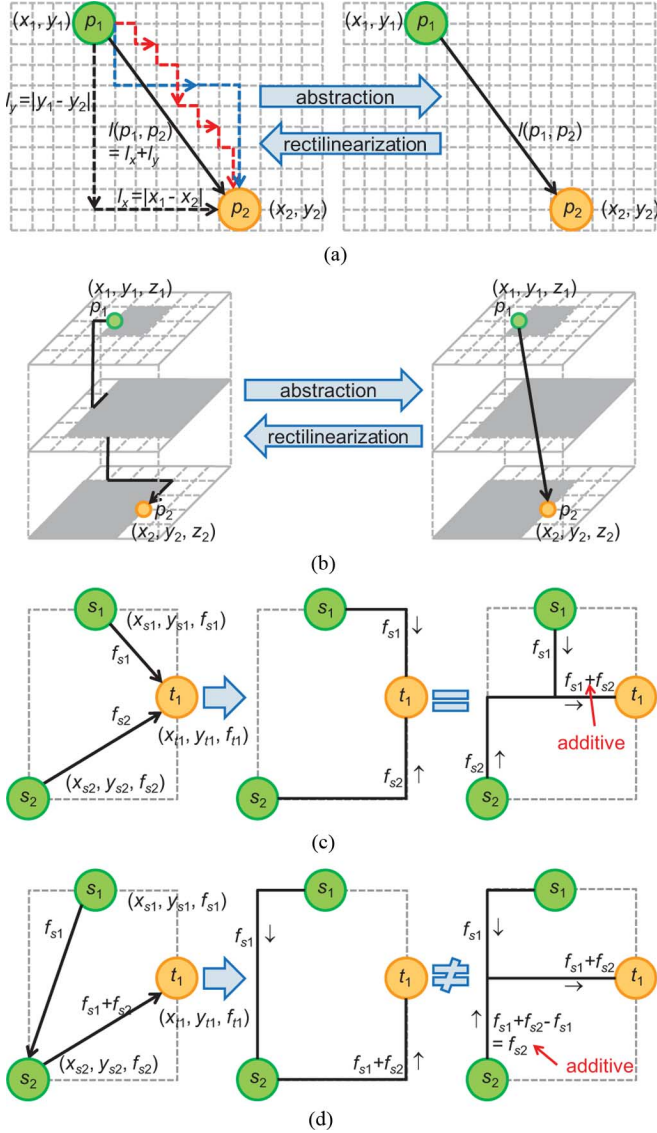


Fig. 3. (a) Wirelength in a plane. (b) Wirelength for multi-layers and obstacles. (c) Superposition of overlapped wires. Wire area keeps the same. (d) Superposition of overlapped wires. Wire area may vary.

B. Wirelength and Wire Area

First of all, consider an obstacle-free plane. For rectilinear routing, only vertical and horizontal lines are allowed. Hence, as depicted in Fig. 3(a), the wirelength $l(p_1, p_2)$ between two arbitrary points $p_1(x_1, y_1, f_1)$ and $p_2(x_2, y_2, f_2)$ is equal to their Manhattan distance

$$l(p_1, p_2) = l_x + l_y = |x_1 - x_2| + |y_1 - y_2|. \quad (6)$$

There are many possible monotonic rectilinear routes for two arbitrary sources/sinks and it can be seen that all monotonic routes consume an equal wirelength. Hence, the practical route between any two sources/sinks can be abstracted by a slant wire segment of length equal to their Manhattan distance. Moreover, due to coordinate independence, l_x and l_y are computed separately.

However, the routing cost varies for layers (vias) and obstacles may exist. In both cases, as shown in Fig. 3(b), there is

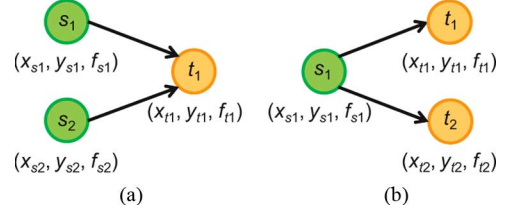


Fig. 4. Greedy-choice of the generic form for wiring topology. (a) Two sources s_1, s_2 , and one sink t_1 . (b) Two sinks t_1, t_2 , and one source s_1 .

a *one-to-one mapping* between the slant wire segment and the wirelength, i.e., the shortest routing path length. The shortest routing path means the path with the minimum *accumulated area cost* for one unit current within this connection. Based on Section III-A, the area cost of a wire segment of length l with one-unit current on a specific layer (via) is l/J_{\max} . Taking the summation of the area costs along a path, we obtain its accumulated area cost. Hence, this abstraction still works. In addition, this abstraction can be also applied for nonuniform temperature distribution. (see Section V).

Typically, the consumed routing resource can be computed as the total wiring area. For practical routes, if two wire segments overlap at some layer, as shown in Fig. 3(c) and (d), the overlapped parts can be *superpositioned*, i.e., *additive* considering current directions. Based on superposition, a current can be split into pieces, planned individually and then combined together. Moreover, overlapped wire segments occupy the same wire area in topology and in detailed route as shown in Fig. 3(c), but the wire area may vary as depicted in Fig. 3(d). Our goal is to find the property of the optimal wiring topology to facilitate detailed routing.

C. Greedy-Choice Property

As mentioned in Section II-A, to minimize the routing resource, i.e., wire area, not only the wirelength for each wire segment but also the magnitude of its flow should be considered. Here, we prove the greedy-choice property of the TEA problem. This property simplifies the direction of a flow thus allowing us to develop the optimal wiring topology in Section IV.

First of all, we figure out the greedy-choice property of the generic form for wire connections. Suppose that there exists an optimal wiring topology for the generic form containing two sources s_1, s_2 , and one sink t_1 . Any more complicated case is composed of many copies of this form. We shall claim, as shown in Fig. 4(a), the greedy-choice property of this generic form indicates sources s_1 and s_2 individually connect sink t_1 . Symmetrically, this generic form can extend to the case with two sinks plus one source, as shown in Fig. 4(b). By the following theorem and corollary, we can largely simplify the routing problem. We start from an obstacle-free plane and then extend to a general multi-layer space with obstacles.

Theorem—Greedy-Choice Property: There exist two sources s_1, s_2 , and one sink t_1 . Let the partial flows of s_1 and s_2 be sunken by t_1 in the optimal wiring topology

$$f_{s_1} + f_{s_2} + f_{t_1} = 0. \quad (7)$$

The greedy-choice property of the partial wiring topology for these flows is in the form that the wires directly connecting from s_1 to t_1 as well as from s_2 to t_1 . Considering the current

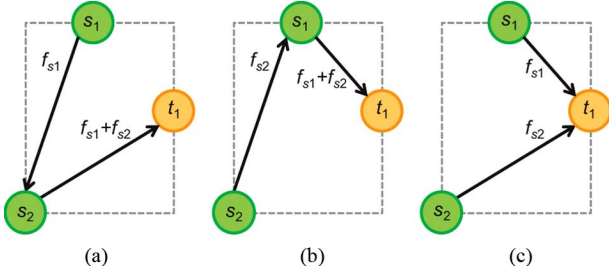


Fig. 5. Greedy-choice property. (a) Option 1: $\{s_1 \rightarrow s_2 \rightarrow t_1\}$. (b) Option 2: $\{s_2 \rightarrow s_1 \rightarrow t_1\}$. (c) Option 3: $\{s_1 \rightarrow t_1\}$ plus $\{s_2 \rightarrow t_1\}$.

directions, the flow within each wire segment can be assigned accordingly.

Proof: We shall prove this theorem by exchange argument.

Without loss of generality, wire connections among s_1 , s_2 , and t_1 fall into the following three options as shown in Fig. 5.

- 1) *Option 1:* s_1 first connects s_2 and then s_2 connects t_1 .
- 2) *Option 2:* s_2 first connects s_1 and then s_1 connects t_1 .
- 3) *Option 3:* s_1 and s_2 connect t_1 individually.

The wire area for each option is as follows:

$$\begin{aligned}
 A(s_1 \rightarrow s_2 \rightarrow t_1) &= f_{s_1} \cdot l(s_1, s_2) + (f_{s_1} + f_{s_2}) \cdot l(s_2, t_1) \\
 &= f_{s_1} \cdot (|x_{s_1} - x_{s_2}| + |y_{s_1} - y_{s_2}|) \\
 &\quad + (f_{s_1} + f_{s_2}) \cdot (|x_{s_2} - x_{t_1}| + |y_{s_2} - y_{t_1}|) \\
 &= f_{s_1} \cdot (|x_{s_1} - x_{s_2}| + |x_{s_2} - x_{t_1}|) \\
 &\quad + f_{s_2} \cdot |x_{s_2} - x_{t_1}| \\
 &\quad + f_{s_1} \cdot (|y_{s_1} - y_{s_2}| + |y_{s_2} - y_{t_1}|) \\
 &\quad + f_{s_2} \cdot |y_{s_2} - y_{t_1}| \\
 A(s_2 \rightarrow s_1 \rightarrow t_1) &= f_{s_2} \cdot l(s_2, s_1) + (f_{s_1} + f_{s_2}) \cdot l(s_1, t_1) \\
 &= f_{s_2} \cdot (|x_{s_2} - x_{s_1}| + |y_{s_2} - y_{s_1}|) \\
 &\quad + (f_{s_1} + f_{s_2}) \cdot (|x_{s_1} - x_{t_1}| + |y_{s_1} - y_{t_1}|) \\
 &= f_{s_2} \cdot (|x_{s_2} - x_{s_1}| + |x_{s_1} - x_{t_1}|) \\
 &\quad + f_{s_1} \cdot |x_{s_1} - x_{t_1}| \\
 &\quad + f_{s_2} \cdot (|y_{s_2} - y_{s_1}| + |y_{s_1} - y_{t_1}|) \\
 &\quad + f_{s_1} \cdot |y_{s_1} - y_{t_1}| \\
 A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1) &= f_{s_1} \cdot l(s_1, t_1) + f_{s_2} \cdot l(s_2, t_1) \\
 &= f_{s_1} \cdot (|x_{s_1} - x_{t_1}| + |y_{s_1} - y_{t_1}|) \\
 &\quad + f_{s_2} \cdot (|x_{s_2} - x_{t_1}| + |y_{s_2} - y_{t_1}|) \\
 &= f_{s_1} \cdot |x_{s_1} - x_{t_1}| + f_{s_2} \cdot |x_{s_2} - x_{t_1}| \\
 &\quad + f_{s_1} \cdot |y_{s_1} - y_{t_1}| + f_{s_2} \cdot |y_{s_2} - y_{t_1}|. \tag{10}
 \end{aligned}$$

If option 3 is optimal, $A_{\min} = A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1)$, we are done. Otherwise, either option 1 or option 2 is optimal

$$\begin{aligned}
 A_{\min} &= A(s_1 \rightarrow s_2 \rightarrow t_1) \\
 &\leq A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1); \text{ or} \\
 A_{\min} &= A(s_2 \rightarrow s_1 \rightarrow t_1) \\
 &\leq A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1). \tag{11}
 \end{aligned}$$

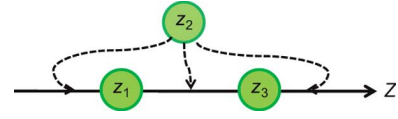


Fig. 6. Consider three points z_1 , z_2 , and z_3 on an axis, where z_1 and z_3 are fixed, while z_2 is movable.

Based on superposition and coordinate independence, the following analysis on the wire area is individually applied to each axis. Consider three arbitrary points, z_1 , z_2 , and z_3 , on an axis. Assume z_1 and z_3 are fixed, while z_2 is movable, as shown in Fig. 6. Considering z_2 is located beyond or in between z_1 and z_3 , we have

$$|z_1 - z_2| + |z_2 - z_3| \geq |z_1 - z_3|. \tag{12}$$

Substituting z_1 , z_2 , and z_3 in (12) with the coordinates of in (8) and (9)

$$\begin{aligned}
 |x_{s_1} - x_{s_2}| + |x_{s_2} - x_{t_1}| &\geq |x_{s_1} - x_{t_1}| \\
 |y_{s_1} - y_{s_2}| + |y_{s_2} - y_{t_1}| &\geq |y_{s_1} - y_{t_1}|; \\
 |x_{s_2} - x_{s_1}| + |x_{s_1} - x_{t_1}| &\geq |x_{s_2} - x_{t_1}| \\
 |y_{s_2} - y_{s_1}| + |y_{s_1} - y_{t_1}| &\geq |y_{s_2} - y_{t_1}|.
 \end{aligned}$$

After simplifying them, we have

$$\begin{aligned}
 A(s_1 \rightarrow s_2 \rightarrow t_1) &\geq A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1); \\
 A(s_2 \rightarrow s_1 \rightarrow t_1) &\geq A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1). \tag{13}
 \end{aligned}$$

Hence, combining (11) and (13)

$$\begin{aligned}
 A_{\min} &= A(s_1 \rightarrow s_2 \rightarrow t_1) \leq A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1) \\
 \text{and} \\
 A(s_1 \rightarrow s_2 \rightarrow t_1) &\geq A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1). \\
 \Rightarrow A_{\min} &= A(s_1 \rightarrow s_2 \rightarrow t_1) = A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1). \\
 A_{\min} &= A(s_2 \rightarrow s_1 \rightarrow t_1) \leq A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1) \\
 \text{and} \\
 A(s_2 \rightarrow s_1 \rightarrow t_1) &\geq A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1). \\
 \Rightarrow A_{\min} &= A(s_2 \rightarrow s_1 \rightarrow t_1) = A(s_1 \rightarrow t_1) + A(s_2 \rightarrow t_1). \tag{14}
 \end{aligned}$$

If option 1 (or option 2) is optimal, option 3 is also optimal. Thus, option 1 (or option 2) can be replaced by option 3 without loss of optimality. The greedy-choice property thus follows. \square

Corollary: The greedy-choice property holds in a general multi-layer space with obstacles.

Proof Sketch: For a general multi-layer space with obstacles, the wirelength in (6) is the shortest path length (minimum accumulated cost) instead of Manhattan distance. The argument for Fig. 6 is modified as follows. Consider three points p_1 , p_2 , and p_3 in a space, where p_1 and p_3 are fixed, while p_2 is movable. p_2 is located either beyond p_1 and p_3 or on the shortest path between p_1 and p_3 . Because of superposition and coordinate independence, considering a multi-layer space with obstacles, the greedy-choice property can be proved by contradiction, i.e., (13) still holds. \square

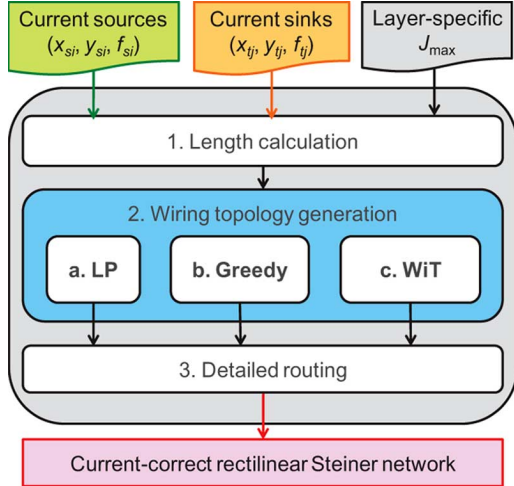


Fig. 7. EM avoidance routing network construction.

By the above theorem and corollary, we can consider wire connections *only* from sources to sinks. The TEA problem can then be viewed as a pairing problem.

IV. WIRING TOPOLOGY GENERATION

In this section, we present the EM avoidance wiring topology generation algorithm.

A. Overview of EM Avoidance Routing Network Construction

Fig. 7 gives the EM avoidance routing network construction flow. In this paper, we focus on wiring topology generation. Based on the greedy-choice property, we simplify the TEA problem as a multiple-source multiple-sink pairing problem. First of all, the wirelength and the flow bound for the connection between every pair of source and sink are computed and recorded by a flow network. Second, sources and sinks are paired, the flow on each connection is determined and a wiring topology is generated. Here, we will introduce two methods based on the greedy-choice property: linear programming and network-flow-based optimization. Later, we will see the wire areas conducted by linear programming and by network-flow-based refinement are the same (optimal). Finally, each connection is rectilinearized by a detailed router based on the stored shortest path. Moreover, as mentioned in Section III, the pairing is done separately for DC and AC. During rectilinearization, the stored paths for selected DC and AC connections will be added together [see (4)]. Fig. 8 shows an example of combining AC and DC topology.

B. Length Calculation

Considering multiple routing layers and avoiding obstacles, during length calculation as shown in Fig. 7, the wirelength for each possible connection is computed by Dijkstra's algorithm [22]. This shortest path (with the minimum *accumulated area cost* for a unit-flow) is stored and if this pair is included in the wiring topology, it will be retrieved at rectilinearization. Fig. 9

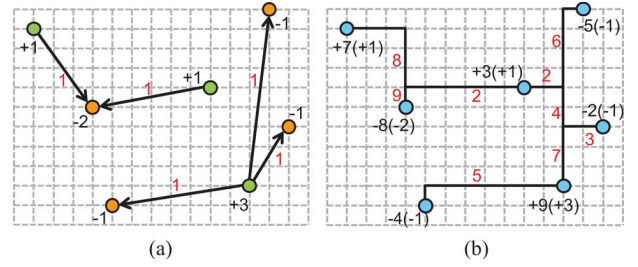


Fig. 8. AC and DC wiring topology of the instance in Fig. 1(a). (a) Assume Fig. 1(g) is the DC wiring topology. Here shows the AC wiring topology, where there are two source-sink groups. (b) The corresponding detailed routing network, where AC and DC paths are added together and the values indicated within parentheses are AC currents.

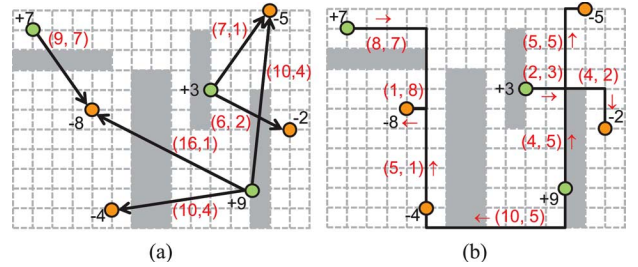


Fig. 9. (a) Instance in Fig. 1(a) with four obstacles (grey blocks) and its obstacle-avoidance wiring topology (optimal area: 178). (b) The corresponding detailed routing tree (area: 178). The pair (length, flow) is attached beside each wire segment.

depicts the resulting wiring topology and routing tree of the instance in Fig. 1(a) with four extra obstacles added.

C. Flow Network and Linear Programming (LP) Formulation

We start from the exact LP formulation for the TEA problem.⁷ As depicted in Fig. 10, a flow network for an instance with m current sources (s_1, s_2, \dots, s_m) and n current sinks (t_1, t_2, \dots, t_n) is a directed graph. Each current source/sink is represented by a vertex. For each pair of source and sink, we have a directed edge (s_i, t_j) from s_i to t_j associated with a triple $(l_{i,j}, f_{i,j}, c_{i,j})$.

- 1) $l_{i,j}$: Wirelength between s_i and t_j .
- 2) $f_{i,j}$: Flow from s_i to t_j .
- 3) $c_{i,j}$: Capacity (upper bound) of flow $f_{i,j}$.

The capacity $c_{i,j}$ and wirelength $l_{i,j}$ can be obtained during length calculation. In addition, two dummy vertices, the super source s_s and the super sink t_t , are added. One edge from s_s to each distinct source s_i is associated with $(0, |f_{s_i}|, |f_{s_i}|)$, while one edge from each distinct sink t_j to t_t is associated with $(0, |f_{s_s}|, |f_{s_s}|)$. In addition, one edge (t_t, s_s) is associated with $(0, |f_{s_s}|, |f_{s_s}|)$, where f_{s_s} is the total flow from sources, $f_{s_s} = \sum_{i=1}^m f_{s_i}$. The objective is to minimize total wire area. Since only the flow from source to sink is considered based on the greedy-choice property, the flow of each pair-wise connection is bounded by the smaller magnitude of its related source and sink, $c_{i,j} = \min(|f_{s_i}|, |f_{t_j}|)$. The wirelength $l_{i,j}$ and capacity

⁷Each flow is a multiple of a unit-flow. Hence, any linear programming solver can find the optimal solution even when the flow variables are declared as the floating number type.

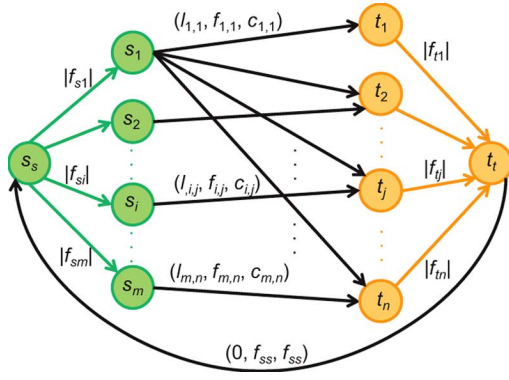


Fig. 10. Flow network for the integer linear program. The capacity $c_{i,j}$ and wirelength $l_{i,j}$ for each edge can be precalculated.

$c_{i,j}$ for each edge can be pre-calculated and they are constants in the following linear program:

$$\begin{aligned} & \text{Minimize} \quad \sum_{i=1}^m \sum_{j=1}^n l_{i,j} f_{i,j} \quad // \text{wire area} \\ & \text{Subject to} \quad f_{s_i} = \sum_{j=1}^n f_{i,j} \quad \text{for } 1 \leq i \leq m, \quad // \text{flow conservation} \\ & \quad \quad \quad f_{t_j} = \sum_{i=1}^m f_{i,j} \quad \text{for } 1 \leq j \leq n, \\ & \quad \quad \quad 0 \leq f_{i,j} \leq c_{i,j}, \quad \text{for all } i, j. \quad // \text{capacity constraint.} \end{aligned}$$

It can be seen that the greedy-choice property largely simplifies the linear program. Compared with the general minimum-cost circulation problem, there are no edges either between sources or between sinks in the flow network constructed in this paper. Thus, the central part of the flow network, i.e., the subgraph induced by sources and sinks, is an $m \times n$ bipartite graph (instead of a clique K_{m+n}). Hence, the number of variables and constraints is bounded by $O(mn)$. Thus, it can then be handled by any linear programming solver efficiently.

D. Network-Flow-Based Optimization

Instead of relying on a powerful linear programming solver, we further develop an optimal algorithm-WiT based on the concept of negative cycle detection [24].

1) *Initial Solution—Greedy Method*: First of all, we shall devise an efficient algorithm to assign an initial flow with sufficiently good quality. For efficiency, we select the greedy method; for effectiveness, we choose the minimum wirelength as the greedy rule. The wirelength between any pair of source and sink can be viewed as the area cost for assigning one-unit flow into this connection. Conceptually, we may greedily start from a pair with minimum wirelength (instead of with minimum area). The pair-wise wirelength can be stored in a minheap and then the greedy method can be completed in $O((mn) \lg(mn))$ time [22].

2) *Flow and Residual Networks*: To construct an optimal wiring topology, we start from the flow network with the initial flow assigned by the aforementioned greedy method. As

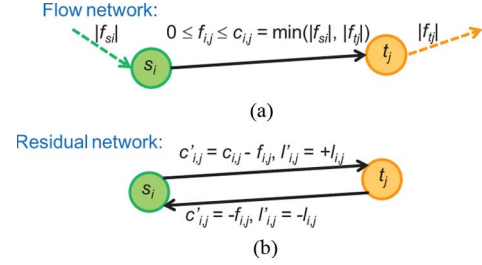


Fig. 11. (a) Flow network. (b) Residual network.

shown in Fig. 11(a), if the flow within the wire between source s_i and sink t_j is $f_{i,j}$ subject to the capacity $c_{i,j}$, then we may feed in no more than $c_{i,j} - f_{i,j}$ flow, or we can take at most $f_{i,j}$ back. One-unit flow injection contributes $+l_{i,j}$ wire area, while one-unit flow removal has $-l_{i,j}$ impact on the wire area. Based on this idea, the residual network can be constructed as Fig. 11(b). The positive/negative sign (\pm) of capacity and wirelength implies the possible direction and area impact of its residual flow. The residual network construction is summarized as follows. For each edge (s_i, t_j) between source s_i and sink t_j with flow $f_{i,j}$ and of wirelength $l_{i,j}$ in the flow network, two edges are constructed in the corresponding residual network, where the residual wirelength/flow/capacity is represented by $(l'_{i,j}, f'_{i,j}, c'_{i,j})$.

1) A forward edge (s_i, t_j) has a residual capacity $c'_{i,j} = c_{i,j} - f_{i,j}$, $0 \leq f'_{i,j} \leq c'_{i,j}$ and has a wirelength $l'_{i,j} = +l_{i,j}$.
2) A backward edge (t_j, s_i) has a residual capacity $c'_{i,j} = -f_{i,j}$, $-f_{i,j} \leq f'_{i,j} \leq 0$ and has a wirelength $l'_{i,j} = -l_{i,j}$.
In addition, a forward/backward edge of zero residual capacity is redundant and thus can be omitted. After applying this process to each edge in the flow network, the residual network is constructed.

3) *Wire Area Optimization*: Based on the residual network introduced above, we can analyze the optimality of a solution by the following theorem.

Theorem—Negative-Cycle Removal: If the flow assignment of a flow network is optimal, there exists no negative cycles in its residual network.

For example, Fig. 12(a) illustrates an initial flow network (the super source and sink are omitted here) and the corresponding residual network can be derived. Fig. 12(b) highlights the negative cycle inside the residual network, $\{s_1, t_1, s_2, t_2, s_1\}$ of length $-2 (= 7 + (-12) + 10 + (-7))$. If one-unit flow is injected along the direction of this cycle, then this negative cycle can be removed and the optimal solution is found.

Hence, wire area optimization can be done by iteratively injecting a feedback flow to a negative cycle until no negative cycles exist in the residual network. Moreover, each negative cycle can be detected and removed in $O(mn)$ time.

4) *Optimal Network-Flow-Based Algorithm*: The WiT algorithm listed in Fig. 13 generates the optimal wiring topology. Based on WiT, we can build up the EM routing framework given in Fig. 7. Line 5 in EMRoute can be done by a detailed router. If the input instance is legal, i.e., satisfying (3), the initial flow is assigned. The initial assignment can be done by the proposed greedy method or by prior works. The solution is then iteratively refined by negative cycle detection and removal. The optimal

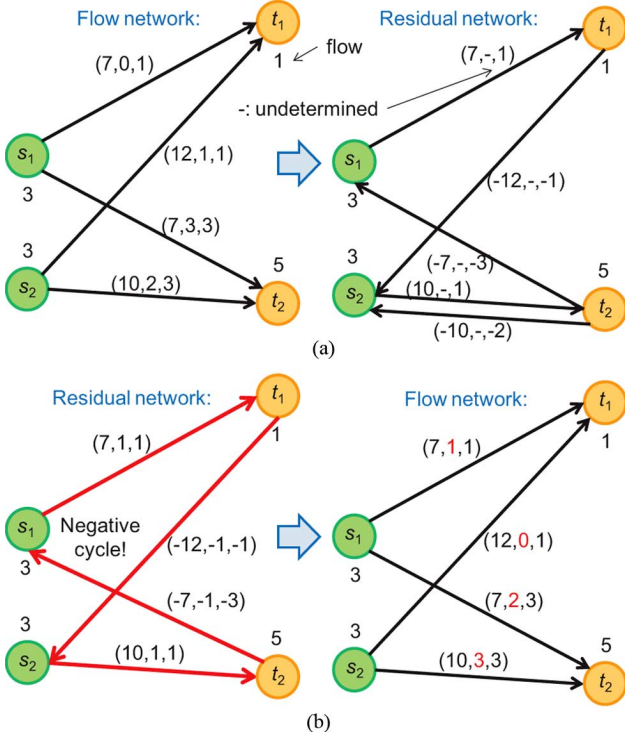


Fig. 12. Negative cycle detection. (a) The flow network for a given flow assignment (area = 53) and its residual flow network, where zero-capacity edges are removed. (b) One negative cycle is removed and the optimal assignment is obtained (area = 51).

```

EMRoute( $S, T$ )
//  $S, T$ : current sources and sinks
//  $L$ : the set of pair-wise shortest wirelength
//  $F$ : flow assignment
1. if the given flow at sources/sinks is illegal then return
2. construct the flow network and calculate paths and lengths  $L$ 
3. find the wiring topology for DC by  $WiT(S, T, L, F_{DC})$ 
4. find the wiring topology for AC by  $WiT(S, T, L, F_{AC})$ 
5. combine  $F_{DC}$  with  $F_{AC}$  and rectilinearize the wiring topology

WiT( $S, T, L, F$ )
1. find an initial flow assignment  $F$ 
2. construct the corresponding residual network of initial flow  $F$ 
3. while there exists a negative cycle in the residual network do
4.   remove the negative cycle
5.   update flow  $F$  and the flow network
6.   update the residual network
7. return  $F$ 

```

Fig. 13. EM avoidance routing with optimal flow assignment by the WiT algorithm.

algorithm is done in $O((mn)\lg(mn) + rmn)$ time with r iterations for refinement. Inspired by [24], we can show that WiT is a strongly polynomial time algorithm; the number of iterations is regardless of the values of flows.

V. EXTENSIONS

In this section, we demonstrate the flexibility of the proposed wiring topology to consider IR drop, nonuniform temperature distribution and wire spacing issues.

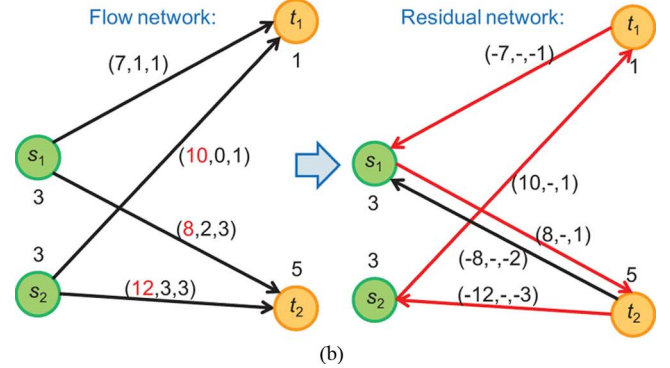
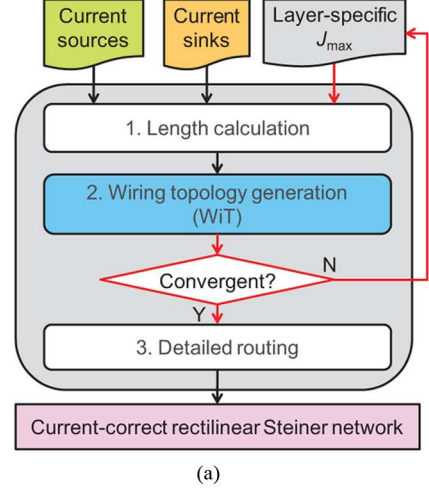


Fig. 14. EM avoidance routing network construction flow for nonuniform temperature distribution. (a) The temperature-aware flow. (b) For the instance shown in Fig. 12(b), where the wirelength is incrementally updated according to temperature deviation, there exists a negative cycle reducing wire area by $1(-1 = 10 - 7 + 8 - 12)$.

A. IR Drop

According to (3), IR drop is computed as follows:

$$\begin{aligned}
 IR &= f \left(\frac{l}{wh} \right) \leq V_{\max} \\
 \Rightarrow \frac{J_{\max}whl}{wh} &= J_{\max}l \leq V_{\max} \\
 \Rightarrow l &\leq l_{\max} = \frac{V_{\max}}{J_{\max}}
 \end{aligned} \tag{15}$$

where V_{\max} represents the bound on IR drop and l_{\max} represents the wirelength bound for a source-sink connection with respect to J_{\max} . It can be seen that if the current density of a wire segment is well-controlled against EM, we can prevent IR drop by setting the upper bound on the wirelength.

Considering IR drop, the initial solution is found as usual. We then reweight the flow network. The length of each violated connection (greater than l_{\max}) is set to as an infinite value. Hence, if the initial solution uses a violated connection and there exists a feasible solution with the minimum wire area, there exists a negative cycle including this violated edge and it can then be fixed. If there is no feasible solution with the minimum wire

TABLE II
COMPARISON ON AREA, RUNTIME, REFINEMENT ITERATIONS BETWEEN LP, WIT AND STATE-OF-THE-ART WORKS

Testcase	INP1	INP2	INP3	INP4	IND1	IND2	IND3	IND4	IND5	RT01	RT02	RT03	RT04	RT05	Average ratio
#Terminals	7	16	10	16	10	10	10	25	33	75	180	303	475	850	
[10] Area	154	122	210	32	6,661	79,400	FAIL	23,112	31,466	FAIL	FAIL	FAIL	FAIL	FAIL	1.388
[10] Runtime (s)	0.001	0.002	0.001	0.002	0.038	0.016	-	0.016	0.040	-	-	-	-	-	
[11] Area	144	98	128	40	5,319	79,000	6,181	16,000	20,814	189,437	10,638,884	3,360,716	6,475,941	59,207,240	1.243
[11] Runtime (s)	0.001	0.002	0.001	0.002	0.001	0.001	0.001	0.003	0.005	0.120	4.958	45.553	297.806	8,573.453	
[11] Refined area	142	90	116	32	5,301	74,200	5,513	13,728	17,044	144,071	7,151,286	2,325,806	4,205,757	37,318,054	1.000
[11] Gain	2	8	12	8	18	4,800	668	2,272	3,770	45,366	3,487,598	1,034,910	2,270,184	21,889,186	
[11] #Iterations	1	2	1	1	1	3	15	20	29	147	622	1,938	4,288	9,238	
[11] Refine runtime (s)	0.000	0.000	0.001	0.000	0.000	0.001	0.001	0.002	0.003	0.028	0.496	4.741	28.883	440.429	
WiT Initial area	142	94	116	32	5,301	78,200	5,629	15,092	19,624	156,489	8,139,250	2,840,420	4,831,845	45,677,120	1.093
WiT Initial runtime (s)	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.015	0.042	0.109	0.425	
WiT Final area	142	90	116	32	5,301	74,200	5,513	13,728	17,044	144,071	7,151,286	2,325,806	4,205,757	37,318,054	1.000
WiT Gain	0	4	0	0	0	4,000	116	1,364	2,580	12,418	987,964	514,614	626,088	8,359,066	
WiT #Iterations	0	1	0	0	0	3	2	17	37	78	415	949	1,197	3,487	
WiT Final runtime (s)	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	<0.001	0.016	0.297	1.794	6.489	89.497	
LP Area	142	90	116	32	5,301	74,200	5,513	13,728	17,044	144,071	7,151,286	2,325,806	4,205,757	37,318,054	1.000
LP Status	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	G.O.	
LP #Variables	12	60	25	64	24	25	25	156	266	1,406	8,100	22,952	56,376	180,621	
LP #Constraints	32	137	61	145	59	61	61	338	566	2,888	16,381	46,208	113,228	362,093	
LP #Nonzeros	60	300	125	320	120	125	125	780	1,330	7,030	40,500	114,760	281,880	903,105	
LP Mem (KB)	25	55	33	58	33	33	33	118	194	1,226	5,878	17,143	41,902	137,159	
LP Runtime (s)	<1.000	<1.000	1.000	<1.000	<1.000	1.000	1.000	<1.000	<1.000	2.000	2.000	5.000	21.000	150.000	

Remarks: 1. #Terminals = #Sources + #Sinks.

Area: the wire area. Average ratio: optimal area is normalized to 1.000.

Refined area: the area after refinement. Initial area: the area of our initial solution. Final area: the area of WiT.

Gain: area reduction done by refinement.

Refine runtime: the runtime of refinement. Initial runtime: the runtime of our initial solution. Final runtime: initial runtime + refine runtime.

#Iterations: the number of refinement iterations.

2. Linear programming (LP) conducted by LINGO always outputs global optimal (G.O.) solutions; its runtimes are rounding to second.
3. Refinement is negative-cycle removal in the WiT algorithm.
4. [10] may generate infeasible solutions (labeled as FAIL). [11] is not refined because it is infeasible for some cases.
5. WiT always converges to the global optimal regardless to the initial solution.

area, after negative-cycle removal, the unfixed violated connections should be widened to satisfy the IR drop bound.

B. Nonuniform Temperature Distribution

Based on (1), the working temperature also affects the current density limit J_{\max} . If the temperature distribution is nonuniform, J_{\max} varies even at the same layer. Based on Section II, the temperature map can be extracted based on the RMS AC current.

Fig. 3(b) shows that when the routing cost varies for each layer/via, a path can be decomposed into wire segments and its wire area equals the accumulated area cost. Based on the same idea, the whole layout space can be divided into regions for a given temperature distribution. Each region corresponds to a distinct J_{\max} limit. Length calculation in Fig. 7 (line 2 of EMRoute in Fig. 13) is adapted accordingly.

Moreover, since the current density and temperature of a wire segment are mutually dependent and time-variant, the wirelength of each possible connection dynamically changes. Hence, the wiring topology should be incrementally updated until convergence. As shown in Fig. 14(a), after each pass, the temperature difference updates J_{\max} and wirelength. The flow network is then incrementally updated and the wiring topology is adapted by negative cycle removal accordingly. Since temperature eventually remains steady under EM safety, the wiring topology gradually converges after several passes. Fig. 14(b) shows an example of incremental update.

C. Wire Width and Wire Spacing Constraints

Moreover, the optimal flow f_{opt} should be in between the minimum printable wire width w_{\min} and the maximum allowable wire width w_{\max} (calibrated from the RMS limit).

In the problem formulation, the consumed routing resource is computed by the wire area. Moreover, we could merge wire segments to reduce the area wasted by wire spacing. As revealed by Ho *et al.*, if each connection is rectilinear, wire merging with the maximum overlapping can be found by dynamic programming for a single-layer without obstacles [25]. Considering obstacles, the V-shape refinement can help [26].

Considering w_{\min} and w_{\max} , the wire width f^* is adjusted after wire merging. If f^* is less than w_{\min} , f^* is set to as w_{\min} . If f^* is greater than w_{\max} , the wire segment is decomposed to several parallel segments and each has a width less than w_{\max} .

Even so, the available routing space may be insufficient due to routing congestion. Hence, considering routing congestion, we can revise the flow network to include not only the shortest path but also alternative paths for each source-sink connection and to constrain the capacity of each possible path by the source/sink currents and the available routing space.

VI. EXPERIMENTAL RESULTS

We implemented our algorithm in C++ language with LEDA package [27] and executed the program on a PC with an Intel Core2 CPU T9400 of 2.53 GHz frequency and 4 GB memory under Windows Vista Business 64 bit Service Pack 1 OS. We also implemented prior works on the same platform.

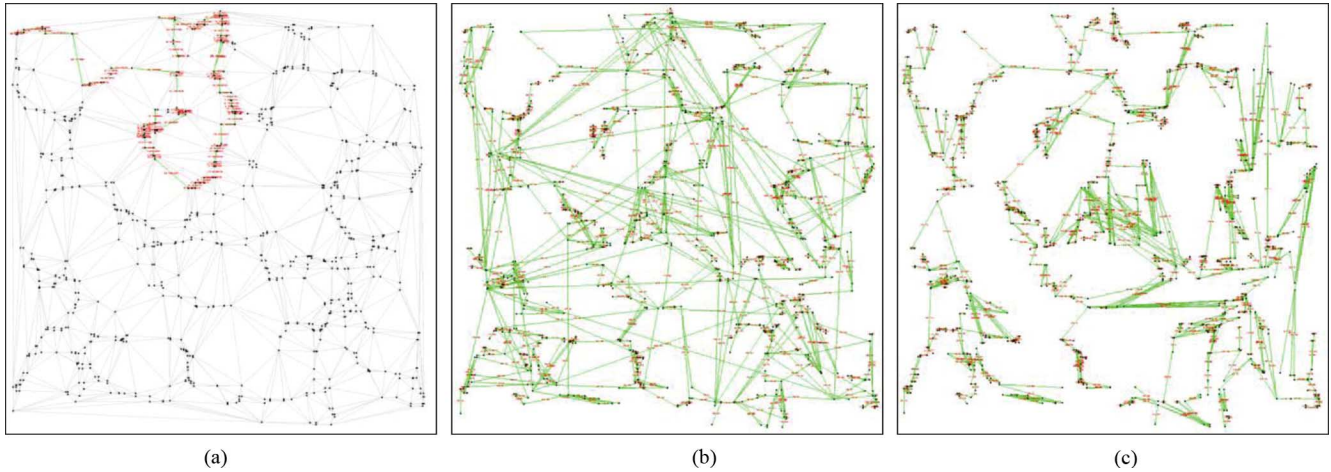


Fig. 15. RT05. (a) Reference [10]: failed. (b) Reference [11]: area = 59, 207, 240. (c) Ours: area = 37, 318, 054.

Since [10] and [11] do not handle multiple layers and obstacles, for fair comparison, experiments are conducted on planar cases without obstacles. Totally fourteen testcases are adopted. The number of terminals k (including m current sources plus n sinks) ranges from 7 to 850. The first one is directly extracted from [11] (as shown in Fig. 1). The following three are tailored as special cases. The last ten are from [28]; five are from industry, five are random. However, [28] does not have current information; we randomly inject a positive or negative current to each terminal, the current value is normally distributed within the range $[-k, +k]$. In practical cases, these values can be extracted from EM simulators. Although the numbers are random in our experiments, the optimality of our method is always guaranteed.

Table II lists the wire area consumed by the wiring topology generated by our methods and state-of-the-art works [10], [11]. Our linear programming formulation is implemented on LINGO [29], indicated by LP in Table II. Based on the greedy-choice property, our LP formulation can always deliver the global optimal solution in a relatively-short runtime, even much faster than [11], especially for large cases. Moreover, the WiT algorithm always refines *any* non-optimal solution to the global optimal. (see the shaded rows in Table II) The non-optimal solutions can be (but not limited to) [11] and our initial solution. In experiments, the number of refinement iterations depends on the initial solution quality; however, the upper bound of iterations does not. It can be seen that the number of refinement iterations for our initial solution is much fewer than that for [11], even 0 for some cases. [10] probably generates infeasible solutions especially for large cases, so we did not try to fix it. “Average ratio” is the average area ratio with respect to the optimal solution. Interestingly, it can be seen that our initial solution outperforms prior works. (On average, our initial solution [10], [11] have $1.093\times$, $1.243\times$, $1.388\times$ as large wire area as the optimal solution, respectively).

Fig. 1 lists the results for INP1 of all methods listed in Table II. Especially, our fast initial solution is optimal for INP1. Fig. 15 illustrates the results of RT05. It can be seen that [10] only connects a relatively small part for tree construction. Reference [11] can complete the wiring topology of large wire

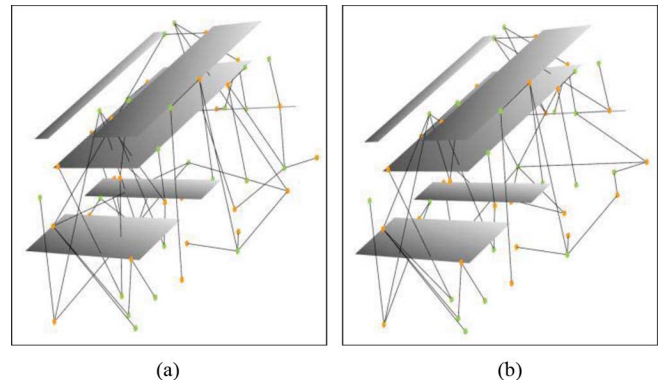


Fig. 16. ML-IND1. (a) The initial wiring topology. (b) The refined wiring topology.

area using over two hour runtime, while we can deliver the optimal solution in 90 s runtime.

Moreover, Table III lists the results for multi-layers and obstacles. Totally 10 testcases are generated based on [30]. The number of terminals ranges from 25 to 1000, the number of obstacles ranges from 6 to 100 and the number of layers ranges from 5 to 10. Here, the routing resource for a unit length wire offering one unit current is set to 1.1^{i-1} for layer i , $3.0 \times (1.1)^{j-1}$ for via j (connecting layer j and layer $j+1$). It can be seen that the average wire area reduction is 13.62%; the initial solution works well in some cases. Fig. 16 shows the initial and final wiring topologies for ML-IND1.

VII. CONCLUSION

In this paper, we focus on wiring topology generation for avoiding EM at the routing stage for analog and mixed-signal designs. The major contribution is we first claim this problem belongs to class P instead of class NP-hard. Based on the proof of the greedy-choice property, we successfully model this problem on a multi-source multi-sink flow network and solve it in a strongly polynomial time. Experimental results prove our algorithm always converges to the global optimal provided by

TABLE III
WIRING TOPOLOGY FOR MULTI-LAYERS AND OBSTACLES

Testcase	ML-IND1	ML-IND2	ML-IND3	ML-IND4	ML-IND5	ML-RT1	ML-RT2	ML-RT3	ML-RT4	ML-RT5
#Terminals	50	200	250	500	1000	25	100	250	500	1000
#Obstacles	6	85	13	100	20	10	20	50	100	100
#Layers	5	6	10	5	5	10	10	10	10	5
Initial area	949,120.1	219,356.9	10,308,177,724.0	6,001,466.5	851,561,899.4	48,880.9	188,667.3	274,162.1	1,016,955.0	4,081,496,146.4
Initial runtime (s)	0.001	0.002	0.004	0.113	0.159	< 0.001	0.001	0.004	0.022	0.149
Final area	802,913.3	180,527.4	10,308,154,616.3	5,047,351.3	679,668,175.1	42,641.3	160,425.5	230,792.3	778,771.8	4,081,249,686.1
Gain	146,206.8	38,829.5	23,107.7	954,115.2	171,893,724.3	6,239.6	28,241.8	43,369.8	238,183.2	246,460.3
#Iterations	41	446	377	1,829	3,715	20	142	498	3,203	4,656
Final runtime (s)	0.003	0.389	0.519	12.516	203.189	0.003	0.036	0.694	21.556	252.662
Impr (%)	15.40	17.70	< 0.01	15.90	20.19	12.76	14.97	15.82	23.42	0.01

Remarks: #Obstacles: number of obstacles.

#Layers: number of layers.

Impr (%): (Initial area - Final area)/(Initial area).

the exact linear programming formulation. In addition, we also extend our approach to incorporate EM avoidance with other practical issues.

APPENDIX

Here, we describe the proof of the theorem of negative cycle removal for reference as follows.

Theorem—Negative-Cycle Removal: If the flow assignment of a flow network is optimal, there exists no negative cycles in its residual network.

Proof: This theorem can be proved by contradiction. Assume flow assignment F corresponds to optimal wire area A_F for the given flow network. Suppose there is a negative cycle $C_N = \{s_i, t_j, \dots, s_i\}$ in the residual network. C_N is a cycle that starts and ends at the same source and it has a negative sum of wirelength L_C on its constituent edges. Moreover, the minimum magnitude of residual capacity among its constituent edges is chosen as the feedback flow f_f . The feedback flow f_f is injected into the negative cycle in the residual network, then the forward (backward) edges in C_N push (return) f_f flow; thus, the negative cycle is then removed. Removing the negative cycle results in an area reduction A_C

$$A_C = L_C \cdot f_f = \left(\sum_{(s_i, t_j) \in C_N \cup (t_j, s_i) \in C_N} l_{i,j} \right) \cdot \min \{c_{i,j}\} < 0. \quad (16)$$

Except the edges on the negative cycle, flows on other edges remain the same. Hence, the updated area $A'_F = A_F + A_C < A_F$, which contradicts to that A_F is optimal. In addition, after the negative cycle is removed, the total value of the updated flow assignment F' equals that of F , i.e., all currents are still completely dispatched. \square

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