Embedded I/O PAD Circuit Design for OTP Memory Power-Switch Functionality

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***Abstract*—An additional high-voltage pad is generally applied for one-time-programming (OTP) memory product applications. This may increase the complexity of input/output (I/O) pad arrangement and the area penalty. In this paper, a novel approach of I/O circuit embedded with the power-switch function is proposed for multifunction integrations in one I/O pad. The capabilities of high-voltage programming, I/O signal handling, electrostatic discharge protection and latch-up prevention for this novel circuit are well examined from silicon verifications.**

***Index Terms*—Electrostatic discharge (ESD), Neobit, one-time programming (OTP).**

I. Introduction

In system program code storages, the configuration setting, and the product identification setting can be provided by embedded non-volatile memory devices [1]–[4]. The complexity of device fabrication may lead to a low product yield and a high process cost. A new embedded one-time-programming (OTP) bit-cell (Neobit) with process compatibility was proposed in [5].

A memory-control-unit (MCU) or thin-film-transistor (TFT) panel driver integrated circuit (IC) often uses OTP memory for IC trimming. The 0.5 μm process with 5 V operation is the usual technology for such products, and is also adopted in this paper. IC circuit designers often need one extra trimming or programming pad for providing IC with two functions: a high-level voltage application at IC program mode and a normal operation voltage application at other IC operation modes. If there are high-pin counts for one IC, the extra pad cost can be neglected. However, an 8-pin MCU is the usual product to adopt for OTP memory; therefore, one extra bonding pad wastes 12.5% cost from the IC pad bonding procedure.

In order to save this programming pad, two methods are often adopted. One method uses charge-pump circuits embedded in the IC to obtain the high-level voltage. However, this methodology requires a large layout area. The other method uses power-switch circuits embedded in the IC to provide a high-level voltage for the IC programmed operation, and to provide a normal-level voltage for the OTP memory at non-programmed statuses [6]. However, such power-switch circuits also require a large layout area. For example, the layout size of power-switch circuit is the same as the OTP memory layout size in case of the 32-bit-OTP memory application.

In this paper, the power-switch circuit is embedded in one I/O bond pad [7]. The circuit designer only enlarges the I/O pad layout size slightly and then owns the power-switch function. These circuits do not need one extra pad for programming the memory. Moreover, functions of both ESD protections and latch-up immunities must be present in one I/O pad. In other words, there are four kinds of functionalities in this novel I/O bond pad: the OTP memory programmed capability, the power-switch functionality for the I/O signal process, good ESD robustness, and the latch-up immunity.

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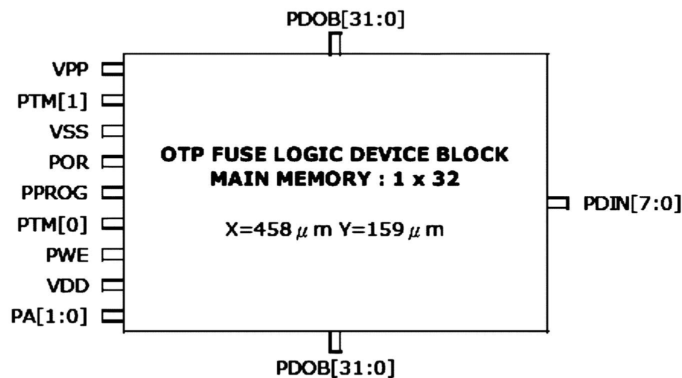

Fig. 1. IC PIN assignment.

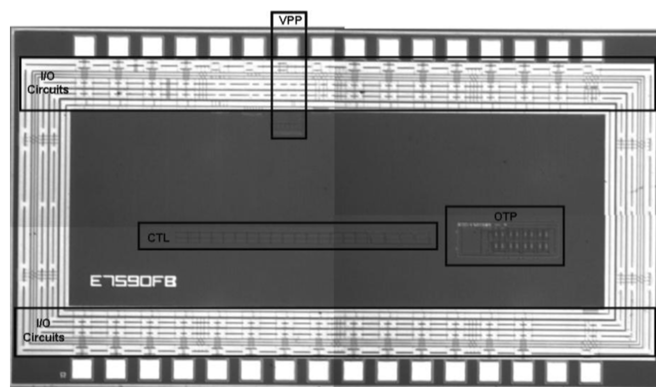

Fig. 2. IC die-photo includes OTP, CTL, and I/O circuits.

II. Memory Architecture

The traditional metal fuse and OTP memory applications were described in [8], which discussed not only Neobit structures and operations, but also Neobit program and read operations. Moreover, Neobit advantages were also included in the paper.

In addition to the program pad (VPP) for the 7.5 V operation voltage at the program mode and 5 V in the IC read cycle, many other kinds of IC pins provide suitable operation voltages, such as shown in Fig. 1. The pin VDD provides the IC power supply and the pin VSS provides the ground-level voltage. The pin PTM offers the test mode enabling function, the pin POR gives the power-on reset functionality, and the pin PPROG is applied for the program mode enabling. The pin PWE is for defining the program cycle, the pin PA is the address input, the pin PDIN is designed for the data input, and the pin PDOB is designed for the data output [9]. The IC pin has the same name as the IC bond pad. This indicates the VPP pin is connected to the VPP pad, as are the other IC pins. From the IC silicon data, 32 OTP cells can be programmed without reliability issues in this IC.

The OTP memory test chip is studied for verifying OTP memory functions; thus all signal pads must be packaged. However, in the final product application, only the VPP pin is present because the OTP memory is used as one intellectual property for the IC application. All other signal pads are controlled by logic control circuits, not connected to IC pins; therefore, ESD testing is focused on the VPP pin only. Fig. 2 illustrates the IC die-photo. There are three major circuits: 1)

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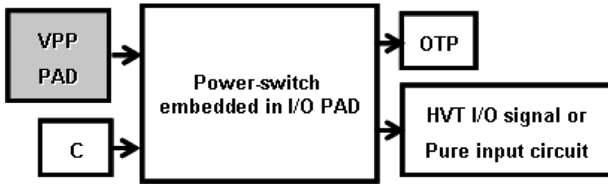

Fig. 3. Connected ports for power-switch functionalities embedded in one I/O PAD.

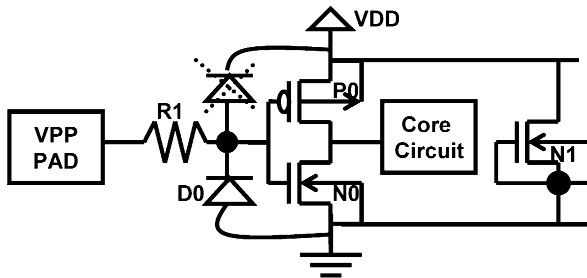

Fig. 4. Input circuit combines one gate-grounded nMOS transistor N1 together. N1 acts as the power-to-ground voltage clamping device.

the OTP control circuit (CTL); 2) the OTP memory (OTP); and 3) the I/O circuits in this test chip.

If the OTP memory is not in the program mode, the OTP cell should not be programmed. However, when ESD currents arrive at the IC, the memory cells are likely charged. If the OTP cell has not been programmed but appears to be programmed, this phenomenon is called the false-program issue. Furthermore, latch-up can induce a high-level voltage that can be larger than the program voltage; therefore it can also falsely program the memory cells. Both ESD and latch-up events can induce OTP memories to be falsely programmed. In this study, both issues are solved and are discussed in Section IV.

III. I/O Circuit and Function Block Description

The connected ports of this I/O pad are illustrated in Fig. 3. There are two input ports: VPP and C. There are also two output ports: one for the OTP memory and one for the high-voltage tolerant (or pure input) circuit. The architecture for handling this VPP pad voltage must be high-voltage-tolerant (HVT) circuits [10] because the VPP pad must provide 7.5 V, which is larger than the 5 V of the VDD. HVT circuits must be used for the 5 V transistors if the applied voltage is 7.5 V. This is different from the 3.3 V transistors under the 5 V applications, although the similar circuit architecture can be utilized. The details of these circuits are not discussed in this study. If circuit designers are unwilling to create such complicated circuits for HVT circuits, pure input circuits without output-driving capabilities and pull-up charge device model (CDM) diodes are recommended, as shown in Fig. 4. The pull-up CDM diode can not be implemented for avoiding programming leakage currents from the VPP pad to VDD. The pull-up CDM charges must be dissipated through the power clamping nMOS transistor, N1.

There are nine function blocks in this I/O circuit, as illustrated in Fig. 5. The OTP memory is shown as the block "OTP" and the I/O port is shown as the block "HVT I/O signal or Pure input circuit." Terminal C can provide low-level voltage at the ESD mode and high-level voltage at I/O and latch-up modes. Block 1 illustrates the ESD protection device in a large layout size. In order to prevent ESD currents entering the OTP memory, Block 2 instructs the ESD avoiding circuits [11]. The traditional ESD protection circuit with the gate-grounded nMOS transistors needs a very large triggering-on voltage; thus, gate-driven circuits with power-up reset circuits [12] are adopted in Block 3 to reduce the ESD device turn-on voltage. For reducing ESD device leakage currents under the IC power-up period, Block 4 is composed of control circuits to reach this target. Moreover, trace-high circuits are included in Block 5 to provide Terminal H a higher-level voltage between VPP and VDD [13]. For transmitting the Terminal C voltage to the VPP pad applied voltage, Block 6 holds the level-shifter circuit. In addition, Block 7 has the voltage pull-high function for providing the OTP memory with the VDD voltage. Block 8 is designed for controlling Block 7. Finally, Block 9 provides one capacitor to store ESD coupling charges. The capacitor can maintain the same voltage as the ground terminal VSS under ESD stresses.

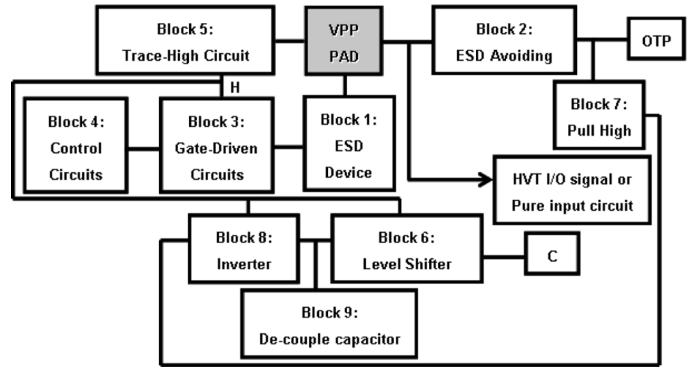

Fig. 5. I/O pad function block diagram.

Fig. 6 illustrates the physical circuits of this study. Block 1 is composed of the ESD nMOS transistor N1 for ESD current dissipations. Block 2 is composed of the ESD avoiding pMOS transistors P1 and P2. P1 can control VPP pad signal to the OTP memory and P2 can stop ESD currents from entering the OTP memory. Block 3 is composed of the pMOS transistor P3, the nMOS transistor N2, the nMOS capacitor N3, and the resistor R1 to form the gate-driven circuits; R1 and N3 form a power-up delay time. Block 4 consists of one PMOS transistor P4 that has one feedback signal from the N1 gate terminal G1 to control the P4 gate terminal. Under normal operations, P4 can turn on to connect Terminal H and Terminal G2 together to reduce the power-up leakage currents. In contrast, P4 can turn off to delay the terminal G2 power-up time at ESD events; thus, G1 can keep a high-level voltage to make N1 turn-on for satisfactory ESD current dissipation. Block 5 is made up of two pMOS transistors P5 and P6. Both N-wells of P5 and P6 are connected to the trace-high Terminal H. The gate terminals of P5 and P6 are cross-connected to VPP and VDD. Terminal H is powered-up to a higher-level voltage of VPP and VDD. Block 6 is a level-shifter circuit that consists of two pMOS transistors, P7 and P8, two nMOS transistors, N4 and N5, and one inverter composed of one pMOS transistor, P9, and one nMOS transistor, N6. For this level shifter circuit, N-well terminals of both P7 and P8 are connected to the trace-high Terminal H, which forces Terminal C1 to follow the high-level voltage for turning P1 off under ESD stresses. Block 7 is made up of one PMOS transistor, P10, for providing the OTP memory with one VDD voltage at IC normal (non-programmed) operations. Block 8 is one inverter made up of one PMOS transistor, P11, and one nMOS transistor, N7. The P11 N-well is connected to the terminal H for tracing the high-level voltage. This block provides one terminal C2 voltage for controlling the P10 gate terminal. C2 can turn P10 on at IC normal operations whereas it can turn P10 off at the IC non-program mode. Finally, in order to keep the terminal C2 at a high-level voltage to turn P10 off at ESD stresses, Block 9 consists of one NMOS capacitor, N8.

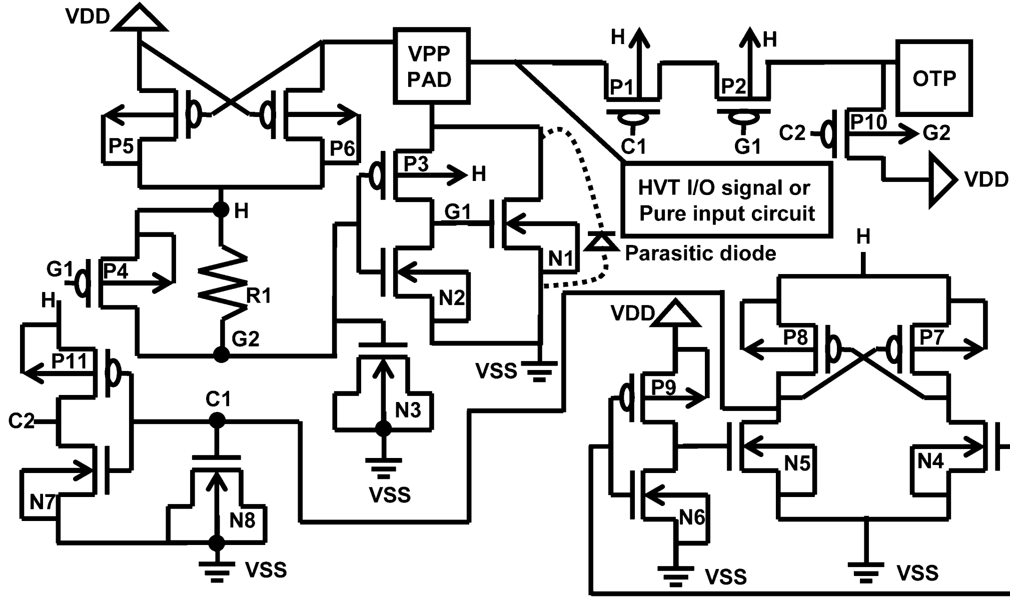

Fig. 6. I/O pad physical circuit.

IV. IC Operation Analysis

There are four kinds of IC operation modes: 1) the program mode that programs OTP memories; 2) the I/O mode wherein I/O signal enters other circuits (not OTP memories) through the VPP pad, and the OTP memory (tied to one power supply); 3) the ESD mode that tests IC ESD robustness; and 4) the latch-up mode that tests IC the latch-up immunity.

For the IC program mode, VPP pad is tied to 7.5 V and VDD is operated at 5 V; therefore, Terminal H is traced to 7.5 V through P6. The pMOS transistor P5 is turned off because its gate terminal is connected to 7.5 V. The P4 gate terminal G1 is connected to the output terminal of the inverter circuit; thus, G1 voltage tends to be low-level. This low-level G1 voltage will tend to turn P4 on and then trigger G2 to follow H. A higher-level G2 voltage will push G1 to a lower-level voltage through the inverter circuit. Thus, G1 and G2 feed each other, and then G2 can follow H (@7.5 V) quickly; it does not need to go through R1 (in several kiloΩ). G1@0 V turns N1 off; therefore, the ESD nMOS transistor N1 will not induce a large current. Furthermore, the terminal C voltage is provided from the internal control circuit and tied to 0 V. Thus, C1 is also at 0 V through the level-shifter circuit. Then, C2 is tied to 7.5 V. Both C1 and G1 are at 0 V and both N-well terminals of P1 and P2 are at 7.5 V; therefore, the VPP pad voltage @7.5 V can be transmitted to the OTP memory. Moreover, C2 (@7.5 V) can turn P10 off; therefore, the 5 V VDD will not be connected to the OTP memory. In brief, P1 and P2 are turned on to transmit the VPP pad voltage to program OTP memory, N1 is turned off to avoid a large leakage current, and P10 is turned off to disconnect VDD and the OTP memory.

For the I/O mode, the VPP pad is operated between 0 and 5 V; therefore Terminal H can be traced to 5 V. Terminal G2 follows Terminal H to reach 5 V through the feedback pMOS transistor P4, and then forces Terminal G1 at 0 V for turning N1 off. Terminal C is tied to 5 V from the logic control circuit; therefore, C1 is at 5 V to turn P1 off and C2 is at 0 V to turn P10 on. To summarize the above descriptions, P10 is turned on to transmit 5 V to the OTP memory. N1 is turned off to avoid a large leakage current. P1 is turned off to prevent the VPP pad signal from disturbing the OTP memory. The VPP pad signal can then enter other circuits.

For the ESD testing, the VPP pad is under ESD stresses, VSS is at 0 V, and the other pads are floating. Negative ESD charges are easily dissipated by the parasitic diode of N1; therefore, only positive ESD charges are discussed here. Zero voltage charges are stored in the NMOS capacitor N3 between VSS and the terminal G2 at the ESD event period (approximately 250 ns [14]). Then, Terminal G1 traces the ESD voltage through the inverter (P3 and N2). This can turn N1 on for forming the gate-driven effect in order to reduce the N1 ESD turn-on voltage. Thus, high-level-voltage G1 turns P2 off to prevent ESD currents from entering the OTP memory. It also turns P4 off to keep the capacitor N3 in a low-level voltage. Terminal C1 can be kept at a low-level voltage through the nMOS capacitor N8. Thus, C2 is tied to the ESD-level voltage and then turn P10 off to prevent ESD charges from damaging the OTP memory via the VDD pad. Briefly, N1 is turned on for ESD dissipations; however, both P2 and P10 are turned off to prevent ESD currents from entering the OTP memory.

P4 can be kept off in 1000 ns whereas it can be turned on after 1000 ns because R1*N3 time constant is approximately 1000 ns. The power-up time of the OTP memory program, the IC latch-up immunity testing, and the I/O signal operation are longer than 1000 ns; thus, P4 can be turned off at the ESD mode, but can be turned on at other modes.

Latch-up is an electrical overstress test for IC normal operation functionality. The program voltage 7.5 V is for programming the OTP memory; thus, the voltage is not for the latch-up testing. In the latch-up testing, the normal operation voltage is 5 V; the maximum operation voltage is 5.5 V. Thus, 8.25 V ($= 1.5\times$ 5.5 V) [15] is chosen for the latch-up testing. Both VDD and the terminal C are offered at 5 V. Terminal H is traced to 8.25 V through P6. G2 is raised to 8.25 V and G1 is pulled down at 0 V. N1 is subsequently turned off. Furthermore, C1 is tied to 8.25 V through the level shifter circuit; C2 is then at 0 V. C1 @8.25 V turns P1 off and C2 @0 V turns P10 on; thus, the 5 V of VDD is transmitted to the OTP memory. Therefore, the OTP memory will not be falsely programmed.

Every terminal voltage of the above analyses under the IC program mode, the I/O mode, and the latch-up mode are simulated through the H-Spice tool. The simulated results are shown in Fig. 7. The voltage of OTP terminal can reach 7.5 V at the programming mode and is maintained at 5 V under the I/O and latch-up modes.

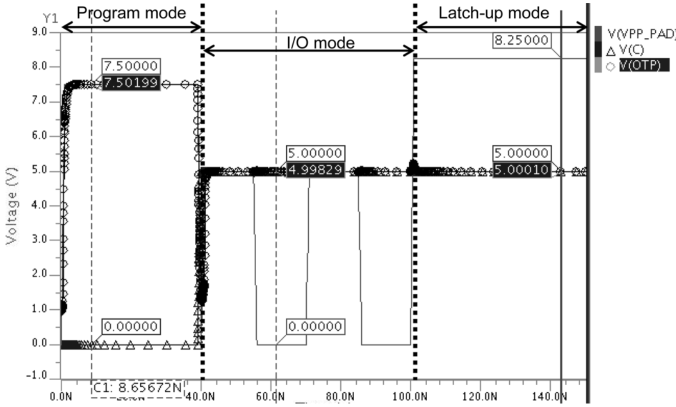

Fig. 7. I/O pad simulation results for memory program, I/O, and latch-up modes.

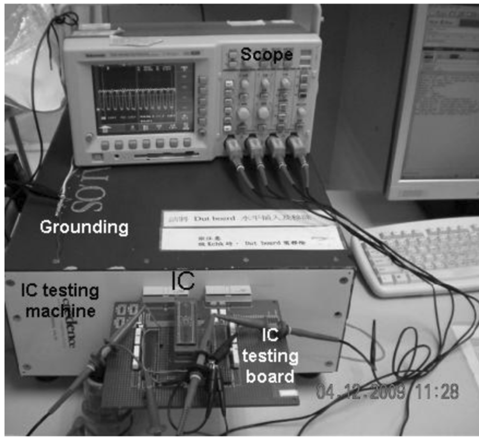

Fig. 8. IC testing environment.

TABLE I
OTP PROGRAM CURRENT RESULTS

Power/ VPP voltage	Pin current name	Stand-by and programmed currents (μ A)		
		Sample 1	Sample 2	Sample 3
VDD =4.5V	Ivdd	0.272	0.273	0.269
VDD2=4.5V	Ivdd2	0.053	0.072	0.051
VPP =7.25V	Ivpp	3456.93	3495.07	3458.45
VDD =5V	Ivdd	0.284	0.285	0.281
VDD2=5V	Ivdd2	0.055	0.047	0.061
VPP =7.5V	Ivpp	3380.63	3458.45	3401.23
VDD =5.5V	Ivdd	0.275	0.285	0.279
VDD2=5.5V	Ivdd2	0.074	0.058	0.063
VPP =7.75V	Ivpp	3678.18	3716.33	3682.76

IC spec: Ivdd and Ivdd2 < 1μ A and Ivpp < 4.8mA@ temperature= 25℃.

TABLE II
PIN CURRENTS UNDER THE I/O SIGNAL OPERATION

Power/ VPP voltage	Pin current name	Stand-by current (μ A)		
		Sample 1	Sample 2	Sample 3
VDD =5.5V	Ivdd	0.096	0.09	0.088
VDD2=5.5V	Ivdd2	0.084	0.078	0.083
VPP @ 10MHz	Ivpp	0.003	0.003	0.003
VDD =5.5V	Ivdd	0.09	0.091	0.087
VDD2=5.5V	Ivdd2	0.001	0.001	0.004
VPP @ 33MHz	Ivpp	0.011	0.01	0.003
VDD =5.5V	Ivdd	0.091	0.088	0.089
VDD2=5.5V	Ivdd2	0.003	0.007	0.005
VPP @ 50MHz	Ivpp	0.006	0.002	0.001

IC spec: Ivdd, Ivdd2 and Ivpp < 1μ A @temperature= 25℃.

TABLE III
PIN CURRENTS AFTER ESD STRESSES

ESD Event	POWER/ VPP VOLTAGE	Pin current name	Stand-by and read current (μ A)	
			Sample 1	Sample 2
VPP-VDD	VDD =5.5V	Ivdd	0.118	0.116
(HBM	VDD2=5.5V	Ivdd2	0.042	0.045
+/- 2.5kV)	VPP =5.5V	Ivpp	0.033	0.019
VPP-VSS	VDD =5.5V	Ivdd	0.123	0.12
(HBM	VDD2=5.5V	Ivdd2	0.046	0.042
+/- 2.5kV)	VPP =5.5V	Ivpp	0.025	0.027
VPP-VDD	VDD =5.5V	Ivdd	0.113	0.12
(MM	VDD2=5.5V	Ivdd2	0.033	0.033
+/- 250V)	VPP =5.5V	Ivpp	0.039	0.035
VPP-VSS	VDD =5.5V	Ivdd	0.111	0.116
(MM	VDD2=5.5V	Ivdd2	0.043	0.046
+/- 250V)	VPP =5.5V	Ivpp	0.024	0.094

IC spec: Ivdd, Ivdd2 and Ivpp < 1μ A @temperature= 25℃.

TABLE IV
PIN CURRENTS AFTER LATCH-UP STRESSES

Latch-up Event	POWER/ VPP VOLTAGE	Pin current name	Stand-by and read Current (μ A)	
			Sample 1	Sample 2
	VDD =5.5V	Ivdd	0.108	0.114
+IT	VDD2=5.5V	Ivdd2	0.033	0.035
(200mA)	VPP =5.5V	Ivpp	0.028	0.037
-IT	VDD =5.5V	Ivdd	0.111	0.111
(200mA)	VDD2=5.5V	Ivdd2	0.037	0.033
	VPP =5.5V	Ivpp	0.037	0.032
+VT	VDD =5.5V	Ivdd	0.109	0.118
(8.25V)	VDD2=5.5V	Ivdd2	0.04	0.042
	VPP =5.5V	Ivpp	0.033	0.028

IC spec: Ivdd, Ivdd2 and Ivpp < 1μ A @temperature= 25℃.

V. EXPERIMENTAL RESULT

The IC testing environment is illustrated in Fig. 8. IC is installed in the testing board, and then the testing board is connected to the testing machine. In order to investigate VPP pad waveform, one scope is connected to IC. VDD is the OTP memory power, VDD2 is the I/O power and VPP is the VPP pad voltage, as shown in Tables I–IV. The corresponding currents are Ivdd, Ivdd2, and Ivpp.

First, the OTP memory can be programmed under the IC program mode; the programmed currents are listed in Table I. In order to obtain IC operation margins, three kinds of programming voltages are applied: 7.25 V ($@\mathrm{VDD} = \mathrm{VDD2} = 4.5$ V), 7.5 V ($@\mathrm{VDD} = \mathrm{VDD2} = 5$ V) and 7.75 V ($@\mathrm{VDD} = \mathrm{VDD2} = 5.5$ V). The OTP memories can be programmed appropriately, and the bit current approximates to 400 μA because the OTP memory is programmed at 8 bits per program cycle. Second, three kinds of frequencies are applied for the I/O functionality testing; the results are listed in Table II. If the I/O circuits are wrong, there will be huge leakage currents from the power terminals. However, the full-chip stand-by current is smaller than 1 μA; thus, IC can work well. In other words, this new circuit architecture provides the OTP memory with 5 V and allows the I/O signal to be transmitted to other circuits under I/O operations.

In order to check for the existence of falsely programmed issues in OTP memory, OTP memories are not programmed before ESD and latch-up stresses. The power stand-by currents (Ivdd and Ivdd2) and

the VPP pad current (Ivpp) are therefore smaller than 1 μA before two kinds of stresses. Table III illustrates ESD testing results of two IC pin combinations, VPP-VDD and VPP-VSS. ESD currents flow from the VPP pad to the VDD or VSS pad (VDD and VSS in 0 V), respectively. ESD testing results show this test-chip can pass human body mode (HBM) in 2.5 kV and machine mode (MM) in 250 V without OTP memory false-programmed issues. Finally, Table IV shows that there are no falsely-programmed events under latch-up overstress conditions. Regardless of whether there are positive/negative current stresses $(+\mathrm{IT}/-\mathrm{IT})$ 200 mA or positive voltage stress $(+\mathrm{VT})$ 8.25 V, this test-chip can successfully pass the latch-up testing criteria [15], and its power and VPP pad currents can be kept smaller than 0.2 μA.

VI. Conclusion

After silicon data verification, this new circuit architecture has been proven to provide power-switch functions in one I/O pad very well. Both functions of programming the OTP memory and processing the I/O signal can work well. Circuit designers can adopt this scheme to save one bonding pad. Furthermore, the functionalities of ESD protection and latch-up prevention for the IC product can also be approached.

This architecture can be applied for all technologies, and a similar architecture has also been proved in the micro-electro-mechanical-systems product processed in 0.18 μm.

Acknowledgment

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Analog Implementation of a Novel Resistive-Type Sigmoidal Neuron

Golnar Khodabandehloo, Mitra Mirhassani, and Majid Ahmadi

***Abstract*—An important part of any hardware implementation of artificial neural networks (ANNs) is realization of the activation function which serves as the output stage of each layer. In this work, a new NMOS/PMOS design is proposed for realizing the sigmoid function as the activation function. Transistors in the proposed neuron are biased using only one biasing voltage. By operating in both triode and saturation regions, the proposed neuron can provide an accurate approximation of the sigmoid function. The neuron circuit is designed and laid out in 90-nm CMOS technology. The proposed neuron can be potentially used in implementation of both analog and hybrid ANNs.**

***Index Terms*—Activation function, analog neuron, sigmoid function, sigmoidal neuron.**

I. Introduction

Artificial neural networks (ANNs) are used in a wide range of applications from signal processing systems to miscellaneous control devices [1]–[5]. Realization of activation function of neurons is one of the major challenges in hardware implementation of ANNs.

Both digital and analog modules can be used to realize the activation function in hardware implementations depending on the type of the neural network. Neural networks can be generally categorized into three groups: digital, analog, and hybrid (mixed-signal) neural networks.

In digital neural networks, both synaptic weight storage cells and activation function are realized by digital gates such as lookup tables (LUTs) which are generally used to approximate the activation function [6]–[8]. In analog neural networks, on the other hand, analog circuits are used both to estimate the activation function and to store the synoptic weights [1], [9]–[11].

The third group of neural networks are hybrid neural networks (HNNs) which are a combination of digital and analog gates [4], [5], [12]–[20]. In HNNs, analog circuits are employed to realize the activation function while weights are stored digitally.

Area and power consumption of analog activation functions are generally less than that of digital implementations [11], [17]–[19]. However, analog circuits are more vulnerable to mismatch and process violations. In addition, digital implementation usually results in a better estimation of the ideal activation function. Consequently, it is important to make analog implementation of neurons more accurate to profit from both an area/power efficient design and an appropriate realization at the same time.

Activation function produces the output of each layer in the feed forward neural networks according to the value of its input. Several activation functions are generally used such as step function, tangent hyperbolic and sigmoid function. The last two ones are nonlinear functions which generate an S shaped curve. In this work, the sigmoid function is realized with an output between 0 and 1.

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