New Design of 2 × VDD-Tolerant Power-Rail ESD Clamp Circuit for Mixed-Voltage I/O Buffers in 65-nm CMOS Technology

Chih-Ting Yeh and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—A new 2 × VDD-tolerant power-rail electrostatic discharge (ESD) clamp circuit realized with only thin gate oxide 1-V (1 × VDD) devices and a silicon-controlled rectifier (SCR) as the main ESD clamp device has been proposed and verified in a 65-nm CMOS process. This new design has a low standby leakage current by reducing the voltage difference across the gate oxide of the devices in the ESD detection circuit. The proposed design with an SCR width of 50 μm can achieve a 6.5-kV human-body-model ESD level, a 300-V machine-model ESD level, and a low standby leakage current of only 103.7 nA at room temperature under the normal circuit operating condition with 1.8 V bias.**

***Index Terms*—Electrostatic discharge (ESD), holding voltage, mixed-voltage I/O buffers, power-rail ESD clamp circuit.**

I. Introduction

THE system-on-a-chip (SoC) has become popular because the number of transistors in a chip is aggressively increasing with the continuously progressed CMOS technology. The gate oxide thickness has been shrunk to improve circuit operating speed for such SoC applications. The power supply voltage has been also scaled down to reduce power consumption. However, for SoC integration, the I/O circuits with low-voltage devices may receive or drive high-voltage signals to communicate with other ICs in microelectronic systems. Therefore, the chip-to-chip mixed-voltage I/O interfaces are required in the microelectronic systems with different power supply voltages [1]–[3].

However, the mixed-voltage I/O interfaces must be designed to prevent undesired leakage current paths [4] and electrical overstress on the gate oxide [5]. In order to solve the gate oxide reliability issue without using the additional thick gate oxide devices, the stacked-MOS configuration had been widely used for mixed-voltage I/O circuits to reduce the process complexity and fabrication cost [6], [7]. However, those prior designs did not consider the gate leakage current if such circuits were further implemented in nanometer CMOS processes. In nanometer CMOS technologies, the gate leakage current must be considered during circuit design. Therefore, some designs on high-voltage-tolerant power-rail electrostatic discharge (ESD) clamp circuit have been recently revealed to reduce the standby leakage current in nanometer CMOS technologies [8], [9].

In this brief, a new low-leakage 2 × VDD-tolerant power-rail ESD clamp circuit realized with only thin gate oxide devices for mixed-voltage I/O applications is investigated in 65-nm CMOS technology. By using this new circuit solution, the standby leakage current of a 2 × VDD power-rail ESD clamp circuit can be successfully achieved on the order of nanoamperes under the normal circuit operating condition.

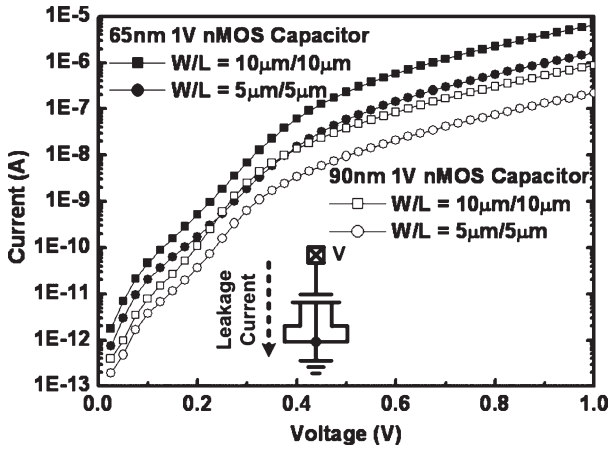

Fig. 1. Simulated gate currents of the nMOS capacitors in 65- and 90-nm CMOS technologies.

II. New Design of 2 × VDD-Tolerant Power-Rail ESD Clamp Circuit

A. Gate Leakage Current in Nanoscale CMOS

When the gate oxide thickness is continuously scaled down in advanced CMOS technology, the gate leakage current has become an inevitable issue. The gate current of the nMOS capacitor is directly dependent on the polygate area and the gate oxide thickness. Based on the BSIM4 model [10] with the device parameters provided from foundry, the gate currents of the nMOS capacitors in 65- and 90-nm CMOS technologies are compared in Fig. 1. The gate currents of the nMOS capacitors with W/L of 5 μm/5 μm and 10 μm/10 μm are 217 and 878 nA

Manuscript received June 8, 2011; revised October 21, 2011 and November 30, 2011; accepted January 9, 2012. Date of publication February 15, 2012; date of current version March 16, 2012. This work was supported in part by the National Science Council of Taiwan under Contract NSC 98-2221-E-009-113-MY2, by the Ministry of Economic Affairs of Taiwan under Project A352BA1130, and by the "Aim for the Top University Plan" of National Chiao Tung University and the Ministry of Education, Taiwan. This paper was recommended by Associate Editor K. Chakrabarty.

C.-T. Yeh is with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the Information and Communications Research Laboratories, Industrial Technology Research Institute, Hsinchu 310, Taiwan.

M.-D. Ker is with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the Department of Electronic Engineering, I-Shou University, Kaohsiung 840, Taiwan.

Digital Object Identifier 10.1109/TCSII.2012.2184372

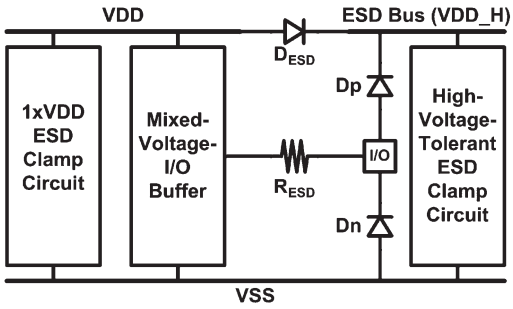

Fig. 2. ESD protection scheme with an on-chip ESD bus for high-voltage-tolerant mixed-voltage I/O buffer.

(1.61 and 6.48 μA) at 1 V in 90-nm (65-nm) technology, respectively. The gate leakage issue in 65-nm CMOS technology is much worse than that in 90-nm CMOS technology due to the thinner gate oxide.

B. ESD Protection Scheme for Mixed-Voltage I/O Buffer

In order to receive the input signals with a 2 × VDD voltage level, the traditional ESD protection design with a direct diode connection from the I/O pad to the power line of 1 × VDD is inappropriate. The ESD protection scheme with an ESD bus and a high-voltage-tolerant ESD clamp circuit for the IC with mixed-voltage I/O interfaces has been reported [7]. The ESD protection scheme for high-voltage-tolerant mixed-voltage I/O buffer is shown in Fig. 2, which is realized with the ESD diodes, the ESD bus, the 1 × VDD ESD clamp circuit, and the high-voltage-tolerant ESD clamp circuit.

For a positive ESD stress zapping at the I/O pad with grounded VSS, the ESD current can be discharged through diode Dp to the ESD bus and then through the high-voltage-tolerant ESD clamp circuit to VSS. For a positive ESD stress zapping at the I/O pad with grounded VDD, the ESD current can be discharged through diode Dp, the ESD bus, the high-voltage-tolerant ESD clamp circuit, the VSS line, and the 1 × VDD ESD clamp circuit. For a negative ESD stress zapping at the I/O pad with grounded VSS, the ESD current can be discharged through diode Dn in the forward-biased condition. For a negative ESD stress zapping at the I/O pad with grounded VDD, the ESD current can be discharged through diode Dn to the VSS line and then through the 1 × VDD ESD clamp circuit to VDD. Therefore, the four modes of the ESD test at the I/O pad with the relatively grounded VDD or VSS in the mixed-voltage I/O buffer can be well protected by this ESD protection scheme.

C. New 2 × VDD-Tolerant Power-Rail ESD Clamp Circuit

The proposed 2 × VDD-tolerant power-rail ESD clamp circuit with the substrate-triggered silicon-controlled rectifier (SCR) device as the main ESD clamp device is shown in Fig. 3. The cross-sectional view of the substrate-triggered SCR device [11] is also illustrated in Fig. 4. The SCR device without the polygate structure is free from the gate leakage problem. The ESD detection circuit is necessary to improve the turn-on speed of the SCR device with a substrate-triggered mechanism under the ESD stress condition. Therefore, the ESD detection circuit

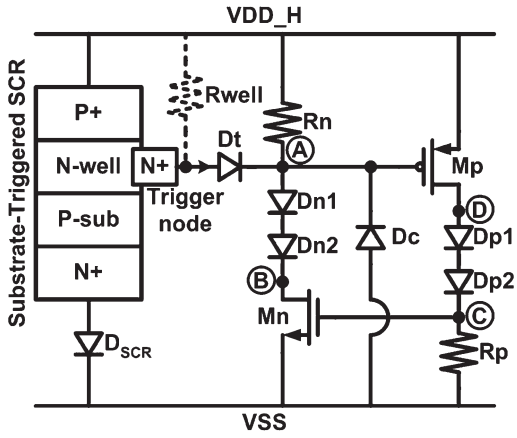

Fig. 3. Proposed 2 × VDD-tolerant power-rail ESD clamp circuit with the substrate-triggered SCR as the ESD clamp device.

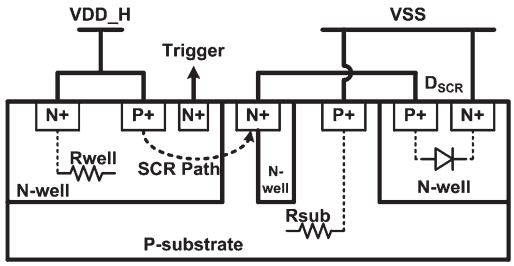

Fig. 4. Cross-sectional view of the ESD clamp device composed of the substrate-triggered SCR device and cascode diode $D_{\rm SCR}$.

realized with only thin gate oxide 1 × VDD devices for 2 × VDD-tolerant applications is designed with considerations of gate leakage current and gate oxide reliability. The main design concept is to reduce the voltage difference across the gate oxide of the devices in the ESD detection circuit. By inserting the diode strings in the ESD detection circuit to reduce the voltage differences across the gates of the MOS transistors, the gate leakage currents of the nMOS and pMOS in the ESD detection circuit can be well controlled to minimize the total standby leakage current.

The purpose of the ESD detection circuit is to keep the SCR device at OFF-state under the normal circuit operation condition and to trigger on the SCR device during the ESD stress event. The detailed descriptions on ESD detection circuit operations are shown in Sections II-D and II-E.

In Fig. 3, Mn is used to conduct the triggering current from the trigger node (the anode of diode Dt in Fig. 3) of the SCR device during the ESD stress event. Under the normal circuit operating condition, Mp and Mn are kept off through resistors Rn and Rp, respectively. There is no triggering current conducting from the trigger node due to the turned-off Mn. Therefore, the SCR device is kept off during the normal circuit operating condition. The RC-based ESD transient detection mechanism is realized by Rn and reverse-biased diode Dc, which can distinguish the ESD stress event from the normal power-on condition. Compared with the thin gate oxide of the MOS transistor in the traditional RC circuit, the reverse-biased diode Dc in the proposed ESD detection circuit has no gate leakage issue. Cascode diode $D_{\rm SCR}$ is used to increase the holding voltage of the ESD clamp device to avoid the transient-

TABLE I
DESIGN PARAMETERS OF THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT

Design Parameters			
Rp (Ω)	1.9k		
Rn (Ω)	25k		
Mp (W/L)	4μm / 0.12μm		
Mn (W/L)	40μm / 0.12μm		
Dp1 & Dp2 (μm^2)	1.14		
Dn1 & Dn2 (μm^2)	24.40		
Dc (μm^2)	156.75		
Dt (μm^2)	24.40		
Widths of D_{SCR} (μm)	30	40	50
Widths of SCR (μm)	30	40	50

induced latchup issue [12]. With a total holding voltage greater than the specified voltage level (2 × VDD), the latchup issue from the SCR used as the ESD clamp device in this work can be completely solved. Additional diode Dt is used to block the connection between Rn and parasitic n-well resistor Rwell in the SCR device for not affecting the RC time constant at node A. The other diodes, namely, Dn1, Dn2, Dp1, and Dp2, are used to reduce the voltage difference across the gate oxide of Mn and Mp in the ESD detection circuit.

D. Operation Under the Normal Circuit Operating Condition

During the normal circuit operating condition with VDD_H of 1.8 V and grounded VSS, the gate voltage of Mp is biased at 1.8 V through resistor Rn. The gate voltage of Mn is biased at 0 V through resistor Rp. Because Mn is turned off, no triggering current is conducted from the trigger node of the SCR device. By inserting the diode strings into the ESD detection circuit, the drain-to-gate and drain-to-source voltages of Mp and Mn can be controlled to be less than 1 V. Therefore, the standby leakage current can be effectively reduced. In addition, all 1-V devices in the proposed ESD detection circuit are free from the gate oxide reliability issue under the normal circuit operating condition.

According to the device dimensions listed in Table I, the simulated voltage waveforms of the proposed ESD detection circuit during the normal power-on transition are shown in Fig. 5. VDD_H is powered up from 0 to 1.8 V with a rise time of 1 ms. In Fig. 5, it is obvious that the gate-to-drain and drain-to-source voltages of all devices do not exceed the 1 × VDD (1-V) range. Therefore, the proposed ESD detection circuit would not suffer the gate oxide reliability issue under the normal circuit operating condition.

E. Operation Under the ESD Transient Event

When a positive ESD-like fast-transient voltage is applied to VDD_H with grounded VSS, the RC time delay would keep node A at a relatively low voltage level, as compared with that at VDD_H. Mp can be quickly turned on to elevate the voltage level of node C. When the voltage level of node C is higher than the threshold voltage of Mn, Mn can be turned on to conduct the triggering current from the trigger node of the SCR device and pull down the voltage level of node A at the same time. Therefore, the proposed ESD detection circuit with the positive feedback mechanism can be continuously turned on to conduct the triggering current during the ESD transient event.

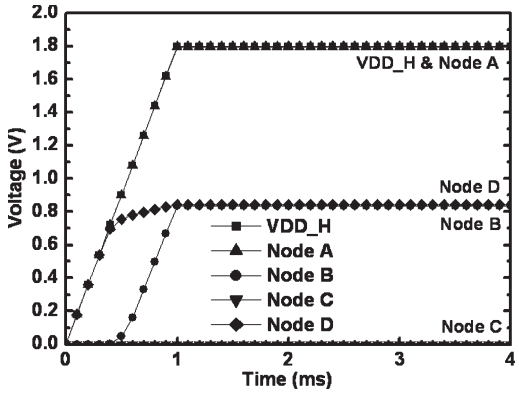

Fig. 5. Simulated voltage waveforms at the nodes of the ESD detection circuit under the normal power-on condition with VDD_H of 1.8 V and a rise time of 1 ms.

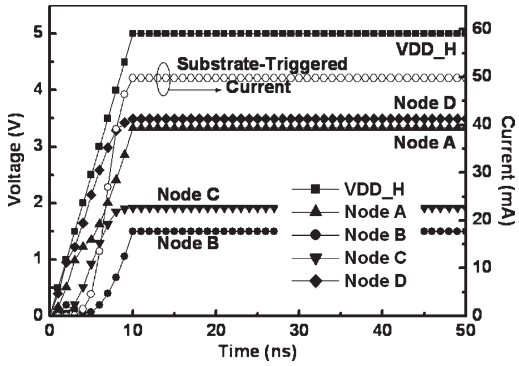

Fig. 6. Simulated voltage waveforms at the nodes and the substrate-triggered current of the ESD detection circuit under the ESD-like transition condition with VDD_H of 5 V and a rise time of 10 ns.

In order to simulate the fast-transient edge of the human-body-model (HBM) [13] ESD event before the breakdown on the ESD protection devices, a 5-V voltage pulse with a rise time of 10 ns is applied to VDD_H. The simulated transient voltage waveforms and the triggering current of the ESD detection circuit during the ESD transition are illustrated in Fig. 6. Mn in the ESD detection circuit can be continuously turned on to conduct the triggering current from the SCR device due to the positive feedback mechanism. Finally, the SCR device is fully turned on to discharge the ESD current from VDD_H to VSS.

III. EXPERIMENTAL RESULTS

The new proposed 2 × VDD-tolerant power-rail ESD clamp circuits have been fabricated in a 65-nm fully silicided CMOS process by using only 1-V devices. The widths of SCR devices in the power-rail ESD clamp circuit are split into 30, 40, and 50 μm to verify the corresponding ESD robustness. In order to avoid the ESD failure location occurring at $D_{\rm SCR}$, the junction width of $D_{\rm SCR}$ and the width of the SCR are kept the same, as listed in Table I. These power-rail ESD clamp circuits are fabricated for dc $I-V$ measurement, transmission-line pulsing (TLP) measurement, ESD test, and turn-on verification measurement. In this brief, each proposed circuit was zapped three times at every ESD voltage step from three separated dice.

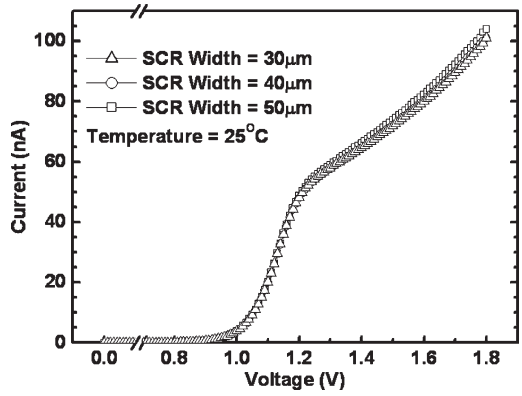

Fig. 7. Measured dc $I-V$ curves of the 2 × VDD-tolerant power-rail ESD clamp circuit with different SCR widths.

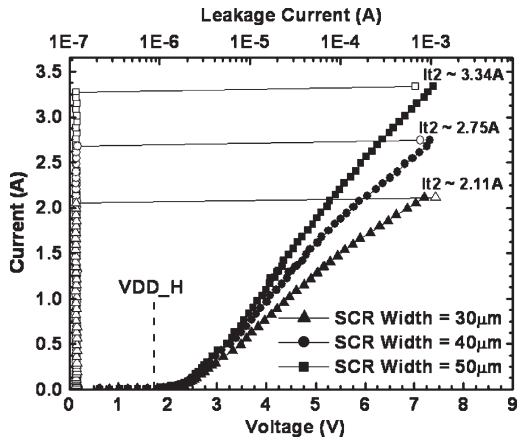

Fig. 8. TLP-measured curves of the fabricated 2 × VDD-tolerant power-rail ESD clamp circuit with different SCR widths.

TABLE II
ESD ROBUSTNESS AND LEAKAGE CURRENT OF THE FABRICATED POWER-RAIL ESD CLAMP CIRCUITS WITH DIFFERENT SCR WIDTHS

2×VDD-Tolerant Power-Rail ESD Clamp Circuit		SCR Width (μm)		
		30	40	50
It2 (A)		2.11	2.75	3.34
HBM ESD Level (kV)		3.5	5.0	6.5
MM ESD Level (V)		150	250	300
Leakage Current (VDD_H = 1.8V)	25°C	100.6nA	101.4nA	103.7nA
	125°C	4.72μA	4.73μA	4.74μA

A. DC $I-V$ Measurement

The dc $I-V$ characteristic of the fabricated 2 × VDD-tolerant power-rail ESD clamp circuit measured by HP4155 from 0 to 1.8 V with the voltage step of 10 mV is shown in Fig. 7. Under the normal operating voltage of 1.8 V, the leakage currents of the fabricated 2 × VDD-tolerant power-rail ESD clamp circuits at different temperatures are listed in Table II. For example, the proposed circuit with the SCR width of 40 μm at the temperature of 25 °C (125 °C) has the leakage current of 101.4 nA (4.73 μA). Based on the measured results in Fig. 7, the SCR device obviously contributes a very small part to the total leakage current due to absence of a polygate structure. In addition, the leakage current of the ESD detection circuit is successfully reduced to the order of nanoamperes because the voltage difference across the gate oxide has been reduced by inserting the diode strings.

B. TLP Measurement and ESD Robustness

In order to investigate the protection performance during the ESD stress events, the TLP generator [14] with a pulsewidth of 100 ns and a rise time of ~2 ns is used to measure the second breakdown current (It2) of the fabricated 2 × VDD-tolerant power-rail ESD clamp circuit. The measured results are shown in Fig. 8. The It2 values of the proposed 2 × VDD-tolerant power-rail ESD clamp circuits are 2.11, 2.75, and 3.34 A for the SCR widths of 30, 40, and 50 μm, respectively. In Fig. 8, the TLP-measured $I-V$ curves have no obvious snapback phenomenon and start to rise up after ~2.4 V, which is higher than the normal operating voltage VDD_H of 1.8 V. Therefore, the proposed 2 × VDD-tolerant power-rail ESD clamp circuit is free from the latchup issue.

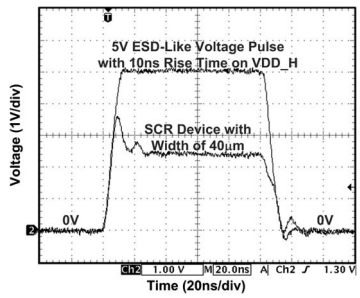

Fig. 9. Measured voltage waveforms of the 2 × VDD-tolerant ESD clamp circuit under the ESD-like condition with a 5-V voltage pulse and a 10-ns rise time.

The It2, HBM, and machine-model (MM) [15] ESD levels of the fabricated 2 × VDD-tolerant power-rail ESD clamp circuit are listed in Table II. The HBM (MM) ESD levels of the proposed 2 × VDD-tolerant power-rail ESD clamp circuits can achieve 3.5, 5.0, and 6.5 kV (150, 250, and 300 V) for the SCR widths of 30, 40, and 50 μm, respectively.

C. Turn-On Verification

In order to observe the turn-on efficiency of the fabricated 2 × VDD-tolerant power-rail ESD clamp circuit, an ESD-like voltage pulse with a rise time of 10 ns and a pulse height of 5 V is applied to VDD_H with grounded VSS to simulate the fast-rising edge of the HBM ESD pulse. The ESD detection circuit will be started to trigger on the SCR device. The measured voltage waveforms on the VDD_H power line under the fast-transient ESD-like stress condition are shown in Fig. 9. In Fig. 9, the applied 5-V voltage pulse is quickly clamped down to a low voltage level of ~2.4 V by the fabricated 2 × VDD-tolerant ESD clamp circuit. The turn-on time is ~5 ns, which is estimated from the maximum voltage peak to the clamped low voltage level in Fig. 9. According to the measured voltage waveforms, the proposed 2 × VDD-tolerant power-rail ESD clamp circuit has been successfully verified with high turn-on efficiency during the ESD stress event.

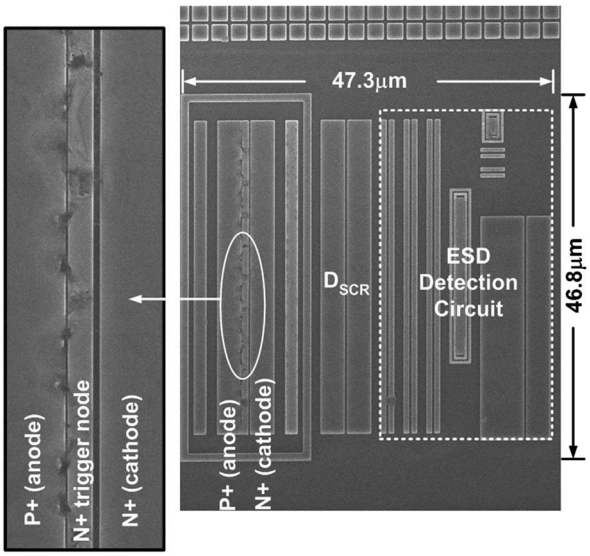

Fig. 10. After a 5-kV VDD_H-to-VSS HBM ESD test, the failure spots were found at the anode-to-cathode path of the whole SCR device, where the SCR is drawn with a width of 40 μm.

TABLE III
COMPARISON WITH PRIOR WORKS

		Prior Work [8]	Prior Work [9]	This Work (Fig. 3)
		W_{SCR} = 45μm Trigger pMOS VDD_H = 1.8V	W_{SCR} = 50μm 25μm Trigger pMOS VDD_H = 2V	W_{SCR} = 50μm 40μm Trigger nMOS VDD_H = 1.8V
Standby Leakage Current	25°C	150nA	170nA	103.7nA
	125°C	1.71μA	1.48μA (@ 100°C)	4.74μA
HBM ESD Level		6.5kV	4.8kV	6.5kV
MM ESD Level		350V	N/A	300V
Trigger Voltage		3~4V	6~7V	~2.4V
Turn-on Time		15ns	N/A	5ns
Layout Area		Small	Large	Small

D. Failure Analysis

To further investigate the turn-on uniformity of the SCR device under ESD stress, the failure analyses were carried out by scanning electron microscopy images. Fig. 10 shows the ESD failure locations on the 2 × VDD-tolerant power-rail ESD clamp circuit with the SCR width of 40 μm after a 5-kV VDD_H-to-VSS HBM ESD test. The anode-to-cathode path along the whole SCR device was found to be damaged, as shown in the zoomed-in figure (at the left-hand side). It implies that the SCR device indeed is turned on uniformly by the proposed ESD detection circuit.

E. Comparison

The comparison between the proposed 2 × VDD-tolerant power-rail ESD clamp circuit and prior works is listed in Table III. The ESD level and the standby leakage current of the proposed design with the SCR device width of only 50 μm are excellent. In addition, because the trigger nMOS used in the ESD detection circuit can conduct a large enough triggering current, the trigger voltage and the turn-on speed of the proposed design are lower and faster than those of prior works.

IV. CONCLUSION

New design of 2 × VDD-tolerant power-rail ESD clamp circuit for mixed-voltage I/O applications has been proposed and successfully verified in 65-nm fully silicided CMOS technology. The new proposed ESD detection circuit is realized with only 1-V devices without suffering the gate oxide reliability issue under 1.8-V (2 × VDD) applications. By inserting the diode strings in the ESD detection circuit, the proposed 2 × VDD-tolerant power-rail ESD clamp circuit demonstrates a standby leakage current of only 103.7 nA under 1.8 V bias at 25 °C. The SCR device with a width of 50 μm can sustain the HBM ESD level of 6.5 kV and the MM ESD level of 300 V. The new proposed 2 × VDD-tolerant power-rail ESD clamp circuit with consideration of the gate leakage current is very useful and cost-effective for on-chip ESD protection in the mixed-voltage I/O buffers.

ACKNOWLEDGMENT

The authors would like to thank Yung-Chih Liang from the Industrial Technology Research Institute for his valuable technical suggestion; Hanwa Electronic Ind. Co., Ltd., Japan, for providing the TLP equipment; and Materials Analysis Technology Inc. (MA-tek), Hsinchu, Taiwan, for the professional failure analysis.

REFERENCES

[1] M. Pelgrom and E. Dijkmans, "A 3/5 V compatible I/O buffer," *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 823–825, Jul. 1995.
[2] G. Singh and R. Salem, "High-voltage-tolerant I/O buffers with low-voltage CMOS process," *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1512–1525, Nov. 1999.
[3] M.-D. Ker and S.-L. Chen, "Design of mixed-voltage I/O buffer by using NMOS-blocking technique," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2324–2333, Oct. 2006.
[4] S. Dabral and T. Maloney, *Basic ESD and I/O Designs*. New York: Wiley, 1998.
[5] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, J. Bialas, L. Longenbach, and J. Howard, "Accelerated gate-oxide breakdown in mixed-voltage I/O circuits," in *Proc. IEEE Int. Rel. Phys. Symp.*, 1997, pp. 169–173.
[6] M.-D. Ker and K.-H. Lin, "Overview on electrostatic discharge protection designs for mixed-voltage I/O interfaces: Design concept and circuit implementations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 2, pp. 235–246, Feb. 2006.
[7] M.-D. Ker and W.-J. Chang, "ESD protection design with on-chip ESD bus and high-voltage-tolerant ESD clamp circuit for mixed-voltage I/O buffers," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1409–1416, Jun. 2008.
[8] C.-T. Wang and M.-D. Ker, "Design of 2 × VDD-tolerant power-rail ESD clamp circuit with consideration of gate leakage current in 65-nm CMOS technology," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1460–1465, Jun. 2010.
[9] M.-D. Ker and C.-Y. Lin, "High-voltage-tolerant ESD clamp circuit with low standby leakage in nanoscale CMOS process," *IEEE Trans. Electron Devices*, vol. 57, no. 7, pp. 1636–1641, Jul. 2010.
[10] BSIM Model, Berkeley Short-Channel IGFET Model. [Online]. Available: http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html
[11] M.-D. Ker and K.-C. Hsu, "Latchup-free ESD protection design with complementary substrate-triggered SCR devices," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1380–1392, Aug. 2003.
[12] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits*. Hoboken, NJ: Wiley, 2009.
[13] Electrostatic Discharge Sensitivity Testing—Human Body Model (HBM)—Component Level, ESD Association Standard, Test Method ESD STM5.1, 2001.
[14] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. EOS/ESD Symp.*, 1985, pp. 49–54.
[15] Electrostatic Discharge Sensitivity Testing—Machine Model (MM)—Component Level, ESD Association Standard, Test Method ESD STM5.2, 1999.